

LKP51200series

Sink and Source DDR

Termination Regulator

LKP51200 series Sink and Source DDR Termination Regulator

1 FEATURES

- Input voltage: Supports 2.5V rail and 3.3V rail
- VLDOIN voltage range: 1.1V to 3.5V
- Requires minimum output capacitance of 20 μ F
- PGOOD to monitor output regulation
- Remote sensing (VOSNS)
- Undervoltage and thermal protection
- Built-in soft start
- Supports DDR, DDR2, DDR3, DDR3L, Low-Power DDR3, and DDR4 VTT applications
- Package: DFN10 (3.00mm $\times$ 3.00mm $\times$ 0.80mm), plastic package

2 APPLICATIONS

- Memory termination regulator for DDR, DDR2, DDR3, DDR3L, Low-Power DDR3, and DDR4
- Notebooks, desktops, and servers
- Telecom and datacom
- Base stations
- LCD-TVs and PDP-TVs
- Copiers and printers

- Set-top boxes

3 GENERAL DESCRIPTION

The LKP51200DF device is a sink and source DDR termination regulator specifically designed for low input

PART NUMBER	PACKAGE	PACKAGE SIZE
LKP51200DF	DFN10	3.00mm $\times$ 3.00mm $\times$ 0.80mm

voltage, low-cost, low-noise systems where space is a key consideration.

The device maintains a fast transient response and requires a minimum output capacitance of only 20 μ F. The device supports a remote sensing function and all power requirements for DDR, DDR2, DDR3, DDR3L, Low-Power DDR3, and DDR4 VTT bus termination.

In addition, the LKP51200DF provides an open-drain PGOOD signal to monitor the output regulation and an EN signal that can be used to discharge VTT during S3 (suspend to RAM) for DDR applications.

Device Information

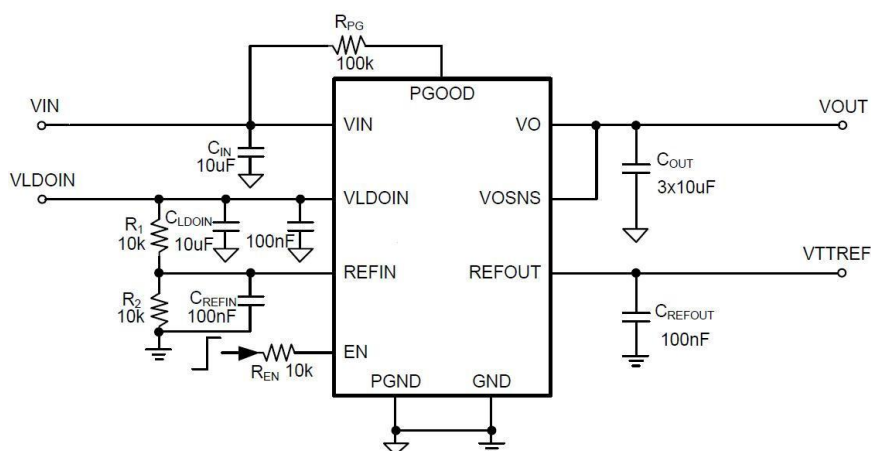


Figure 1. LKP51200DF Typical Application Diagram

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4 Pin Configuration and Functions

4.1 Pin Configuration

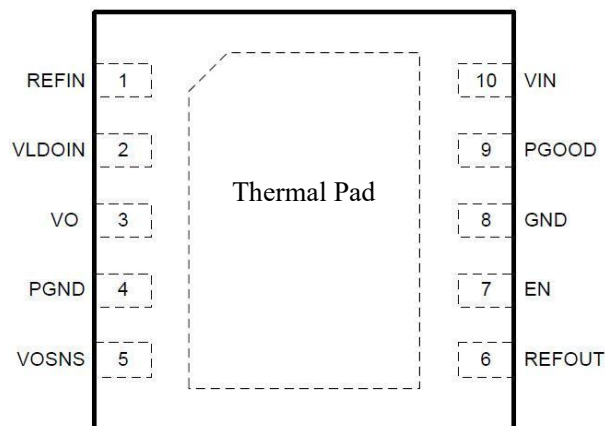


Figure 2. Pin Configuration (Top View)

Table 1. Pin Functions

NO.	Symbol	Description
1	REFIN	Reference input. A 100nF ceramic capacitor to GND is recommended.
2	VLDOIN	Supply voltage for the LDO. A minimum 10 μ F ceramic capacitor to PGND is recommended.
3	VO	Power output for the LDO. A minimum 20 μ F ceramic capacitor to PGND is recommended (place as close as possible to the output).
4	PGND	Power ground for the LDO.
5	VOSNS	Voltage sense input for the LDO. Connect to the positive terminal of the output capacitor or the load.
6	REFOUT	Reference output. A 100nF ceramic capacitor to GND is recommended.
7	EN	Enable control, active high. For auto-start, connect EN to VIN. Do not leave floating. For DDR VTT application, connect to SLP_S3.
8	GND	Signal ground.
9	PGOOD	Open-drain, power-good indicator. Asserts high when output is within $\pm 20\%$ of REFOUT.
10	VIN	Power supply input. A minimum 1 μ F ceramic capacitor to GND is recommended.
Thermal Pad		Thermal pad. Must be soldered to the PCB ground plane for proper thermal performance.

5 Specifications

5.1 Absolute Maximum Ratings (over operating free-air temperature range, unless otherwise noted) ⁽¹⁾

Parameter	Symbol	MIN	MAX	UNIT
VIN pin voltage	V _{IN}	-0.3	3.6	V
VO pin voltage	V _{OUT}	-0.3	3.6	V
REFIN pin voltage	V _{REFIN}	-0.3	3.6	V
REFOUT pin voltage	V _{REFOUT}	-0.3	3.6	V
VOSNS pin voltage	V _{VOSNS}	-0.3	3.6	V
VLDOIN pin voltage	V _{VLDOIN}	-0.3	3.6	V
EN pin voltage	V _{EN}	-0.3	6.5	V
PGOOD pin voltage	V _{PGOOD}	-0.3	6.5	V
Power dissipation	P _D	-	2	W
Pin soldering temperature (5s)	T _h	240	250	°C
Storage temperature range	T _{STG}	-55	150	°C
Junction temperature range	T _J	150		°C

(1): Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability and lifetime.

5.2 Recommended Operating Conditions

Parameter	Symbol	MIN	MAX	UNIT
VIN pin voltage	V _{IN}	2.375	3.5	V
VO pin voltage	V _{OUT}	0	3.5	V
REFIN pin voltage	V _{REFIN}	0.5	1.8	V
REFOUT pin voltage	V _{REFOUT}	0	1.8	V
VOSNS pin voltage	V _{VOSNS}	0	3.5	V
VLDOIN pin voltage	V _{VLDOIN}	0	3.5	V
EN pin voltage	V _{EN}	0	3.5	V
PGOOD pin voltage	V _{PGOOD}	0	3.5	V
Operating free-air temperature	T _A	-40	+85	°C

5.3 Thermal Information

THERMAL METRIC ⁽¹⁾	LKP51200DF	UNIT
	10 PINS	
R _{θJc (top)} Junction-to-case (top) thermal resistance	86	°C/W
R _{θJc (bot)} Junction-to-case (bottom) thermal resistance	12	°C/W

(1): Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability and lifetime.

5.4 Electrical Characteristics

(TA=25°C, unless otherwise specified)

Parameter	Symbol	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply current	I _{IN}	V _{EN} =3.3V, No load	-	0.7	2	mA
Shutdown current	I _{SHDN}	V _{EN} =0V, V _{REFIN} =0V, No load	-	65	100	μA
		V _{EN} =0V, V _{REFIN} >0.4V, No load	-	200	500	μA
VLDOIN input current	I _{LDOIN}	V _{EN} =3.3V, No load	-	1	50	μA
VLDOIN Shutdown current	I _{LDOIN(SDN)}	V _{EN} =0V, No load	-	0.1	50	μA
REFIN Shutdown current	I _{REFIN}	V _{EN} =3.3V	-	-	1	μA
VO output DC voltage	V _{VOSNS}	V _{REFOUT} =1.25V(DDR1), I _O =0A	1.235	1.25	1.265	V
		V _{REFOUT} =0.9V(DDR2), I _O =0A	0.885	0.9	0.915	V
		V _{REFOUT} =0.75V(DDR3), I _O =0A	0.735	0.75	0.765	V
		V _{REFOUT} =0.675V(DDR3L), I _O =0A	0.660	0.675	0.690	V
		V _{REFOUT} =0.6V(DDR4), I _O =0A	0.585	0.6	0.615	V
VO output voltage tolerance	V _{VOTOL}	-2A<I _{VO} <2A, T _A =25°C	-25	-	25	mV
VO source current limit	I _{VOSRCL}	With reference to REFOUT, V _{VOSNS} =0.9V _{REFOUT} , T _A =25°C	3	-	4.5	A
VO sink current limit	I _{VOSNCL}	With reference to REFOUT, V _{VOSNS} =1.1V _{REFOUT} , T _A =25°C	3.5	-	5.5	A
Output discharge resistance	R _{DSCHRG}	V _{REFIN} =0V, V _{OUT} =0.3V, V _{EN} =0V, T _A =25°C	-	18	25	Ω
PGOOD threshold	V _{TH(PG)}	PGOOD window lower threshold with respect to REFOUT	-23.5	-20	-17.5	%
		PGOOD window upper threshold with respect to REFOUT	17.5	20	23.5	
		Hysteresis,	-	5	-	

PGOOD start-up delay	TPGDLY	Rising edge	-	2	-	ms
PGOOD output low voltage	VPGLow	ISINK = 4mA	-	-	0.4	V
Parameter	Symbol	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PGOOD bad delay	TPBADDLY	VVOSNS is outside the $\pm 20\%$ PGOOD window	-	10	-	μ s
PGOOD leakage current	IPGLK	VVOSNS = VREFIN (PGOOD high impedance), VP GOOD = VVIN + 0.2V	-		1	μ A
REFIN voltage range	VREFIN	-	0.5	-	1.8	V
REFIN undervoltage lockout	VREFIN_UVLO	REFIN rising	360	390	420	mV
REFIN undervoltage lockout hysteresis	VREFIN-UVHYS	-	-	30	-	mV
REFOUT voltage	VREFOUT	-	-	REFIN	-	V
REFOUT voltage tolerance	VREFOUTTOL	-1mA<IREFOUT<1mA, VREFIN=1.25V	-12	-	12	mV
		-1mA<IREFOUT<1mA, VREFIN=0.9V	-12	-	12	mV
		-1mA<IREFOUT<1mA, VREFIN=0.75V	-12	-	12	mV
		-1mA<IREFOUT<1mA, VREFIN=0.675V	-12	-	12	mV
		-1mA<IREFOUT<1mA, VREFIN=0.6V	-12	-	12	mV
REFOUT source current limit	VREFOUTSRCL	VREFOUT=0V	10	40	-	mA
REFOUT sink current limit	VREFOUTSNCL	VREFOUT=0V	10	40	-	mA
VIN UVLO threshold	VVIN_UVLO	-	2.2	2.3	2.4	V
VIN UVLO hysteresis	VVIN_UVHYS	-	-	60	-	mV
High-level input voltage	VENIH	-	1.7	-	-	V
Low-level input voltage	VENIL	-	-	-	0.3	V
Enable input current	IENLK	VEN=3.3V	-1	0.1	1	μ A
Thermal shutdown threshold	TSD	-	-	150	-	$^{\circ}$ C
Thermal shutdown hysteresis	THYS	-	-	20	-	$^{\circ}$ C

6 Typical Characteristics

$3 \times 10\mu\text{F}$ ceramic capacitors used on output.

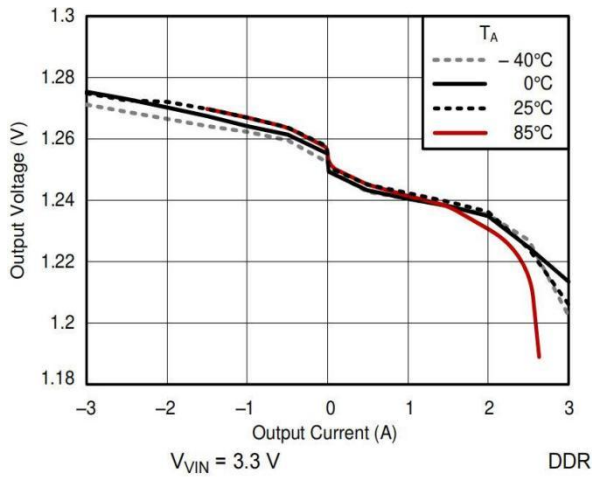


Figure 3. Load Regulation

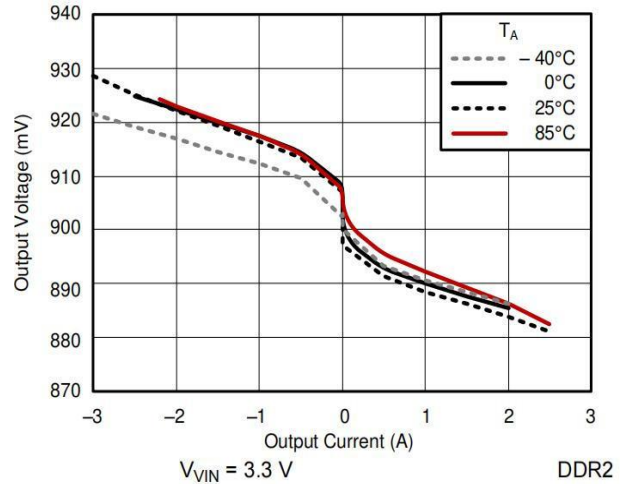


Figure 4. Load Regulation

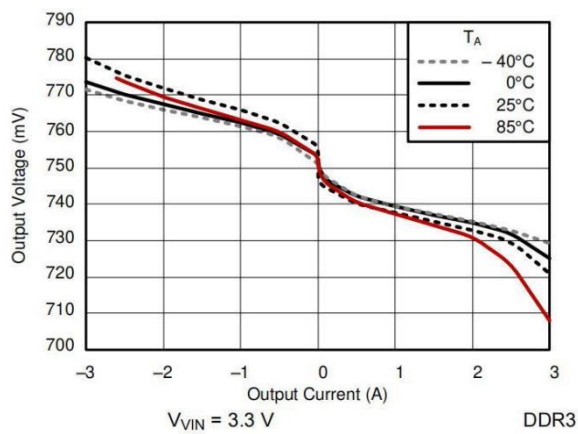


Figure 5. Load Regulation

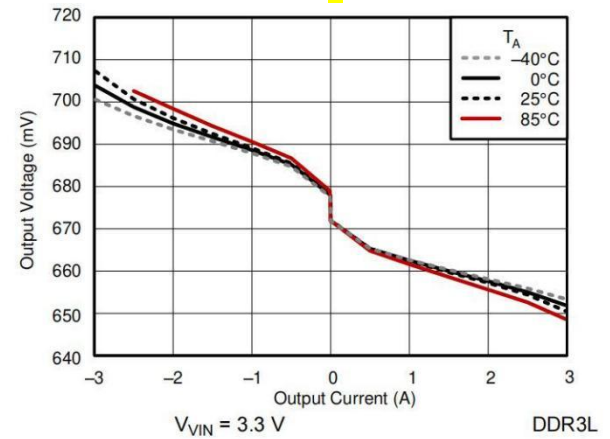


Figure 6. Load Regulation

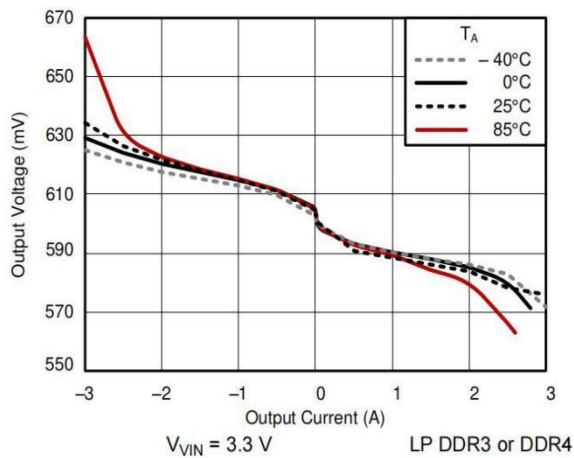


Figure 7. Load Regulation

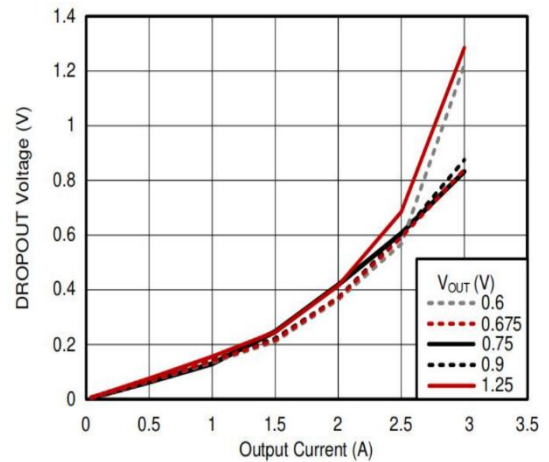


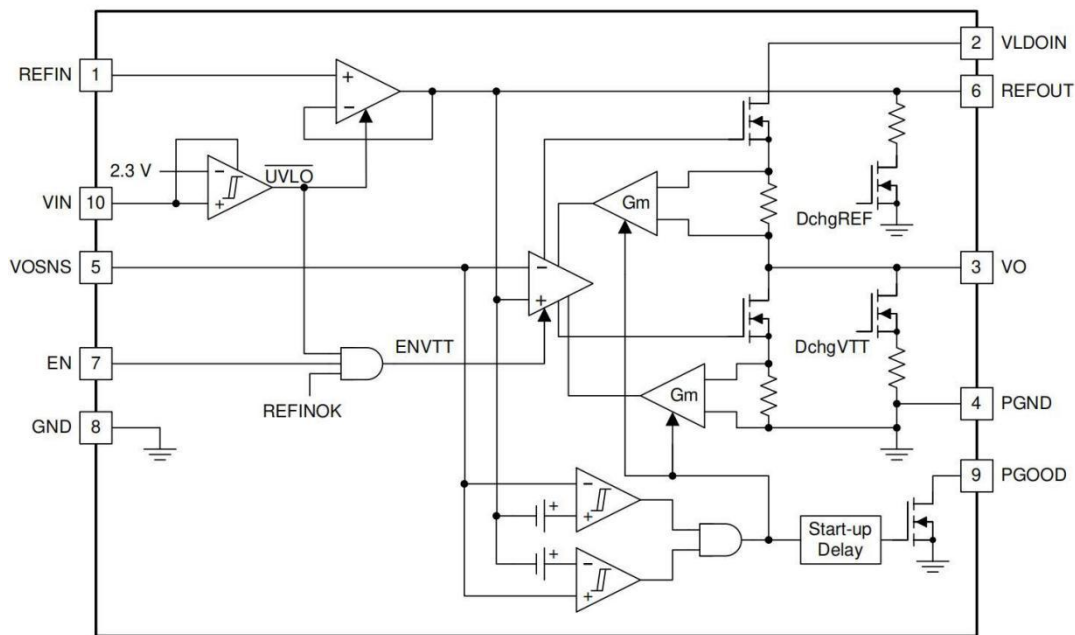
Figure 8. Dropout Voltage vs Output Current

7 Application Information

7.1 Functional Description

The LKP51200DF device is a DDR termination regulator specifically designed for low input voltage, low-cost, low-noise systems where space is a key consideration. The device maintains a fast transient response and requires a minimum output capacitance of only 20 μ F. The device supports a remote sensing function and all power requirements for DDR, DDR2, DDR3, DDR3L, Low-Power DDR3, and DDR4 VTT bus termination.

7.2 Functional Block Diagram



7.3 Typical Application

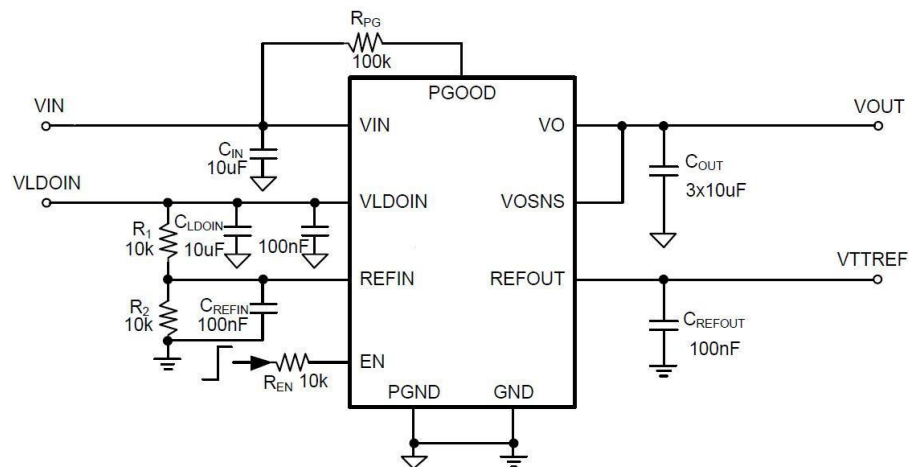


Figure 9. Typical Application

NOTE 1: CIN – A minimum 10 μ F, X7R or higher grade ceramic capacitor is recommended. Place CIN between VIN and PGND and minimize the loop formed by the capacitor and VIN/PGND. For VIN undervoltage lockout (UVLO) protection, when VIN is lower than the UVLO threshold voltage, both VO and REFOUT are powered off. This shutdown is a non-latch protection.

NOTE 2: CLDOIN – A 10 μ F + 100nF ceramic capacitor combination is recommended. If a larger COUT ceramic capacitor is used, it is recommended that the CLDOIN capacitance be half of COUT.

NOTE 3: COUT – Three 10 μ F, X7R ceramic capacitors are recommended to minimize ESR and ESL. Place them as close as possible to the VO pin. To achieve tight regulation with minimum effect of trace resistance, connect VOSNS as a separate trace from the high current path to the positive terminal of the load or COUT.

7.4 Output Load Considerations

PCB traces should be kept short. Input and output capacitors should be placed as close as possible to the device pins. Ensure that the thermal pad on the bottom of the device is connected to the PCB ground plane.

7.5 Reference Input

REFIN is the reference input. The REFOUT output voltage follows REFIN within the VREFOUT range.

When REFIN is configured for standard DDR termination applications, REFIN can be set by an external equivalent ratio voltage divider connected to the memory supply bus (VDDQ). The LKP51200DF supports REFIN voltages from 0.5V to 1.8V.

7.6 Reference Output

REFOUT is the reference output. When configured for DDR termination applications, REFOUT provides the DDR VTT reference voltage for the memory application. It is capable of supporting both sourcing and sinking loads of 10mA. REFOUT becomes active when REFIN voltage rises to 0.39V and VIN is above the UVLO threshold. When REFOUT is less than 0.375V, it is disabled and subsequently discharges to GND through an internal 10k Ω MOSFET. REFOUT is independent of the EN pin state.

7.7 Power Good

The LKP51200DF provides an open-drain PGOOD output that goes high when the VO output is within $\pm 20\%$ of REFOUT. PGOOD de-asserts within 10 μ s after the output exceeds the size of the PGOOD window. During initial VO start-up, PGOOD asserts high 2ms (typ) after VO enters the PGOOD window. Because PGOOD is an open-drain output, a pull-up resistor of 100k Ω is recommended.

7.8 Output Capacitor and Transient Response

The ESR of the output capacitor affects stability, especially with small capacitance. A minimum output capacitance of 10 μ F with an ESR of 3 Ω or less is recommended to prevent oscillation.

Special consideration must be given to the use of ceramic capacitors. Different dielectric types (Z5U, Y5V, X5R, X7R) have different performance under temperature and applied voltage. X5R and X7R have more stable characteristics and are preferred as output capacitors. X7R offers better stability over temperature, while X5R is more cost-effective.

Voltage and temperature coefficients are not the only sources of issues. Some ceramic capacitors exhibit piezoelectric response, generating voltage under mechanical stress from vibration or thermal transients in the system.

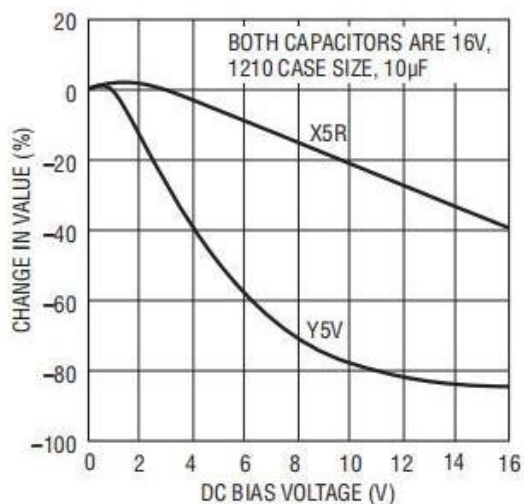


Figure 10. Ceramic Capacitor DC Bias Characteristic

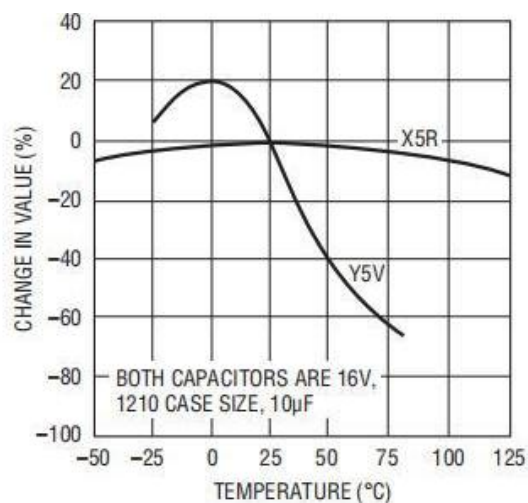
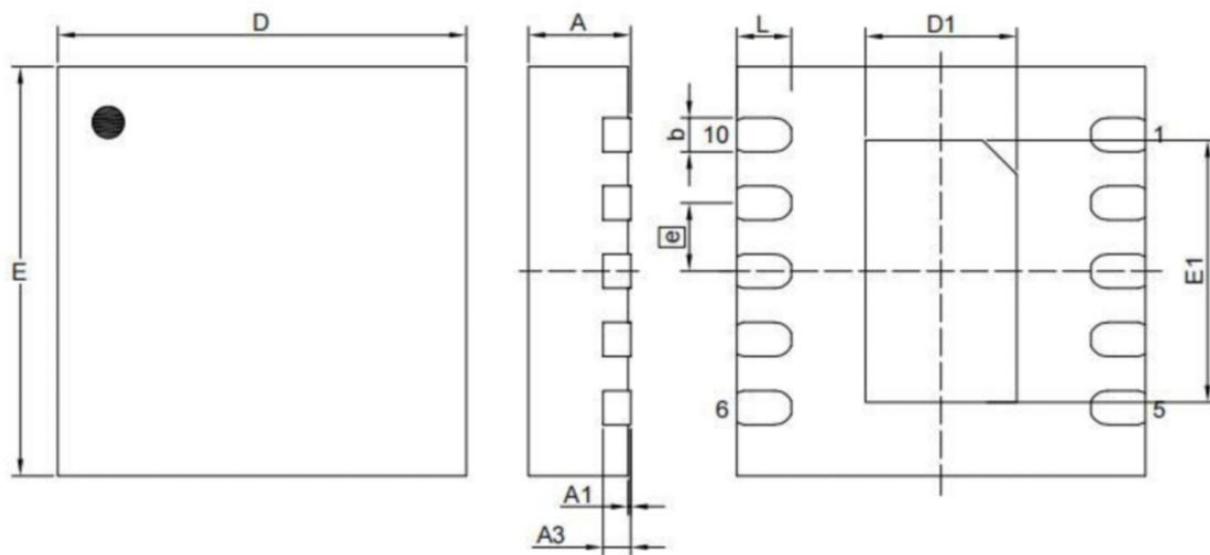


Figure 11. Ceramic Capacitor Temperature Characteristic

8 Package Information



DIM	Unit: mm		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203REF		
b	0.18	0.24	0.30
D	3.00BSC		
D1	1.11	1.45	1.80
E	3.00BSC		
E1	1.92	2.21	2.50
e	0.50BSC		
L	0.27	0.37	0.47

9 Ordering Information

LK

①

P

②

51200

③

DF

④

① Product Series Code

② Classification Identifier

③ Product Code

④ Package Type

Table 2. Ordering Information

Part Number	Package	Quality Grade	Operating Temperature
LKP51200DF	DFN10, Plastic Package	Industrial	-40°C~+85°C

10 Packaging Information

Version Number	Date	Version Description	Change Description
REV 1.00	2024-11-04	Updated version	—
REV 1.01	2025-12-01	Updated version	Package update
REV 1.02	2026-5-20	Updated version	Data update