TECH PUBLIC
台舟电子

DMP22D5UFB4-TP

N-Channel Enhancement Mode MOSFET

WWW.TECHPUBLIC.COM

Features

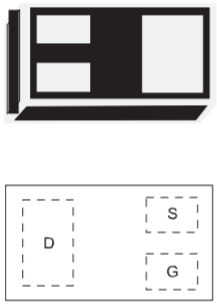
VDS = 20V

- RDS(ON) =300mΩ (typ.) @ VGS= 2.5V
- RDS(ON) =250mΩ (typ.) @ VGS= 4.5V
- ESD Protected up to 2KV

Application

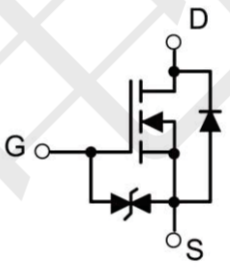
- Load/Power Switching
- Interfacing Switching
- Battery Management for Ultra Small Portable Electronics
- Logic Level Shift

Package and Pin Configuration



DFN1006-3L

Circuit diagram



Absolute Maximum Ratings (T_A=25°C unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	±8	V
Continuous Drain Current	I_D	0.9	A
Pulsed Drain Current (t=300μs) (1)	I_{DM}	1.5	A
Power Dissipation (2)	P_D	0.35	W
Thermal Resistance from Junction to Ambient	$R_{\theta JA}$	357	℃/W
Junction Temperature	T_J	150	℃
Storage Temperature	T_{STG}	-55~ +150	℃

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Type	Max	Unit
Static Characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D =250μA	20	25		V
Zero gate voltage drain current	I_{DSS}	V_{DS} =20V,V_{GS} = 0V			1	μA
Gate-body leakage current	I_{GSS}	V_{GS} =±18V, V_{DS} = 0V			±10	μA
Gate threshold voltage(3)	$V_{GS(th)}$	V_{DS} =V_{GS}, I_D =250μA	0.5	0.7	1.1	V
Drain-source on-resistance(3)	$R_{DS(on)}$	V_{GS} =4.5V, I_D =500mA		250	400	mΩ
		V_{GS} =2 5V I_D =500mA		300	500	
Forward tranconductance	g_{FS}	V_{DS} =10V, I_D =500mA			1.2	S
Dynamic characteristics(4)						
Input Capacitance	C_{iss}	V_{DS} =10V,V_{GS} =0V,f =1MHz		45		pF
Output Capacitance	C_{oss}			9		
Reverse Transfer Capacitance	C_{rss}			6		
Switching Characteristics(4)						
Turn-on delay time	$t_{d(on)}$	V_{GS}=4.5V,V_{DS}=10V, I_D=2A,R_{GEN}=6Ω		1.2		ns
Turn-on rise time	t_r			25		
Turn-off delay time	$t_{d(off)}$			14		
Turn-off fall time	t_f			17		
Source-Drain Diode characteristics						
Diode Forward voltage(3)	V_{DS}	I_S=0.15A, V_{GS} = 0V			1.3	V

Characteristic Curves

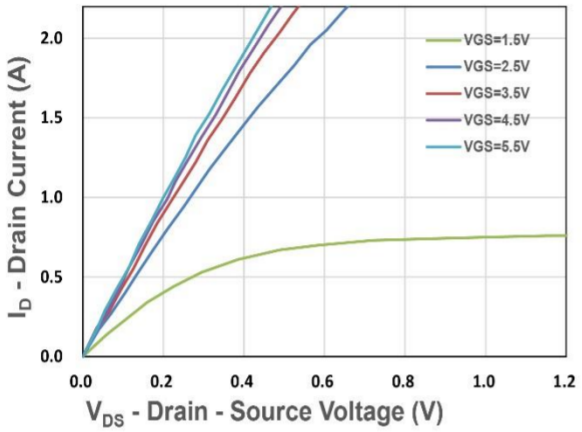


Figure 1. Output Characteristics

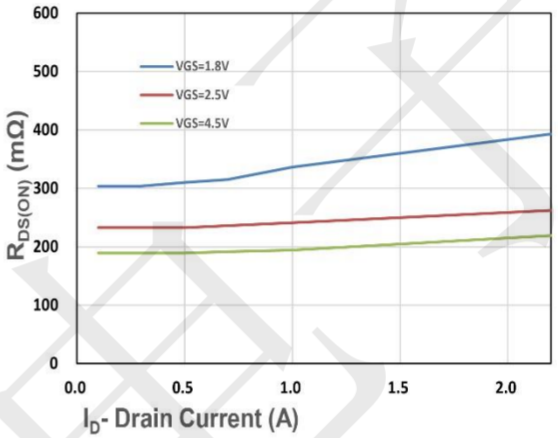


Figure 2. On-Resistance vs. ID

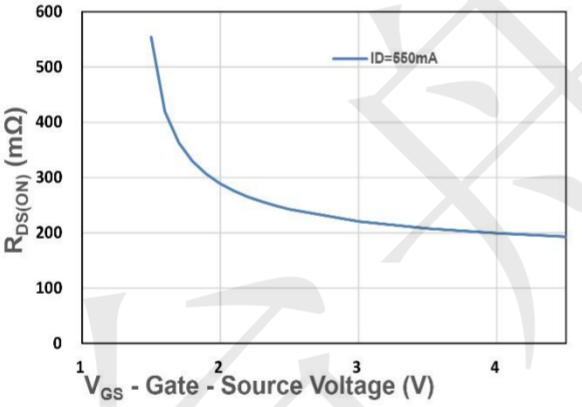


Figure 3. On-Resistance vs. VGS

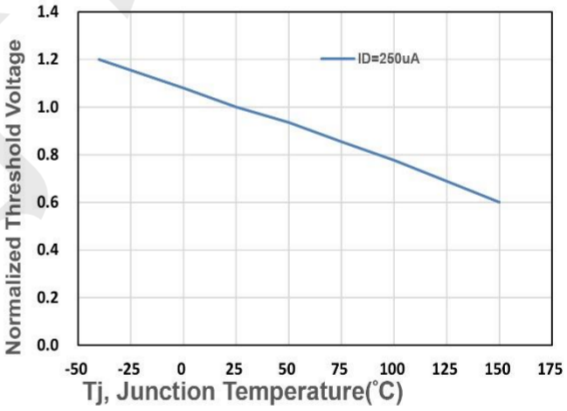


Figure 4. Gate Threshold Voltage

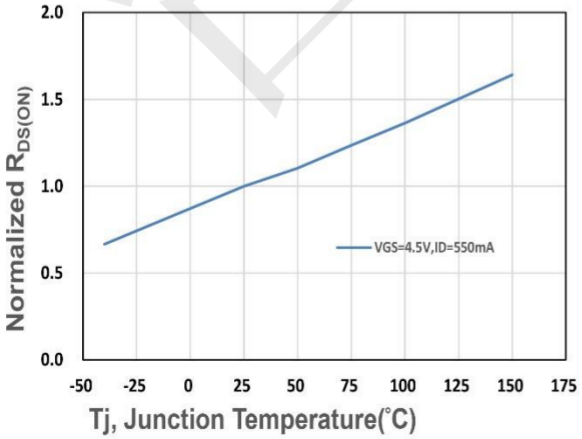


Figure 5. Drain-Source On Resistance

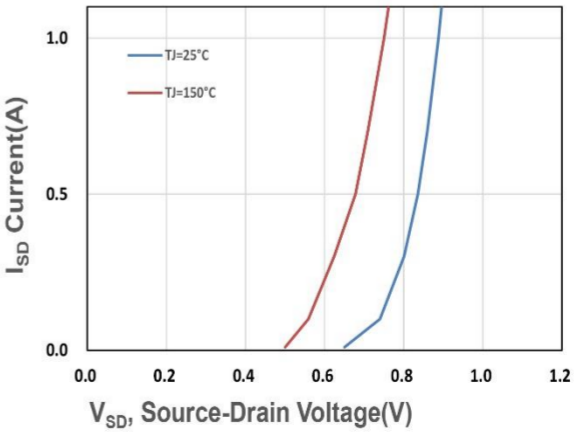


Figure 6. Source-Drain Diode Forward

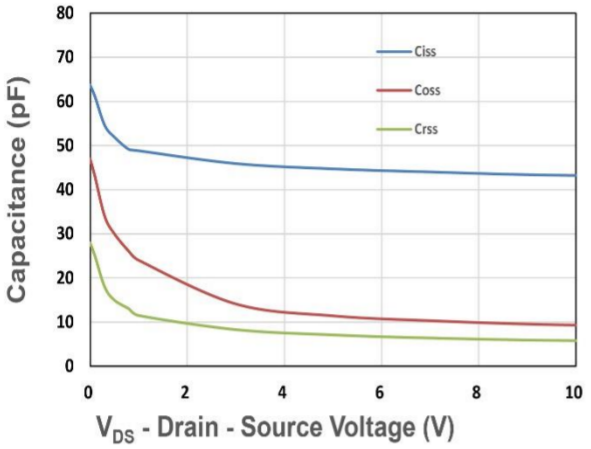


Figure 7. Capacitance

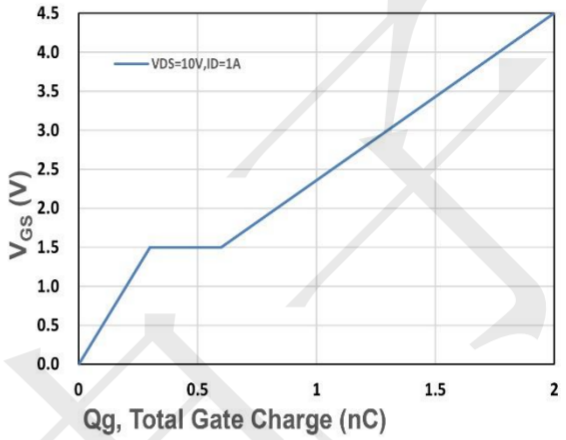


Figure 8. Gate Charge Characteristics

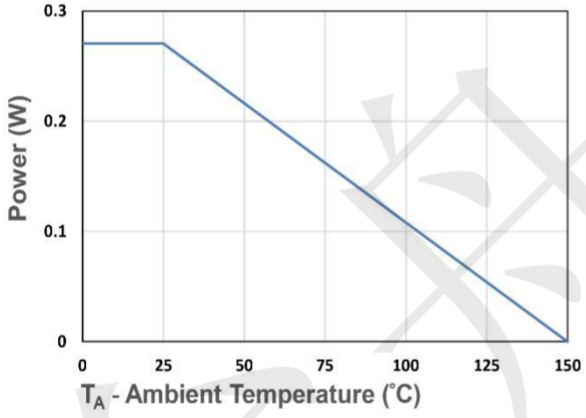


Figure 9. Power Dissipation

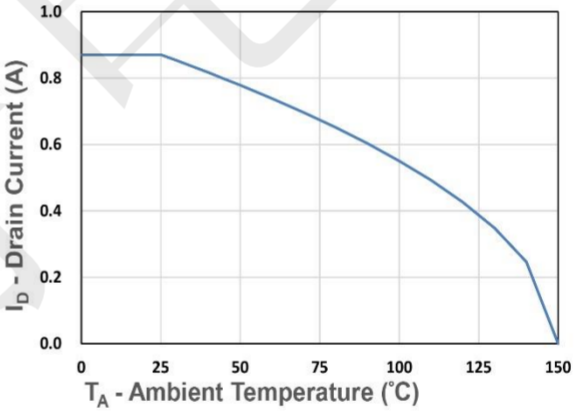


Figure 10. Drain Current

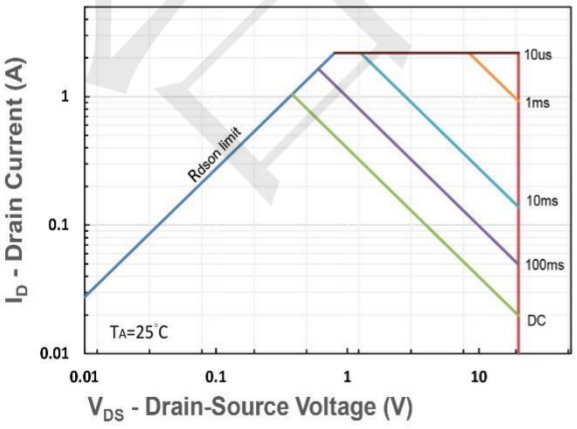


Figure 11. Safe Operating Area

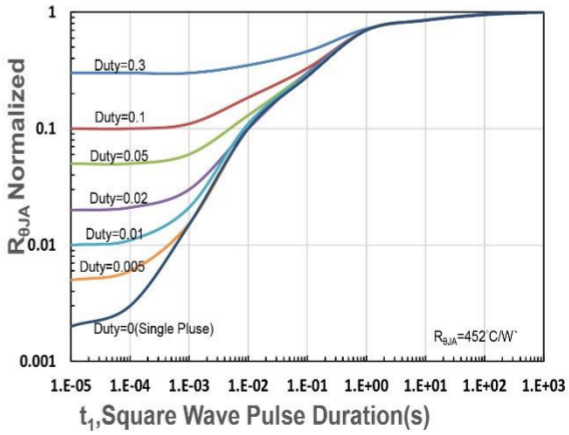
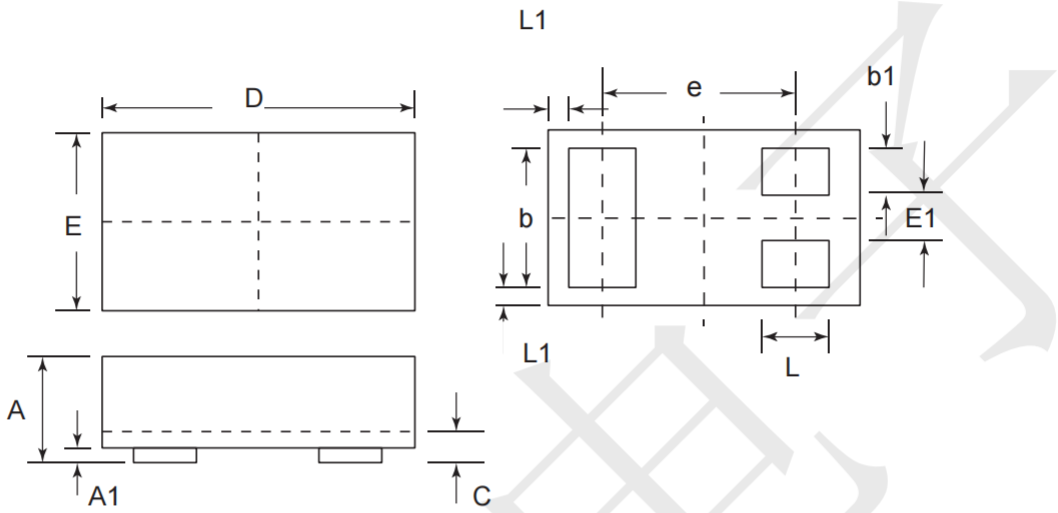


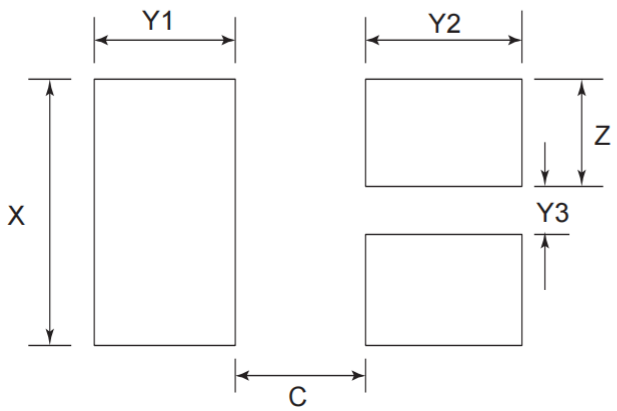
Figure 12. RθJA Transient Thermal Impedance

DFN1006-3L Package Outline Drawing



SYM	DIMENSIONS					
	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.45	0.50	0.55	0.018	0.020	0.022
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.45	0.50	0.55	0.018	0.020	0.022
b1	0.10	0.15	0.20	0.004	0.006	0.008
C	0.12	0.15	0.18	0.005	0.006	0.007
D	0.95	1.00	1.05	0.037	0.039	0.041
e	0.65 BSC			0.026 BSC		
E	0.55	0.60	0.65	0.022	0.024	0.026
E1	0.15	0.20	0.25	0.006	0.008	0.010
L	0.20	0.25	0.30	0.008	0.010	0.012
L1	0.05 REF			0.0002 REF		

Suggested Land Pattern



SYM	DIMENSIONS	
	MILLIMETERS	INCHES
C	0.25	0.010
X	0.65	0.024
Y1	0.50	0.020
Y2	0.50	0.020
Y3	0.25	0.010
Z	0.20	0.008