

Description:

This N+N Channel MOSFET uses advanced trench technology and design to provide excellent $R_{DS(on)}$ with low gate charge.

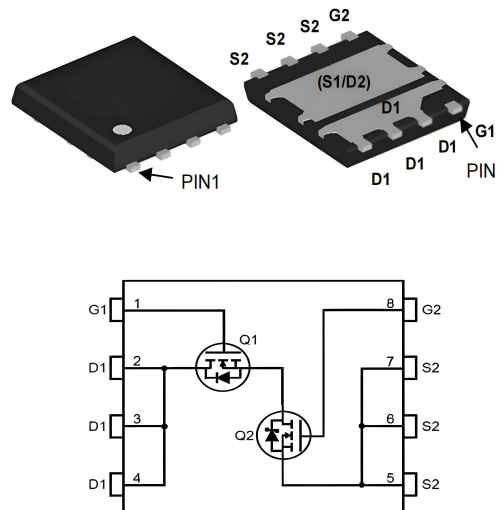
It can be used in a wide variety of applications.

Features:

N-Channel: $V_{DS}=40V, I_D=45A, R_{DS(on)} < 7.5m\Omega @ V_{GS}=10V$ (Typ: $6m\Omega$)

N-Channel: $V_{DS}=40V, I_D=60A, R_{DS(on)} < 5.5m\Omega @ V_{GS}=10V$ (Typ: $4.5m\Omega$)

- 1) Low gate charge.
- 2) Green device available.
- 3) Advanced high cell density trench technology for ultra low $R_{DS(on)}$.
- 4) Excellent package for good heat dissipation.
- 5) MSL3



Package Marking and Ordering Information:

Part NO.	Marking	Package	Packing
TMD0705DTG	D0705DT	TDFN5*6 Asym	5000 pcs/Reel

Absolute Maximum Ratings: ($T_C=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	N-Channel	N-Channel	Units
V_{DS}	Drain-Source Voltage	40	40	V
V_{GS}	Gate-Source Voltage	± 20	± 20	V
I_D	Continuous Drain Current- $T_C=25^\circ\text{C}^1$	45	60	A
	Continuous Drain Current- $T_C=100^\circ\text{C}^1$	31.5	42	
I_{DM}	Pulsed Drain Current ²	180	240	A
E_{AS}	Single pulse avalanche energy ³	36	85	mJ
P_D	Power Dissipation - $T_C=25^\circ\text{C}$	40	50	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150		$^\circ\text{C}$

Thermal Characteristics:

Symbol	Parameter	N-CH	P-CH	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Cast	3.1	2.5	$^\circ\text{C}/\text{W}$

N-Channel Electrical Characteristics: ($T_C=25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Off Characteristics						
BV _{DSS}	Drain-Sourtce Breakdown Voltage	V _{GS} =0V,I _D =250 μ A	40	---	---	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{GS} =0V, V _{DS} =40V	---	---	1	μ A
I _{GSS}	Gate-Source Leakage Current	V _{GS} =± 20V, V _{DS} =0A	---	---	± 100	nA
On Characteristics						
V _{GS(th)}	Gate-Source Threshold Voltage	V _{GS} =V _{DS} , I _D =250 μ A	1	1.5	2	V
R _{DS(ON)}	Drain-Source On Resistance ⁴	V _{GS} =10V,I _D =20A	---	6	7.5	m Ω
		V _{GS} =4.5V,I _D =10A	---	9	11	m Ω
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} =20V, V _{GS} =0V, f=1MHz	---	660	---	pF
C _{oss}	Output Capacitance		---	357	--	
C _{rss}	Reverse Transfer Capacitance		---	26	---	
Switching Characteristics						
t _{d(on)}	Turn-On Delay Time	V _{DS} =20V, I _D =50A, R _{ENG} =3 Ω ,V _{GS} =10V	---	5	---	ns
t _r	Rise Time		---	3	---	ns
t _{d(off)}	Turn-Off Delay Time		---	21	---	ns
t _f	Fall Time		---	2.3	---	ns
Q _g	Total Gate Charge	V _{GS} =10V, V _{DS} =20V, I _D =50A	---	12	---	nC
Q _{gs}	Gate-Source Charge		---	1.8	---	nC
Q _{gd}	Gate-Drain “Miller” Charge		---	2.3	---	nC
Drain-Source Diode Characteristics						
V _{SD}	Diode Forward Voltage	V _{GS} =0V, I _{SD} =1A	---	---	1.2	V
I _S	Continuous Drain Curren	V _D =V _G =0V	---	---	45	A
I _{SM}	Pulsed Drain Current		---	---	180	A

Notes:

1. Computed continuous current assumes the condition of $T_{j,Max}$ while the actual continuous current depends on the thermal & electro-mechanical application board design
2. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
3. EAS condition : $T_J=25^{\circ}C, V_{DD}=20V, V_G=10V, L=0.5mH$
4. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 0.5\%$

N-Typical Characteristics: ($T_C=25^{\circ}C$ unless otherwise noted)

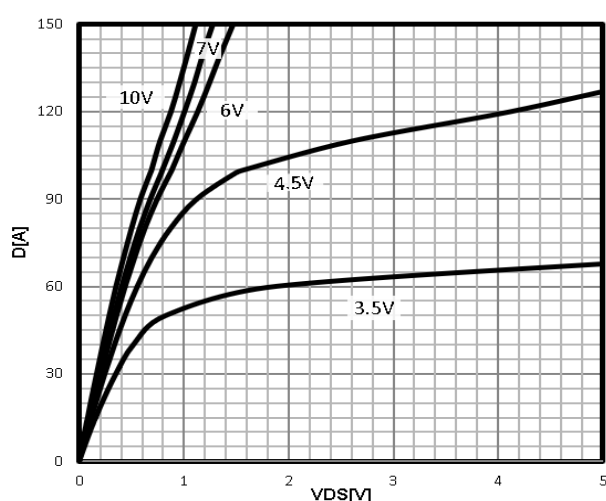


Figure 1: Typ. output characteristics
 $I_D=f(V_{DS})$

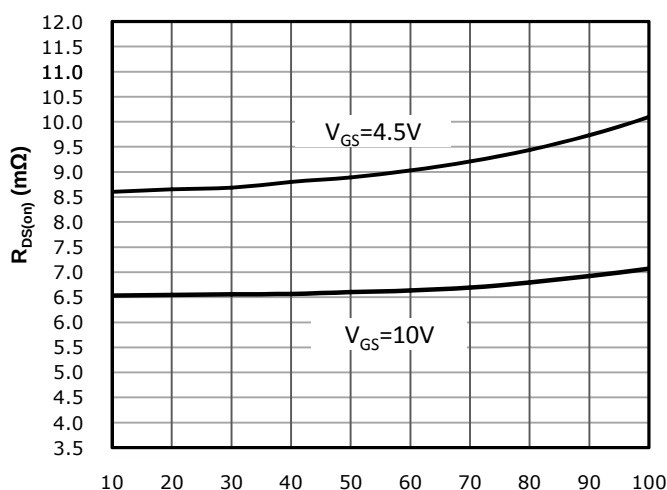


Figure 2: $R_{DS(on)}$ vs Drain Current and Gate Voltage

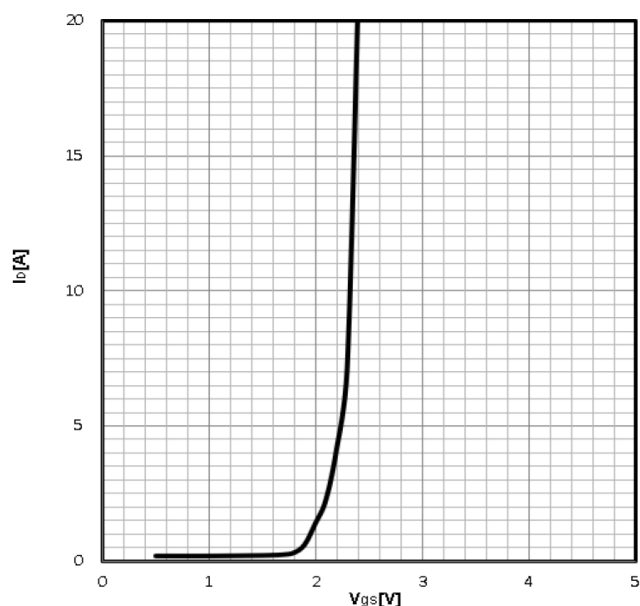


Figure 3: Typ. transfer characteristics
 $I_D=f(V_{GS})$

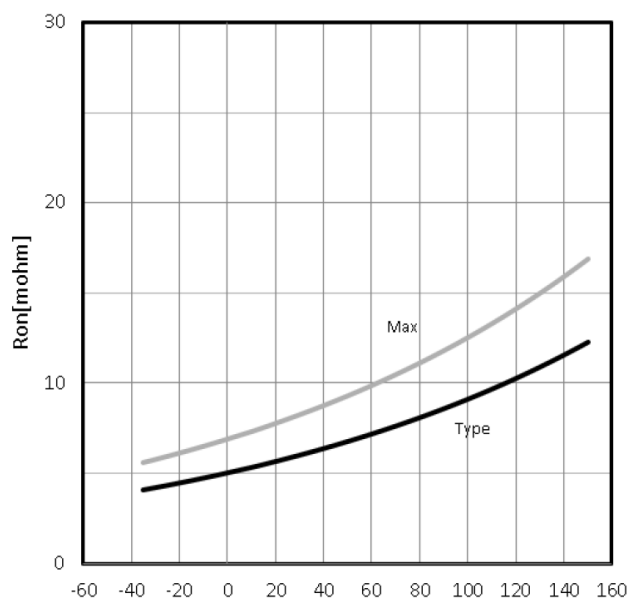


Figure 4: Drain-source on-state resistance
 $R_{DS(on)}=f(T_j); I_D=12A;$

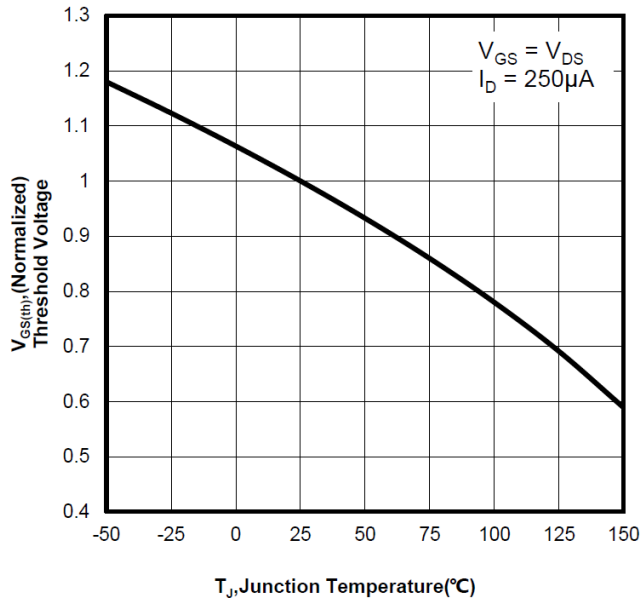


Figure 5 Gate Threshold Voltage
 $V_{TH}=f(T_J)$; $I_D=250\mu A$

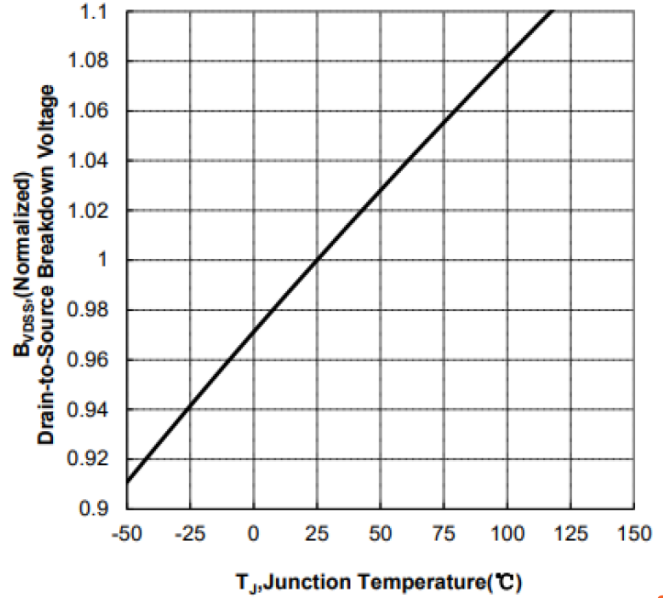


Figure 6: Drain-source breakdown voltage
 $V_{BR(DSS)}=f(T_J)$; $I_D=250\mu A$

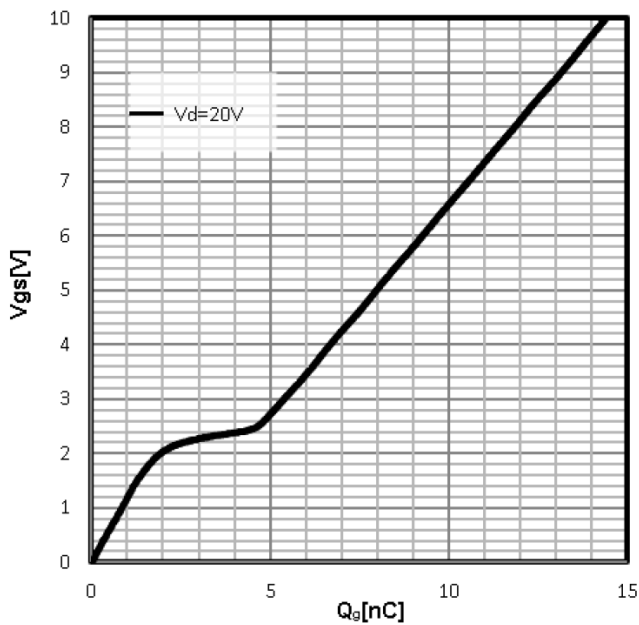


Figure 7: Typ. gate charge
 $V_{GS}=f(Q_g)$; $I_D=5A$

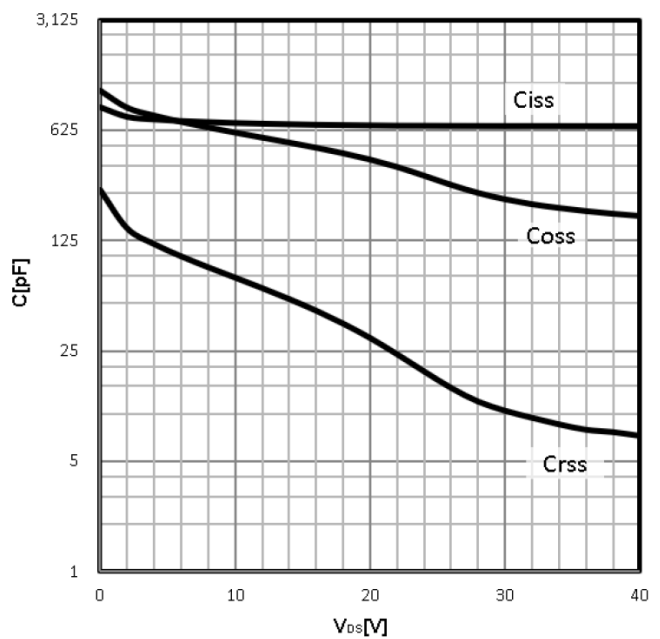


Figure 8: Typ. capacitances
 $C=f(V_{DS})$; $V_{GS}=0V$; $f=1MHz$

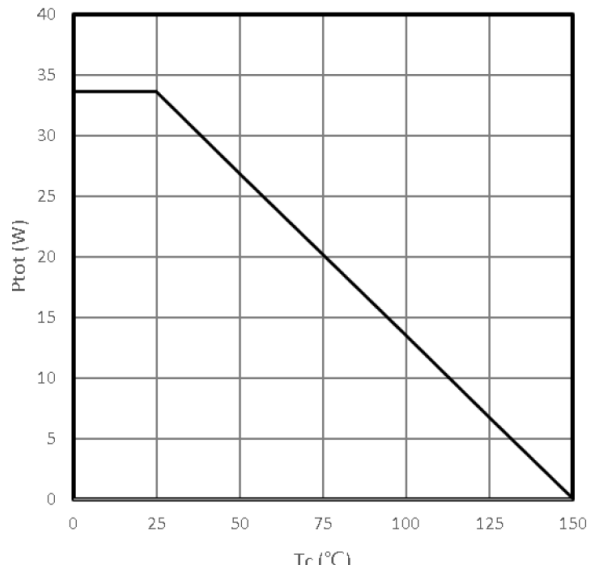


Figure 9: Power Dissipation
 $P_{tot}=f(T_c)$

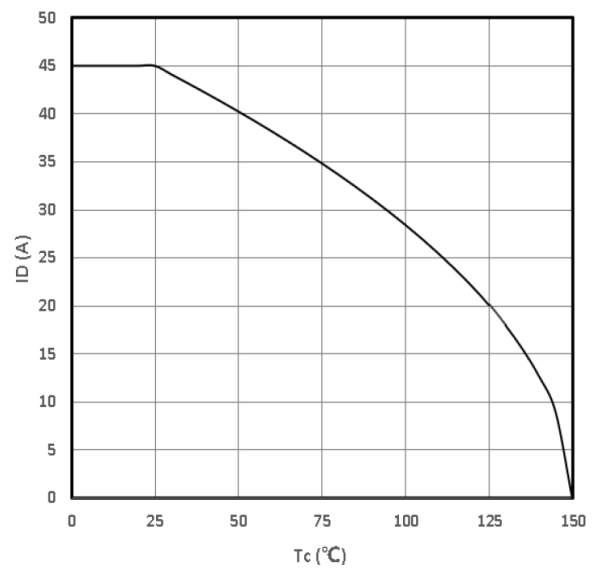


Figure 10: Maximum Drain Current
 $I_D=f(T_c)$

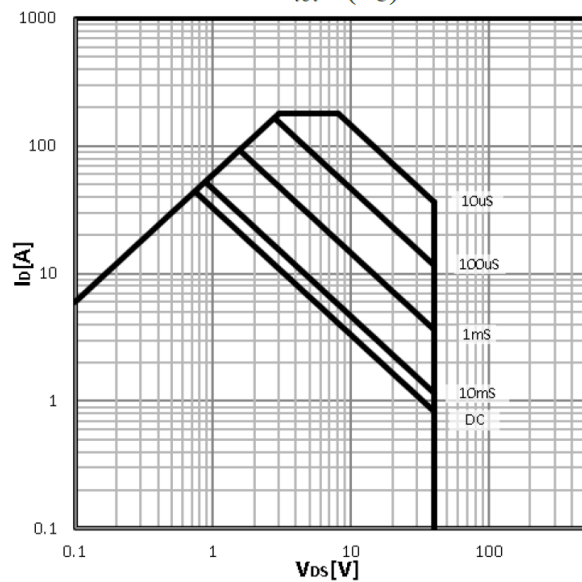


Figure.11: Safe operating area
 $I_D=f(V_{DS})$

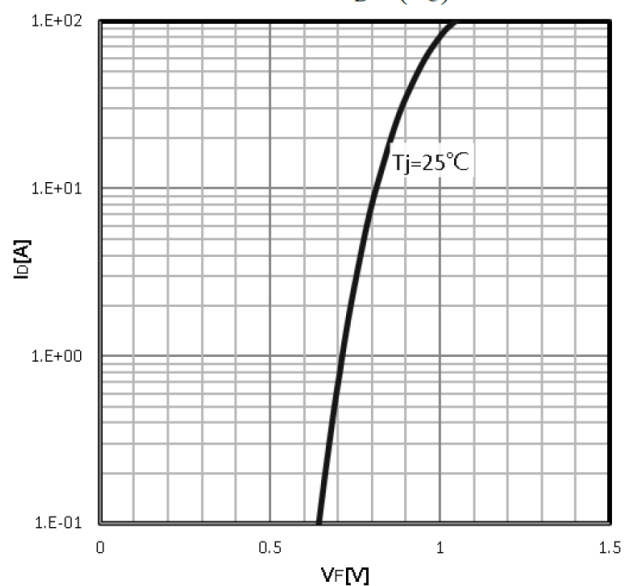
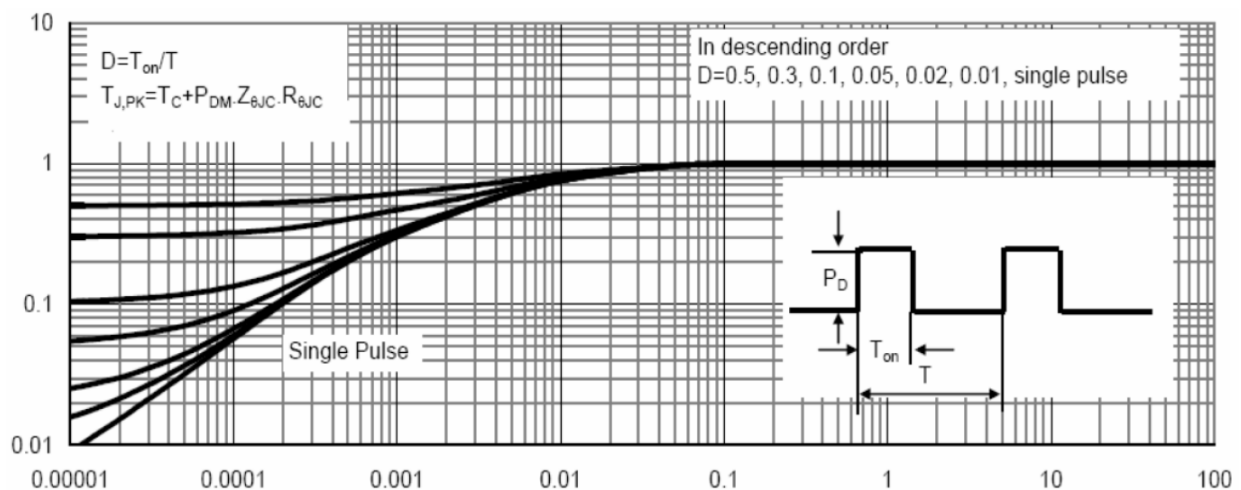


Figure 12 Body Diode Forward Voltage Variation
 $I_F=f(V_{GS})$



Max. transient thermal impedance

$$Z_{thJC}=f(t_p)$$

N-Channel Electrical Characteristics: ($T_C=25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Off Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250 μ A	40	---	---	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{GS} =0V, V _{DS} =40V	---	---	-1	μ A
I _{GSS}	Gate-Source Leakage Current	V _{GS} =± 20V, V _{DS} =0A	---	---	± 100	nA
On Characteristics						
V _{GS(th)}	Gate-Source Threshold Voltage	V _{GS} =V _{DS} , I _D =250 μ A	1	1.5	2	V
R _{DS(on)}	Drain-Source On Resistance ⁴	V _{GS} =10V, I _D =20A	---	4.5	5.5	m Ω
		V _{GS} =4.5V, I _D =10A	---	6.8	8	
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} =20V, V _{GS} =0V, f=1MHz	---	997.5	---	pF
C _{oss}	Output Capacitance		---	580	---	
C _{rss}	Reverse Transfer Capacitance		---	32	---	
Switching Characteristics						
t _{d(on)}	Turn-On Delay Time	V _{DD} = 20V, I _D =-50A V _{GS} = 10V, R _{GEN} =3 Ω	---	6.5	---	ns
t _r	Rise Time		---	2.7	---	ns
t _{d(off)}	Turn-Off Delay Time		---	27	---	ns
t _f	Fall Time		---	3.6	---	ns
Q _g	Total Gate Charge	V _{GS} =10V, V _{DS} =20V, I _D =50A	---	17	---	nC
Q _{gs}	Gate-Source Charge		---	4.5	---	nC
Q _{gd}	Gate-Drain “Miller” Charge		---	2	---	nC
Drain-Source Diode Characteristics						
I _S	Continuous Drain to Source Diode	V _D =V _G =0V	---	---	60	A
I _{SM}	Pulsed Drain to Source Diode		---	---	240	---
V _{SD}	Source-Drain Diode Forward Voltage	V _{GS} =0V, I _S =1A	---	---	1.2	V

Notes:

1. Computed continuous current assumes the condition of $T_{j,Max}$ while the actual continuous current depends on the thermal & electro-mechanical application board design
2. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
3. EAS condition : $T_J=25^{\circ}C$, $V_{DD}=20V$, $V_G=10V$, $L=0.5mH$
4. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 0.5\%$

N-Typical Characteristics: ($T_C=25^{\circ}C$ unless otherwise noted)

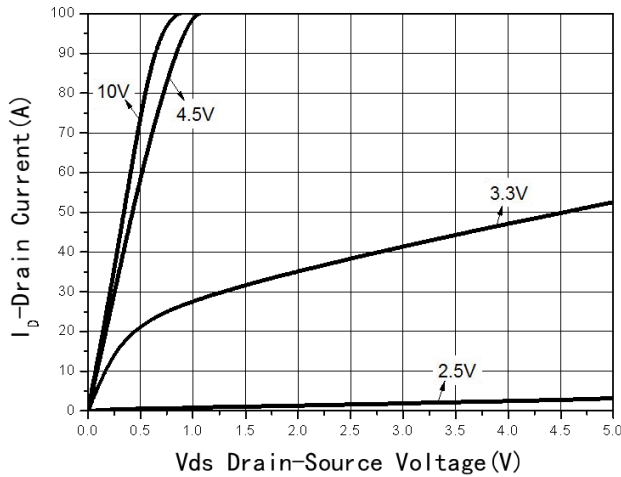


Fig1 Output Characteristics

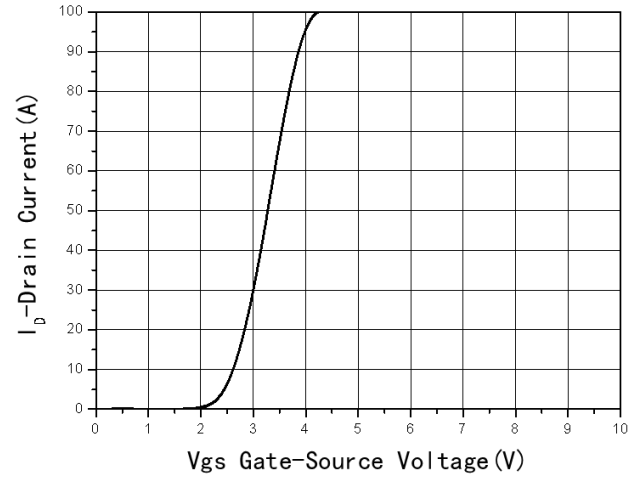


Fig2 Transfer Characteristics

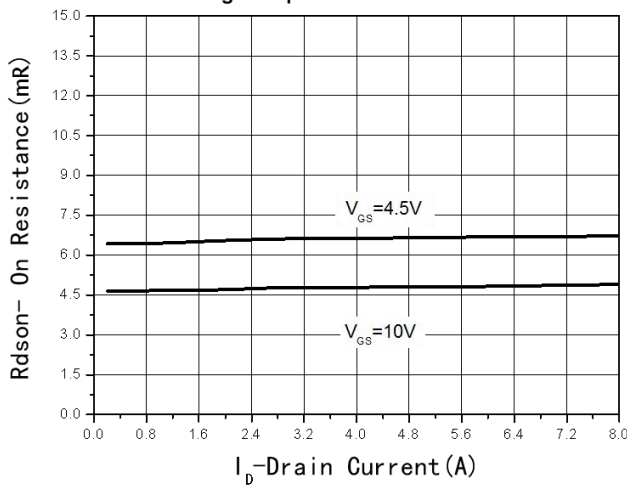


Fig3 $R_{DS(on)}$ -Drain current

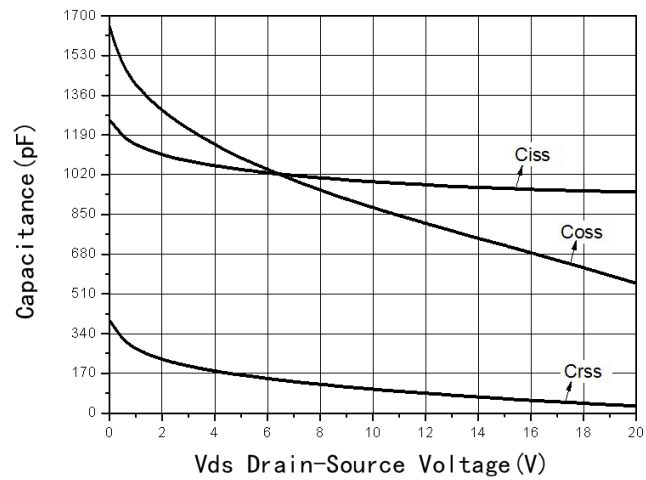


Fig4 Capacitance vs V_{DS}

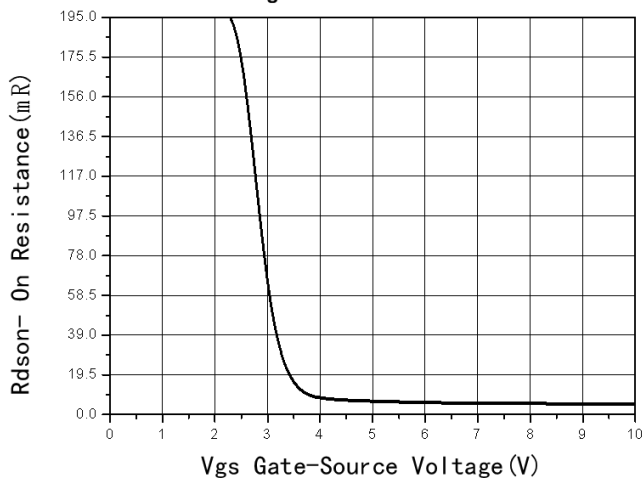


Fig5 $R_{DS(on)}$ -Gate Drain voltage

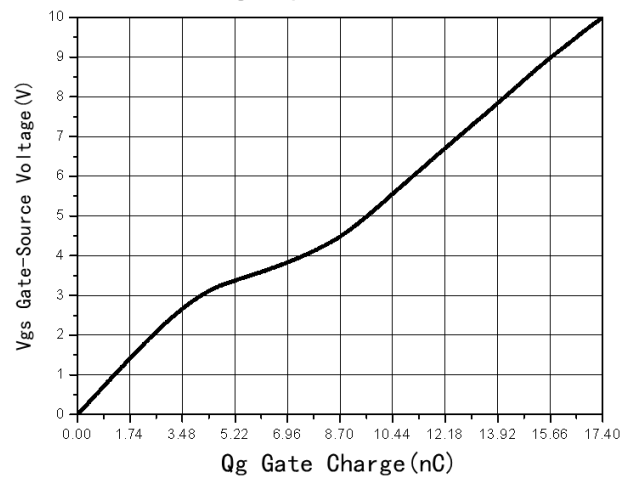


Fig6 Gate Charge

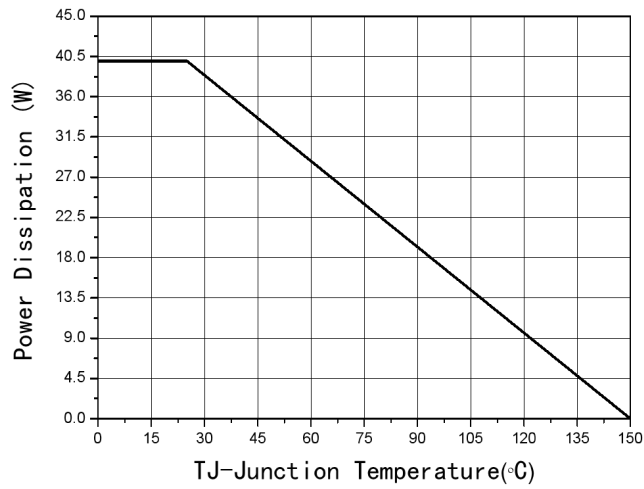


Fig7 Power De-rating

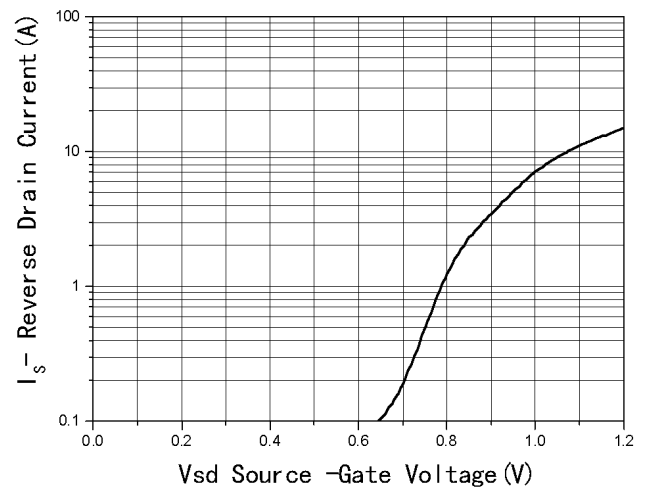
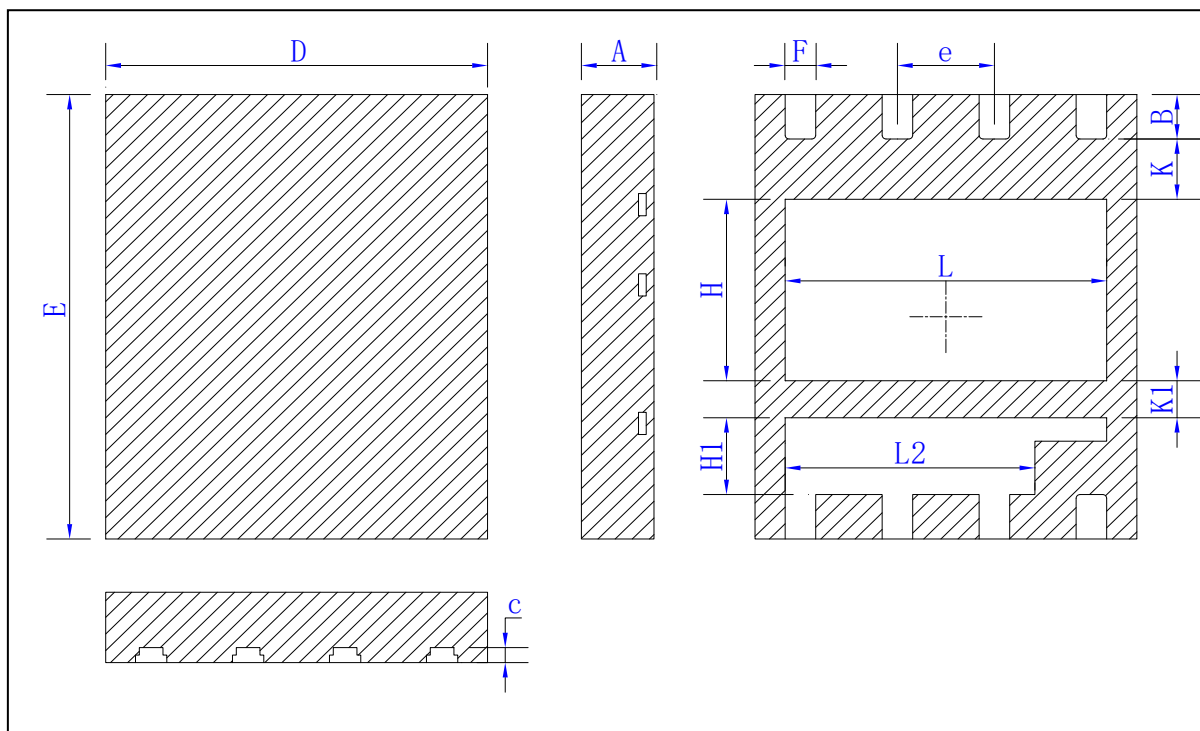


Fig8 Source-Drain Diode Forward

TDFN5×6 Asym Package Information:



UNIT: mm

Symbol	Min	Typ	Max
A	0.90	0.95	1.00
B	0.50	0.60	0.70
C	0.153	0.203	0.253
D	4.90	5.00	5.10
E	5.90	6.00	6.10
e	1.22	1.27	1.32
F	0.35	0.40	0.45
H	2.35	2.45	2.55
H1	0.93	1.03	1.13
L	4.06	4.21	4.36
L2	3.07	3.22	3.37
K	7	0.80	0.90
K1	0.40	0.50	0.60

Marking Information:

①. Doingter LOGO

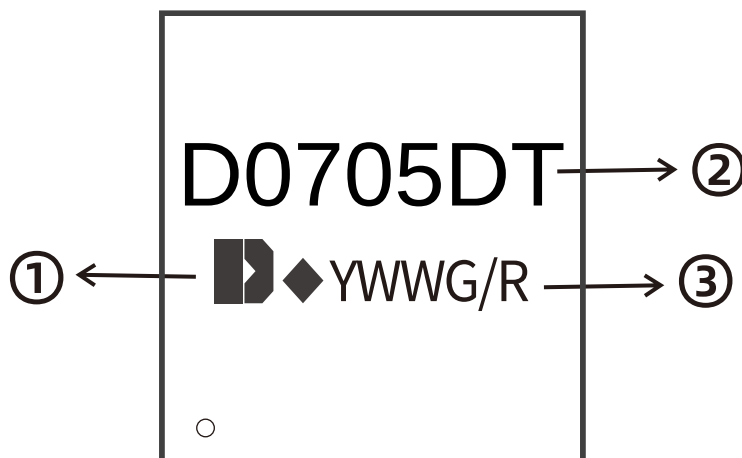
②. Part NO.

③. Date Code(YWWG / R)

Y : Year Code , last digit of the year

WW : Week Code(01-53)

G/R : G(Green) /R(Lead Free)

**Previous Version**

Version	Date	Subjects (major changes since last revision)
1.0	2025-04-13	Release of final version

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