

74AHCT1G00 Series

2-INPUT NAND GATE

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Features

- Operation Voltage Range:4.5~5.5V
- Low Power Dissipation
- High noise immunity
- Input compatible with TTL voltage
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

General Description

The 74AHCT1G00 is a 2-input NAND gate which provides the function $Y = \overline{A \cdot B}$.

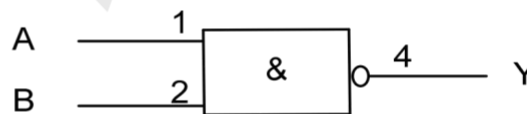
Applications

- IP Phones
- Notebook PCs
- Printers
- Solar Inverters
- DLP positive projection system
- Access Control and Security

Logic Diagram



Logic symbol

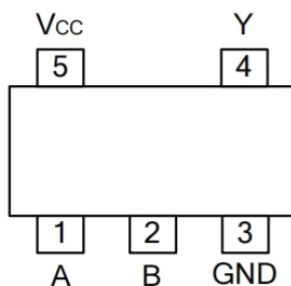


IEC logic symbol

Ordering Information

ORDER NUMBER	PACKAGE DESCRIPTION	PACKAGE OPTION
74AHCT1G00GV-TP	SOT23-5	Tape and Reel,3000
74AHCT1G00GW-TP	SOT353	Tape and Reel,3000

Pin Configuratio



SOT23-5 / SOT353

Function Table

INPUT		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

Note: H: HIGH voltage level; L: LOW voltage level.

ABSOLUTE MAXIMUM RATINGS ($T_A=25^{\circ}\text{C}$, unless otherwise specified) (Note 2)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	VCC	-0.5 ~ 7	V
Input Voltage	VIN	-0.5 ~ 7	V
Output Voltage	VOUT	-0.5 ~ VCC+0.5	V
Input Clamp Current	I _{IK}	±20	mA
Output Clamp Current	I _{OK}	±20	mA
Output Current	I _{OUT}	±25	mA
VCC or GND Current	I _{CC}	±50	mA
Storage Temperature	T _{STG}	-65 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V _{CC}		4.5	--	5.5	V
Input Voltage	V _{IN}		0	--	5.5	V
Output Voltage	V _{OUT}		0	--	V _{CC}	V
Input Transition Rise or Fall Rate	$\Delta t/\Delta v$	V _{CC} =5.0+0.5V	--	--	20	ns/V
Operating Temperature	T _A		-40	--	+125	°C

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ELECTRICAL CHARACTERISTICS ($T_A=25^\circ\text{C}$, unless otherwise specified)

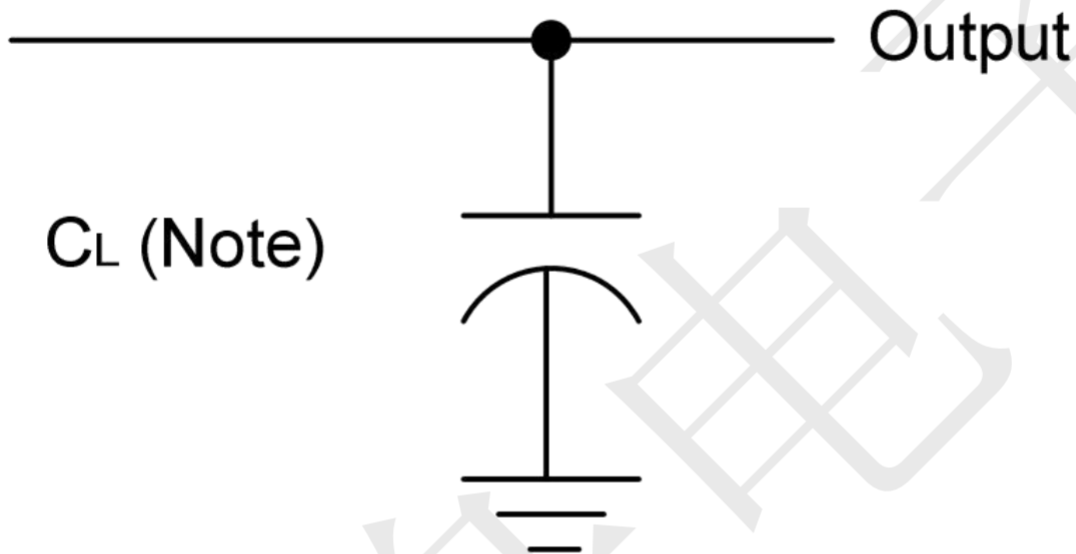
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-Level Input Voltage	V_{IH}	$V_{CC}=4.5\text{V}\sim 5.5\text{V}$	2.0	--	--	V
Low-Level Input Voltage	V_{IL}	$V_{CC}=4.5\text{V}\sim 5.5\text{V}$	--	--	0.8	V
High-Level Output Voltage	V_{OH}	$V_{CC}=4.5\text{V}, I_{OH}=-50\mu\text{A}$	4.4	4.5	--	V
		$V_{CC}=4.5\text{V}, I_{OH}=-8\text{mA}$	3.94	--	--	
Low-Level Output Voltage	V_{OL}	$V_{CC}=4.5\text{V}, I_{OL}=50\mu\text{A}$	--	--	0.1	V
		$V_{CC}=4.5\text{V}, I_{OL}=8\text{mA}$	--	--	0.36	
Input Leakage Current	$I_{I(LEAK)}$	$V_{CC}=5.5\text{V}, V_{IN}=V_{CC}$ or GND	--	--	± 0.1	μA
Quiescent Supply Current	I_Q	$V_{CC}=5.5\text{V}, V_{IN}=V_{CC}$ or GND $I_{OUT}=0$	--	--	1	μA
Additional Quiescent Supply Current	ΔI_Q	$V_{CC}=5.5\text{V}, V_{IN}=3.4\text{V}; I_{OUT}=0$; other input at V_{CC} or GND	--	--	1.35	mA
Input Capacitance	C_{IN}	$V_{IN}=V_{CC}$ or GND	--	2	10	pF
Power Dissipation Capacitance	C_{PD}	$f=1\text{MHz}$, No load	--	10.5	--	pF

DYNAMIC CHARACTERISTICS

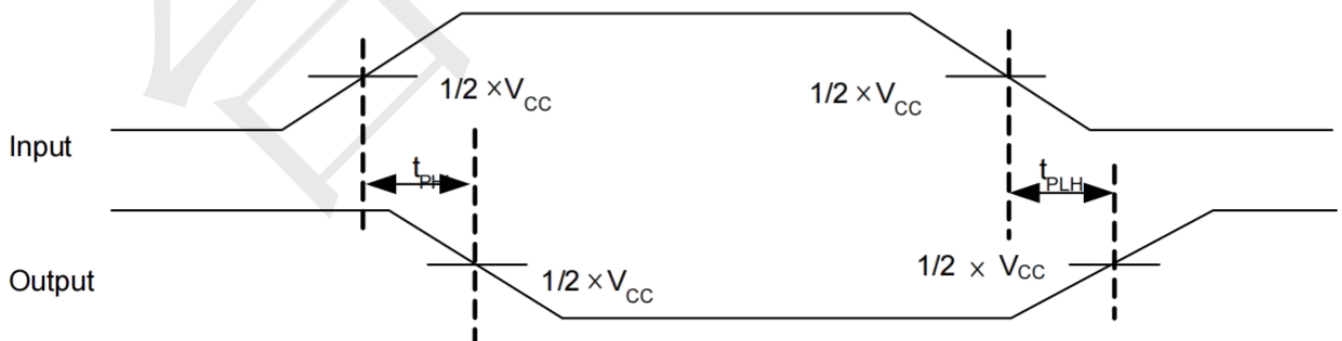
($t_R, t_F \leq 3\text{ns}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay From Input (A and B) to Output(Y)	t_{PLH}	$V_{CC}=5\text{V} \pm 0.5\text{V}, C_L=15\text{pF}$	--	5	6.9	ns
	t_{PHL}		--	5	6.9	ns
	t_{PLH}	$V_{CC}=5\text{V} \pm 0.5\text{V}, C_L=50\text{pF}$	--	5.5	7.9	ns
	t_{PHL}		--	5.5	7.9	ns

TEST CIRCUIT AND WAVEFORMS

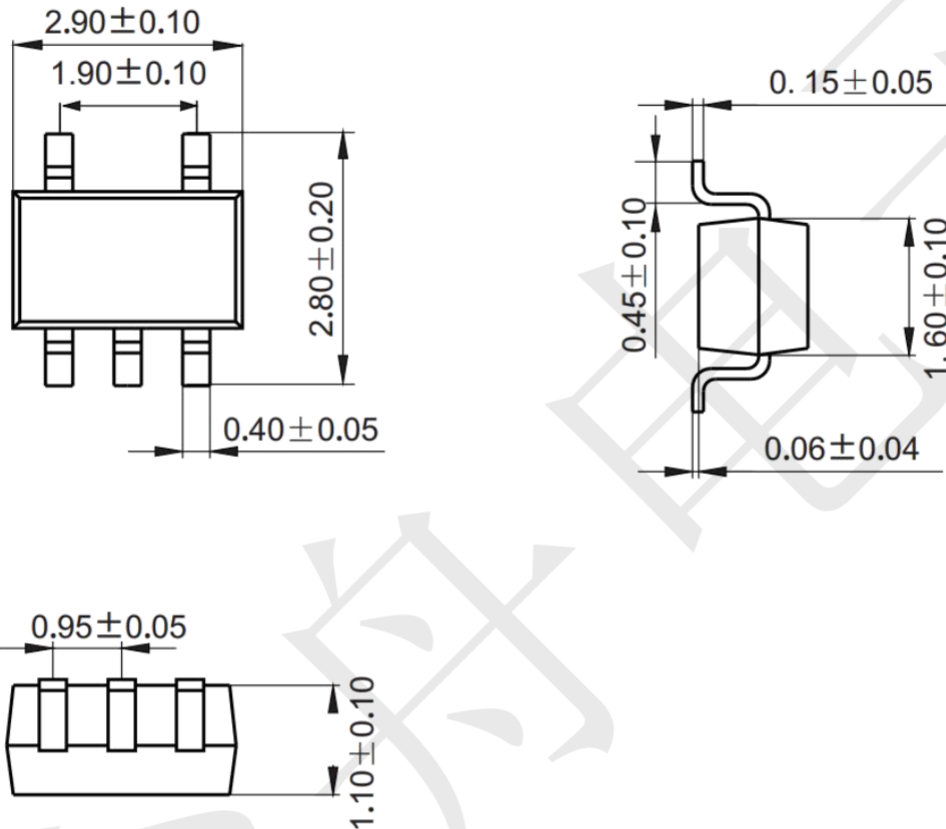


Note: C_L includes probe and jig capacitance.

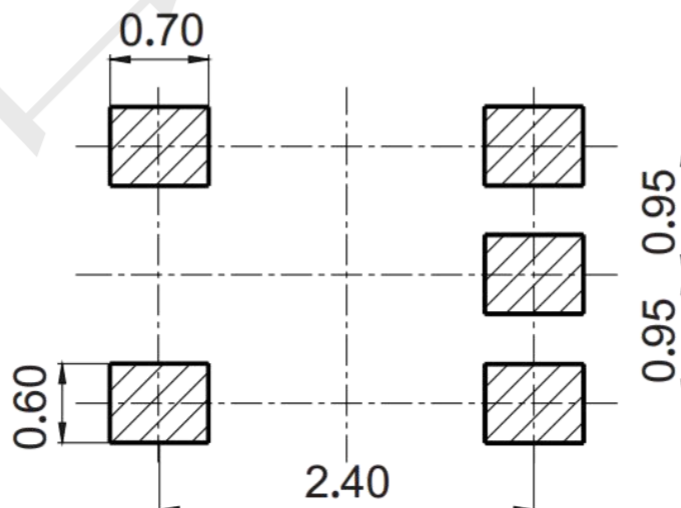


Package information (Unit: mm)

SOT23-5

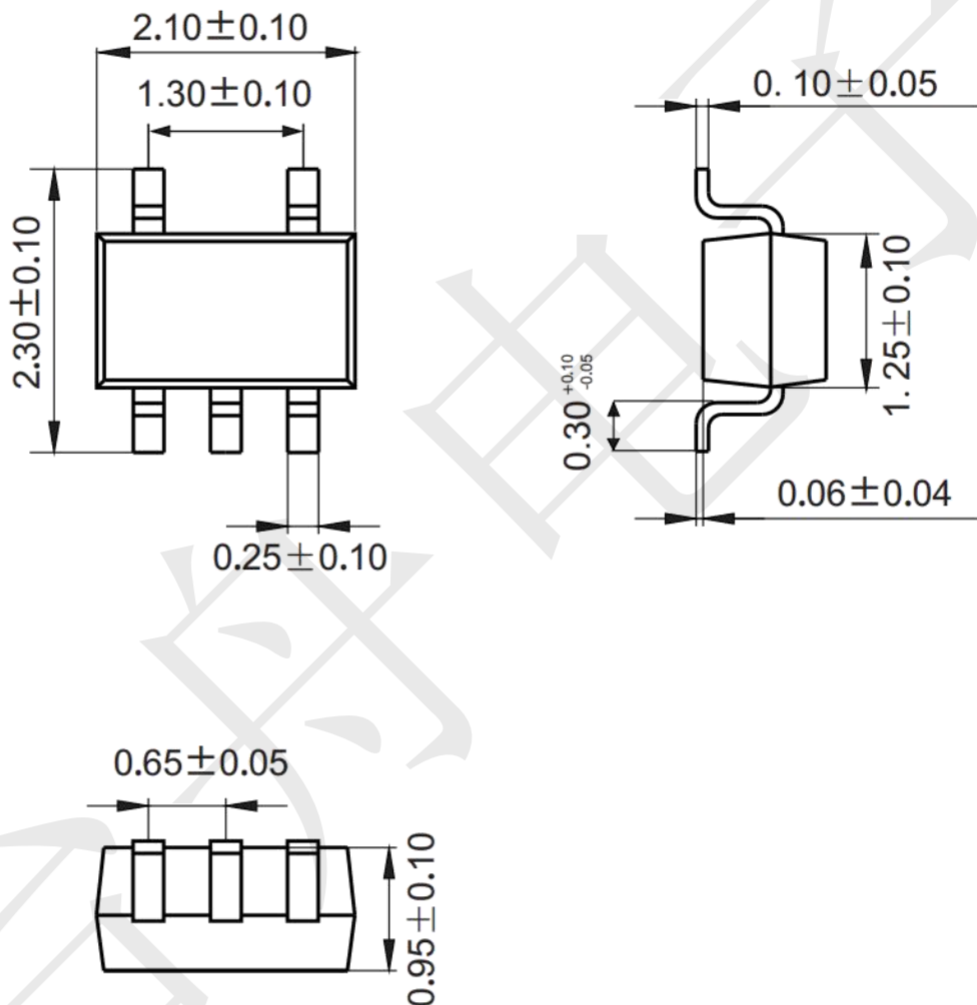


Mounting Pad Layout (Unit: mm)



Package information

SOT353 (Unit: mm)



Mounting Pad Layout (unit: mm)

