

Silicon N-Channel Power MOSFET

Description

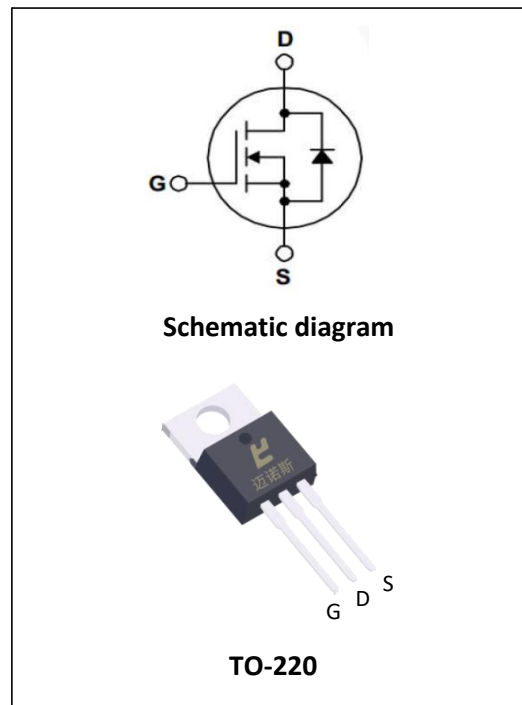
MPT042N10P, the N-channel Enhanced Power MOSFETs, is obtained by advanced double trench technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. This is suitable device for motor drivers and high speed switching applications.

General Features

- ① $V_{DS}=100V$, $R_{ds(on)} < 3.8m\Omega$ @ $V_{GS}=10V$ (Typ: $3.4m\Omega$)
- ② Fast Switching
- ③ Low On-Resistance
- ④ Low Gate Charge
- ⑤ Low Reverse transfer capacitance
- ⑥ High avalanche ruggedness
- ⑦ RoHS product

Application

- ① Motor drivers
- ② Switching applications



Package Marking And Ordering Information:

Ordering Codes	Package	Product Code	Packing
MPT042N10-P	TO-220	MPT042N10P	Tube

Absolute Maximum Ratings (at $T_C = 25^\circ C$, unless otherwise specified)

Symbol	Parameter	Value	Units
V_{DSS}	Drain-to-Source Voltage	100	V
I_D	Continuous Drain Current, Silicon Limited	180	A
	Continuous Drain Current, Package Limited	120	A
	Continuous Drain Current $T_C = 100^\circ C$, Silicon Limited	128	A
I_{DM}	Pulsed Drain Current (Note1)	720	A
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Avalanche Energy (Note2)	520	mJ
P_D	Power Dissipation	227.2	W
	Derating Factor above $25^\circ C$	1.82	W/ $^\circ C$
T_J, T_{stg}	Operating Junction and Storage Temperature Range	150, -55 to 150	$^\circ C$
T_L	Maximum Temperature for Soldering	260	$^\circ C$

Note1: Repetitive Rating: Pulse width limited by maximum junction temperature

Note2: $L=0.5mH$, $I_{as}=35A$, Start $T_J=25^\circ C$

Thermal characteristics

Symbol	Parameter	Value	Units
$R_{\theta JC}$	thermal resistance,Junction-to-Case	0.55	$^{\circ}\text{C}/\text{W}$
$R_{\theta JA}$	thermal resistance,Junction-to-Ambient	62.5	$^{\circ}\text{C}/\text{W}$

Electrical Characteristics (at $T_c = 25^{\circ}\text{C}$, unless otherwise specified)

OFF Characteristics						
Symbol	Parameter	Test Conditions	Values			Units
			Min.	Typ.	Max.	
V_{DS}	Drain to Source Breakdown Voltage	$V_{GS}=0\text{V}, I_D=250\mu\text{A}$	100	--	--	V
I_{DSS}	Drain to Source Leakage Current	$V_{DS}=100\text{V}, V_{GS}=0\text{V}, T_j=25^{\circ}\text{C}$	--	--	1	μA
		$V_{DS}=80\text{V}, V_{GS}=0\text{V}, T_j=125^{\circ}\text{C}$	--	--	100	μA
$I_{GSS(F)}$	Gate to Source Forward Leakage	$V_{GS}=+20\text{V}$	--	--	100	nA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	$V_{GS}=-20\text{V}$	--	--	-100	nA

ON Characteristics						
Symbol	Parameter	Test Conditions	Values			Units
			Min.	Typ.	Max.	
$R_{DS(ON)}$	Drain-to-Source On- Resistance	$V_{GS}=10\text{V}, I_D=50\text{A}(\text{Note4})$	--	3.4	3.8	m Ω
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu\text{A}(\text{Note4})$	2.0	3.0	4.0	V
Pulse width $t_p \leq 300\mu\text{s}, \delta \leq 2\%$						

Dynamic Characteristics						
Symbol	Parameter	Test Conditions	Values			Units
			Min.	Typ.	Max.	
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}$ $V_{DS}=50\text{V}$ $f=1.0\text{MHz}$	--	7102	--	PF
C_{oss}	Output Capacitance		--	2584	--	
C_{rss}	Reverse Transfer Capacitance		--	174	--	
Q_g	Total Gate Charge	$I_D=50\text{A}$ $V_{DD}=50\text{V}$ $V_{GS}=10\text{V}$	--	102	--	nC
Q_{gs}	Gate to Source Charge		--	30	--	
Q_{gd}	Gate to Drain ("Miller") Charge		--	19.6	--	

Switching Characteristics						
Symbol	Parameter	Test Conditions	Values			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	$V_{DD} = 50V$ $I_D = 50A$ $V_{GS} = 10V$ $R_G = 3\Omega$ Resistive Load	--	29	--	ns
t_r	Rise Time		--	33	--	
$t_{d(OFF)}$	Turn-Off Delay Time		--	48	--	
t_f	Fall Time		--	26	--	

Source-Drain Diode Characteristics						
Symbol	Parameter	Test Conditions	Values			Units
			Min.	Typ.	Max.	
I_S	Continuous Source Current	$T_C = 25^\circ C$	--	--	120	A
I_{SM}	Maximum Pulsed Current		--	--	720	A
V_{SD}	Diode Forward Voltage	$I_S = 50A, V_{GS} = 0V$ (Note4)	--	--	1.2	V
T_{rr}	Reverse Recovery Time	$I_S = 50A,$ $T_j = 25^\circ C$ $dI_F/dt = 100A/\mu s,$ $V_{GS} = 0V$	--	80	--	ns
Q_{rr}	Reverse Recovery Charge		--	189	--	nC

Characteristics Curves

Figure 1. Safe Operating Area

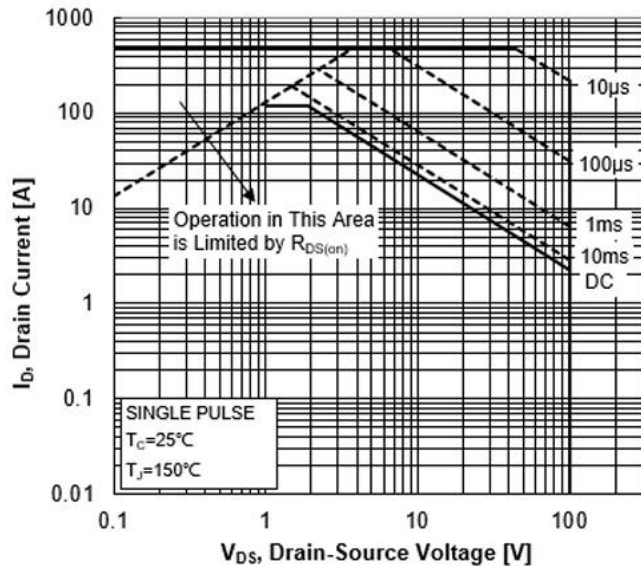


Figure 2. Maximum Power Dissipation vs Case Temperature

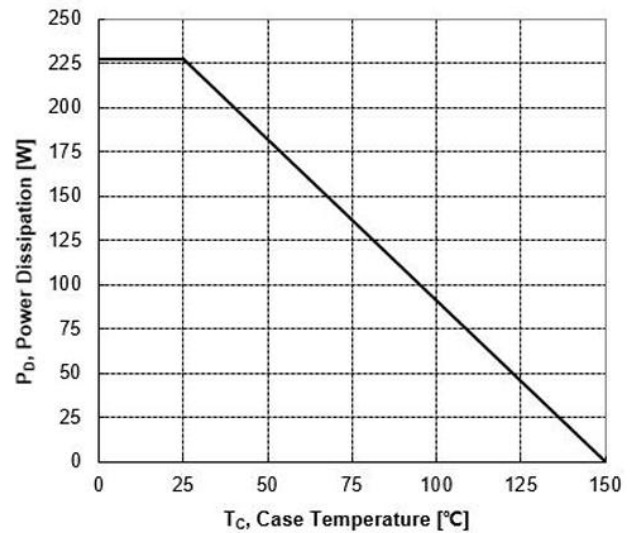


Figure 3. Maximum Continuous Drain Current vs Case Temperature

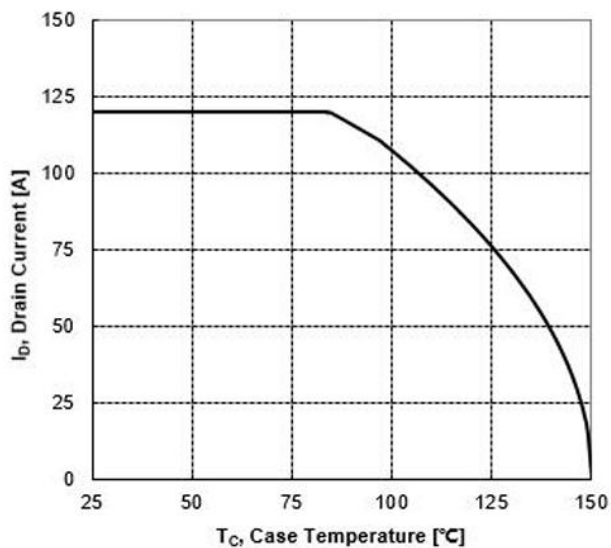


Figure 4. Typical Output Characteristics

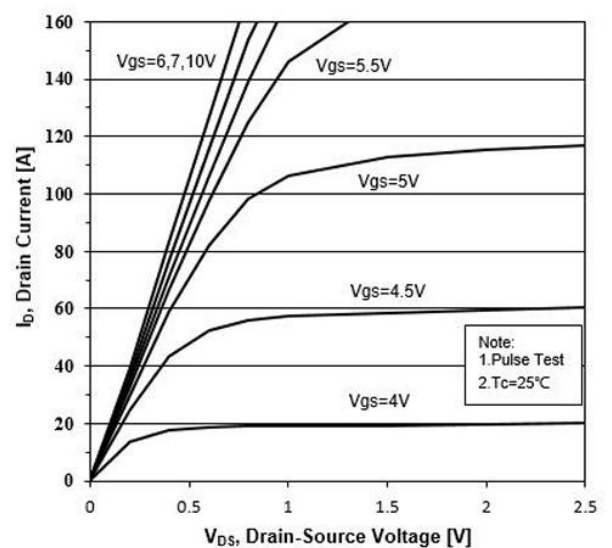


Figure 5. Transient Thermal Impedance

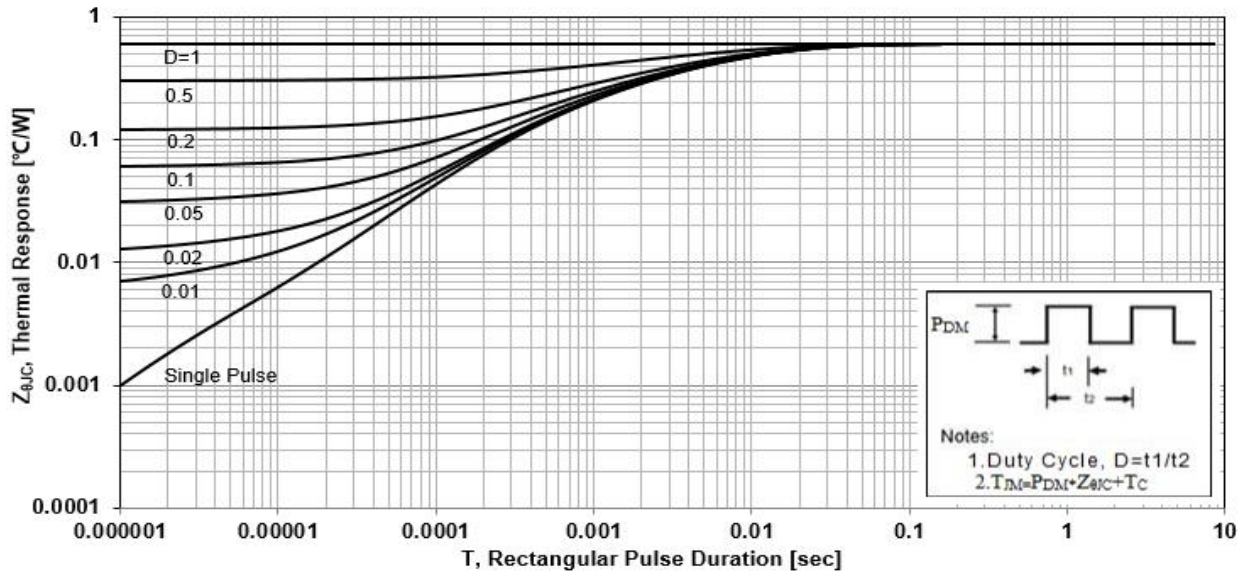


Figure 6. Typical Transfer Characteristics

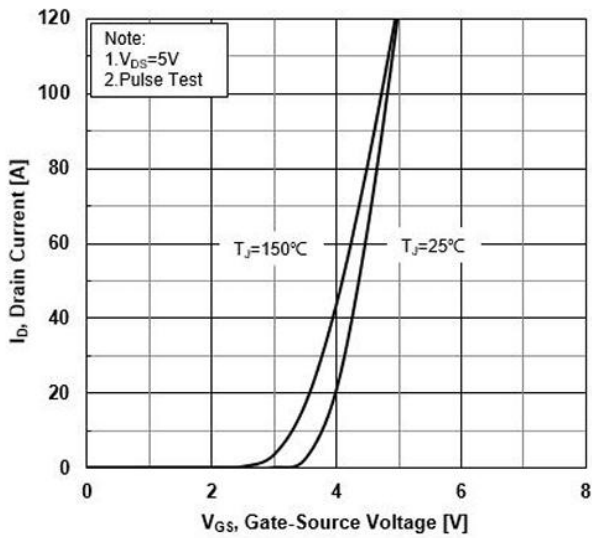


Figure 7. Source-Drain Diode Forward Characteristics

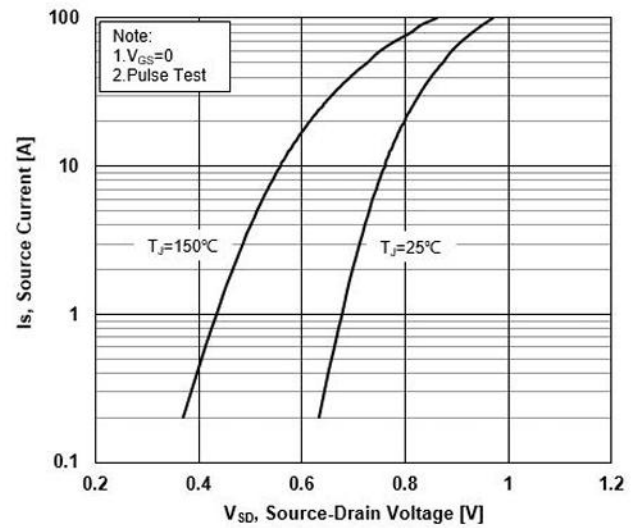


Figure 8. Drain-Source On-Resistance vs Drain Current

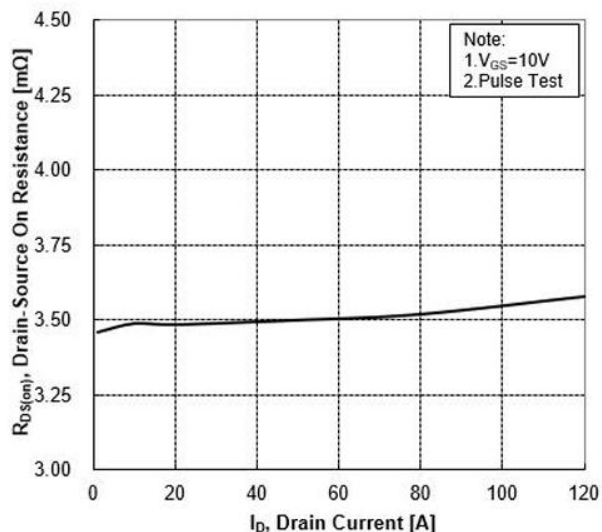


Figure 9. Normalized On-Resistance vs Junction Temperature

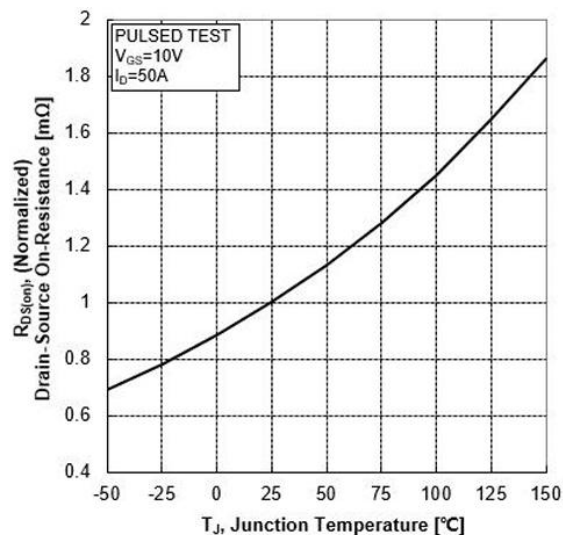


Figure 10. Normalized Threshold Voltage vs Junction Temperature

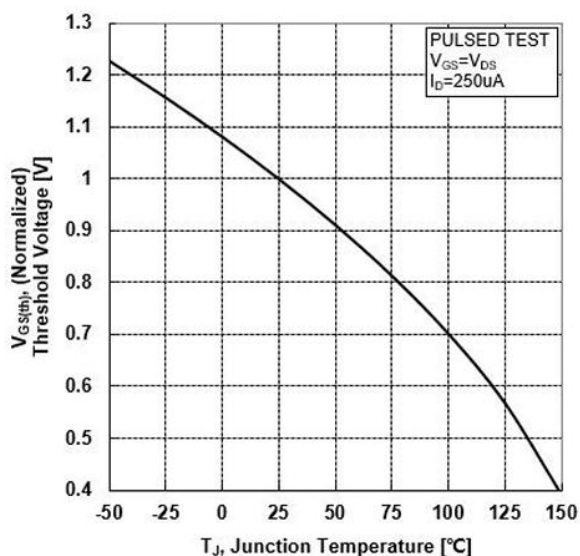


Figure 11. Normalized Breakdown Voltage vs Junction Temperature

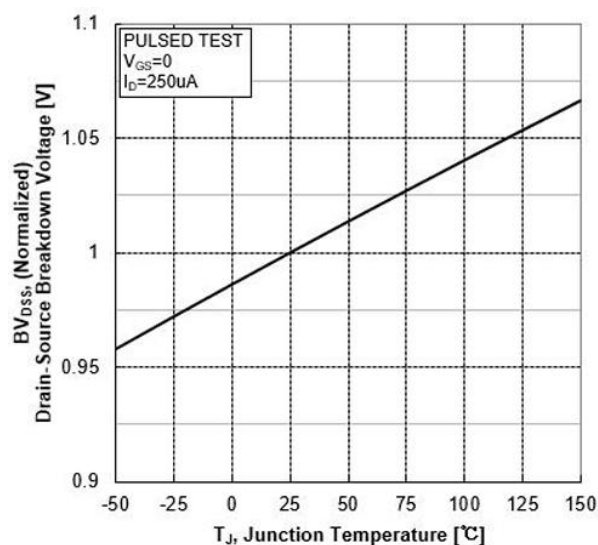


Figure 12. Capacitance Characteristics

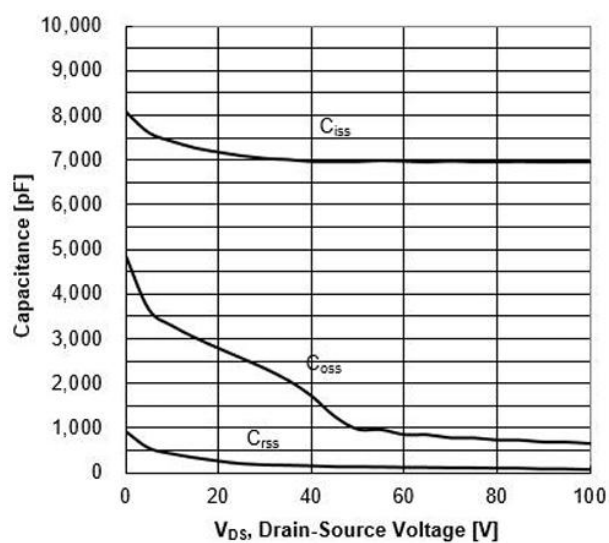
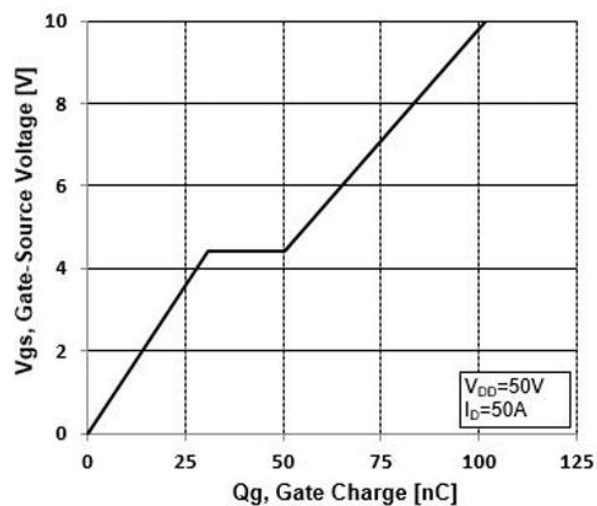
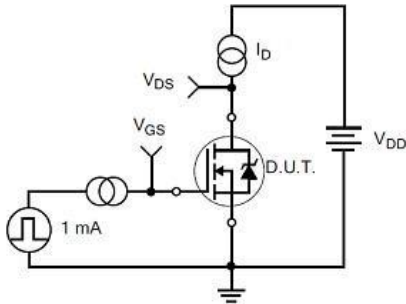
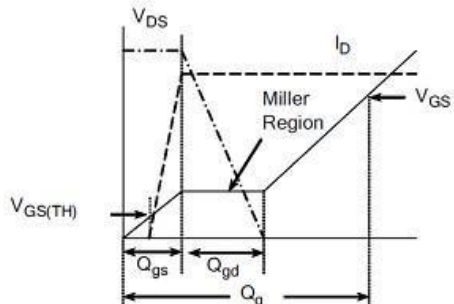
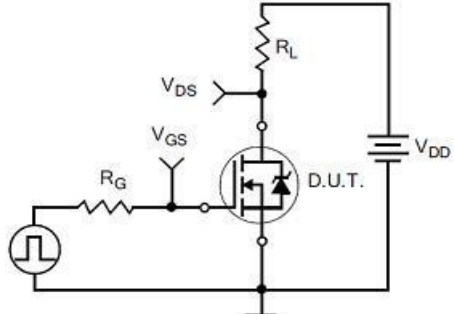
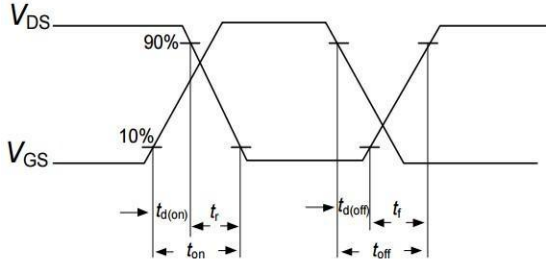
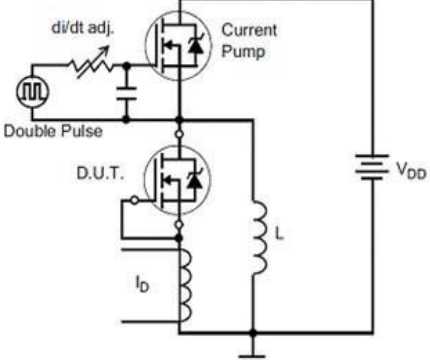
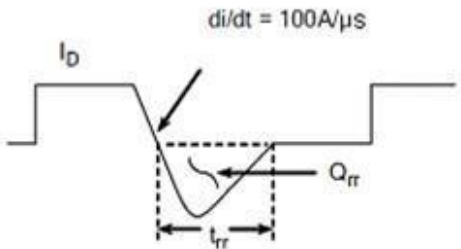
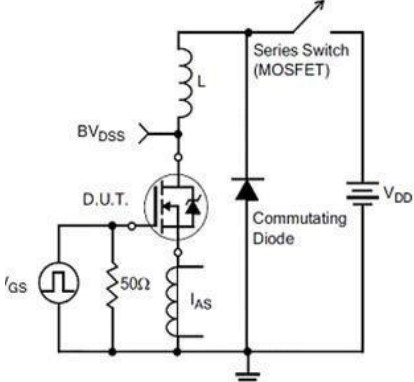
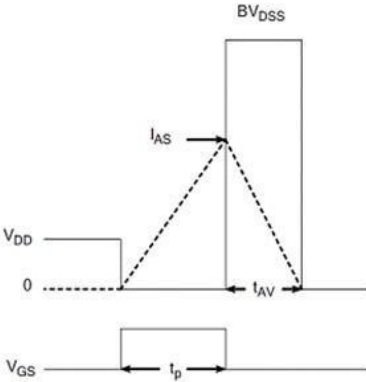


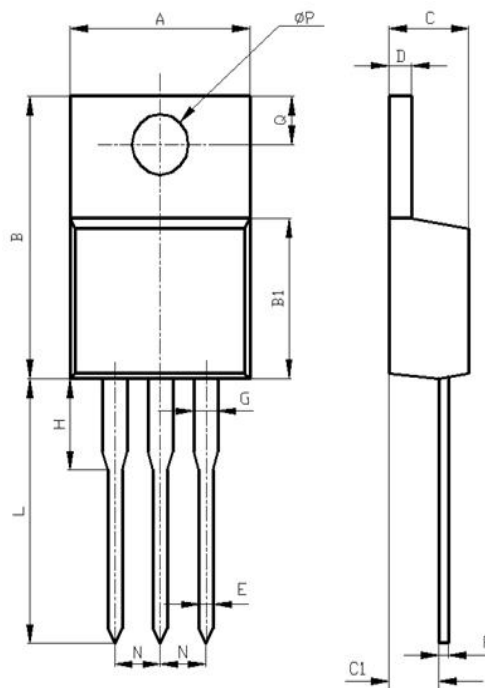
Figure 13. Typical Gate Charge vs Gate-Source Voltage



Test Circuit and Waveform

Gate Charge Test Circuit  The diagram shows a MOSFET (D.U.T.) with its gate connected to a 1 mA current source and its drain connected to a load resistor and a drain current source I_D. The gate voltage is V_{GS} and the drain voltage is V_{DS}. The supply voltage is V_{DD}.	Gate Charge Waveforms  The diagram shows the relationship between V_{DS}, I_D, and V_{GS} during a switching event. It identifies the Miller Region, the threshold voltage $V_{GS(TH)}$, and the gate charges Q_{gs}, Q_{gd}, and Q_g.
Resistive Switching Test Circuit  The diagram shows a MOSFET (D.U.T.) with its gate connected to a current source and its drain connected to a load resistor R_L. The gate voltage is V_{GS} and the drain voltage is V_{DS}. The supply voltage is V_{DD} and the gate resistor is R_G.	Resistive Switching Waveforms  The diagram shows the switching waveforms for V_{DS} and V_{GS}. It indicates the 90% and 10% voltage levels and the time intervals $t_{d(on)}$, t_r, $t_{d(off)}$, and t_{off}.
Diode Reverse Recovery Test Circuit  The diagram shows a MOSFET (D.U.T.) with its gate connected to a current source and its drain connected to a diode and an inductor L. The gate voltage is V_{GS} and the drain voltage is V_{DS}. The supply voltage is V_{DD}. A current pump and a double pulse source are used to control the diode current I_D.	Diode Reverse Recovery Waveform  The diagram shows the reverse recovery current I_D and the reverse recovery charge Q_{rr} during the reverse recovery process. The di/dt is specified as 100A/μs.
Unclamped Inductive Switching Test Circuit  The diagram shows a MOSFET (D.U.T.) with its gate connected to a current source and its drain connected to an inductor L and a series switch (MOSFET). The gate voltage is V_{GS} and the drain voltage is V_{DS}. The supply voltage is V_{DD}. A commutating diode and a 50Ω resistor are also shown.	Unclamped Inductive Switching Waveform  The diagram shows the switching waveforms for V_{DS} and V_{GS}. It indicates the peak drain-source voltage BV_{DSS}, the average current I_{AS}, and the pulse width t_p.

Package Description



Symbol	Values(mm)	
	MIN	MAX
A	9.60	10.6
B	15.0	16.0
B1	8.90	9.50
C	4.30	4.80
C1	2.30	3.10
D	1.20	1.40
E	0.70	0.90
F	0.30	0.60
G	1.17	1.37
H	2.70	3.80
L	12.6	14.8
N	2.34	2.74
Q	2.40	3.00
Ø P	3.50	3.90

TO-220 Package

NOTE:

1. Exceeding the maximum ratings of the device in performance may cause damage to the device, even the permanent failure, which may affect the dependability of the machine. Please do not exceed the absolute maximum ratings of the device when circuit designing.
2. When installing the heat sink, please pay attention to the torsional moment and the smoothness of the heat sink.
3. MOSFETs is the device which is sensitive to the static electricity, it is necessary to protect the device from being damaged by the static electricity when using it.
4. Shenzhen Minos reserves the right to make changes in this specification sheet and is subject to change without prior notice.

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