钍地半导体
Tudi Semiconductor

Product Specification

TUDI-MC3486

Quad differential line receiver with tri-state outputs

网址 www.sztdbdt.com

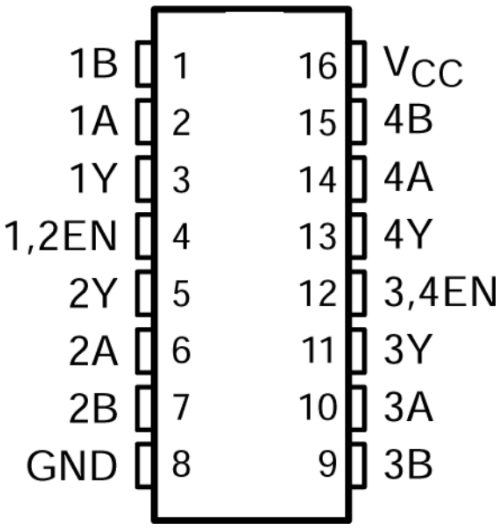
用芯智造·卓越品质

semiconductor device manufacturer

- Design
- research and development
- production
- and sales

Features

- Meets or exceeds the requirements of ANSI standards EIA/TIA-422-B and EIA/TIA-423-B, and ITU recommendations.10 and V.11
- Tri-state TTL compatible outputs
- Fast transition times
- Powered by a single 5V supply



MC3486

Applications

- Motor drives
- Factory automation and control

Description

The MC3486 is a monolithic quad differential line receiver that meets the requirements of ANSI standards TIA/EIA-422- and TIA/EIA-423-B, as well as ITU recommendations V.10 and V.11. The MC3486 provides four differential input line receivers with TTL-compatible outputs. When the appropriate output enable is at a logic low level, the outputs can provide a high-impedance state at any output pin using-state circuitry.
The MC3486 achieves excellent performance when used in conjunction with the MC3487 quad differential line driver. The device is housed in a16-pin package and is powered by a single 5V supply. The rated operating temperature range of the MC3486 is 0°C to 70°C.

Ordering information

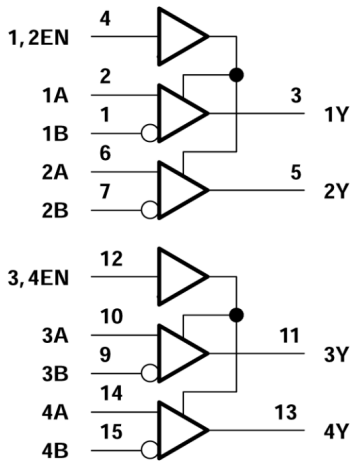
Order Number	Package	Package Quantity	Marking On The park	Temperature
MC3486DR-TUDI	SOP16	Tape,Reel,2500	MC3486	0℃ to 70℃
MC3486N-TUDI	DIP16	Tube,25,A box of 2000	MC3486N	

Pin Configuration and Functions

Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
1B	1	I	Channel 1 Differential Receiver Inverting Input
1A	2	I	Channel 1 Differential Receiver Non-Inverting Input
1Y	3	O	Channel 1 Single Ended Output
1,2 EN	4	I	Active High Enable for Channels 1 and 2
2Y	5	O	Channel 2 Single Ended Output
2A	6	I	Channel 2 Differential Receiver Non-Inverting Input
2B	7	I	Channel 2 Differential Receiver Inverting Input
GND	8	GND	Device GND
3B	9	I	Channel 3 Differential Receiver Inverting Input
3A	10	I	Channel 3 Differential Receiver Non-Inverting Input
3Y	11	O	Channel 3 Single Ended Output
3,4 EN	12	I	Active High Enable for Channels 3 and 4
4Y	13	O	Channel 4 Single Ended Output
4A	14	I	Channel 4 Differential Receiver Non-Inverting Input
4B	15	I	Channel 4 Differential Receiver Inverting Input
Vcc	16	PWR	Device VCC(4.75V to 5.25V)

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.



Logic Diagram (Positive Logic)

Specifications

Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
VI	Input voltage(A or B inputs)		±15	V
ViD(see)	Differential input voltage		±25	V
	Enable input voltage		8	V
IoL	Low-level output current		50	mA
	Lead temperature 1,6 mm(1/16 inch) from case for 10seconds		260	℃
Tstg	Storage temperature range	-65	150	℃

(1) Stresses beyond those listed under “ absolute maximum ratings ” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “ recommended operating conditions ” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.

Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.75	5	5.25	V
VIc	Common-mode input voltage			±7	V
VID	Differential input voltage			±6	V
VIH	High-level enable input voltage	2			V
VIL	Low-level enable input voltage			0.8	V
TA	Operating free-air temperature	0		70	℃

Thermal Resistance Characteristics

THERMAL METRIC		D (SOIC)	N(PDIP)	NS (SOP)	UNIT
		16-PINS			
R θJA	Junction-to-ambient thermal resistance	84.6	60.6	88.5	°C/W
RθJC(top)	Junction-to-case (top)thermal resistance	43.5	48.1	46.2	°C/W
R θJB	Junction-to-board thermal resistance	43.2	40.6	50.7	°C/W
ψ JT	Junction-to-top characterization parameter	10.4	27.5	13.5	°C/W
ψ JB	Junction-to-board characterization parameter	42.8	40.3	50.3	°C/W
R θJC(bot)	Junction-to-case (bottom)thermal resistance	n/a	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC package thermal metrics application report.

Switching Characteristics

V_{CC} = 5 V, C_L = 15 pF, T_A = 25 ° C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
tPHL	Propagation delay time,high-to low-level output	See Figure 2		28	35	ns
tpLH	Propagation delay time,low-to high-level output			27	30	ns
tpZH	Output enable time to high level	See Figure 3		13	30	ns
tpzL	Output enable time to low level			20	30	ns
tPHZ	Output disable time from high level			26	35	ns
tpLZ	Output disable time from low level			27	35	ns

Electrical Characteristics

over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
VIT+	Differential input high-threshold voltage	Vo=2.7 V,	Io=-0.4 mA			0.2	V
VIT -	Differential input low-threshold voltage	Vo=0.5V,	Io=-8mA		-0.2		V
VIK	Enable-input clamp voltage	II=-10 mA				-1.5	V
VoH	High-level output voltage	VID=0.4V, SeeNote 4and Fig 1	Io=-0.4 mA,				V
VoL	Low-level output voltage	VID=-0.4V, SeeNote 4 and Fig 1	Io=8 mA,		2.7		V
Ioz	High-impedance-state output current	VIL=0.8V,	VID=-3V,	Vo=2.7V		40	μA
		VL=0.8V,	VID=3V,	Vo=0.5V		-40	
IIB	Differential-input bias current	Vcc=0Vor 2.25V,Other inputs at 0V		VI=-10V		-3.25	mA
				VI=-3V		-1.5	
				VI =3V		1.5	
				VI=10V		3.25	
IIH	High-level enable input current	VI=2.25V				100	μA
		VI=2.7V				20	
IIL	Low-level enable input current	VI=-0.5V				-100	μA
Ios	Short-circuit output current	VID=3v,	Vo=0,	See Note 5	-15	-100	mA
Icc	Supply current	VIL=0				85	mA

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum, is used in this data sheet for threshold voltages only.
(2) Refer to ANSI Standards TIA/EIA-422-B and TIA/EIA-423-B for exact conditions.
(3) Only one output should be shorted at a time.

Parameter Measurement Information

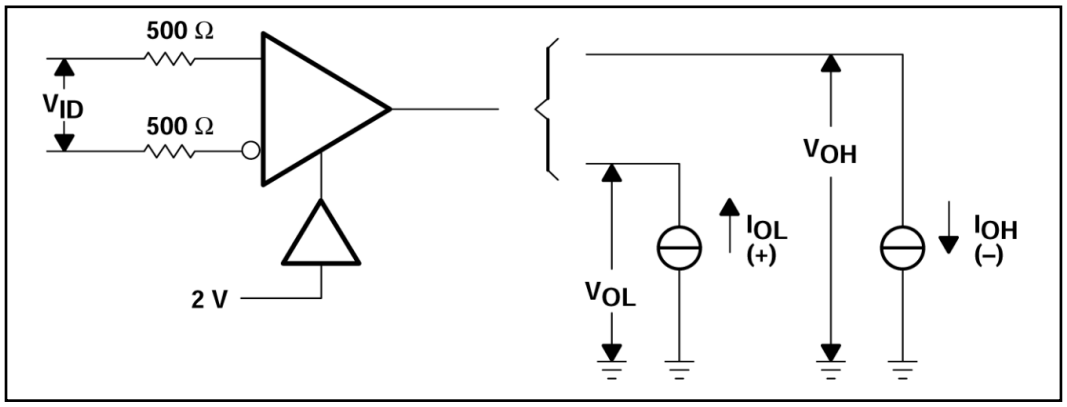


Fig 1. V OH , VOL

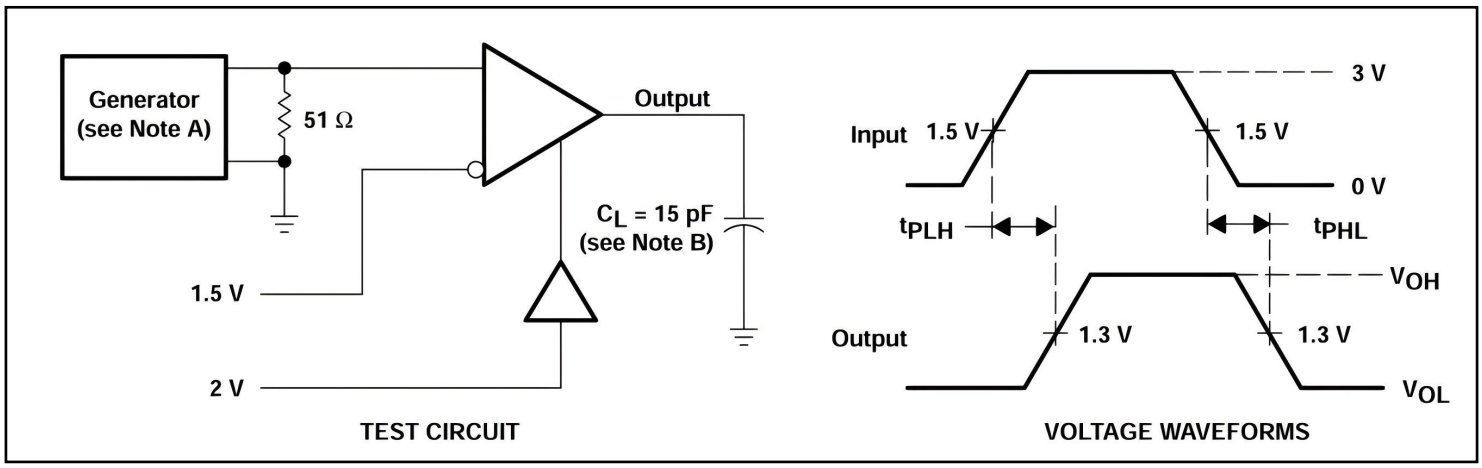


Fig 2. Test Circuit and Voltage Waveforms

A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, tr ≤ 6 ns, tf ≤ 6 ns. B. CL includes probe and stray capacitance.

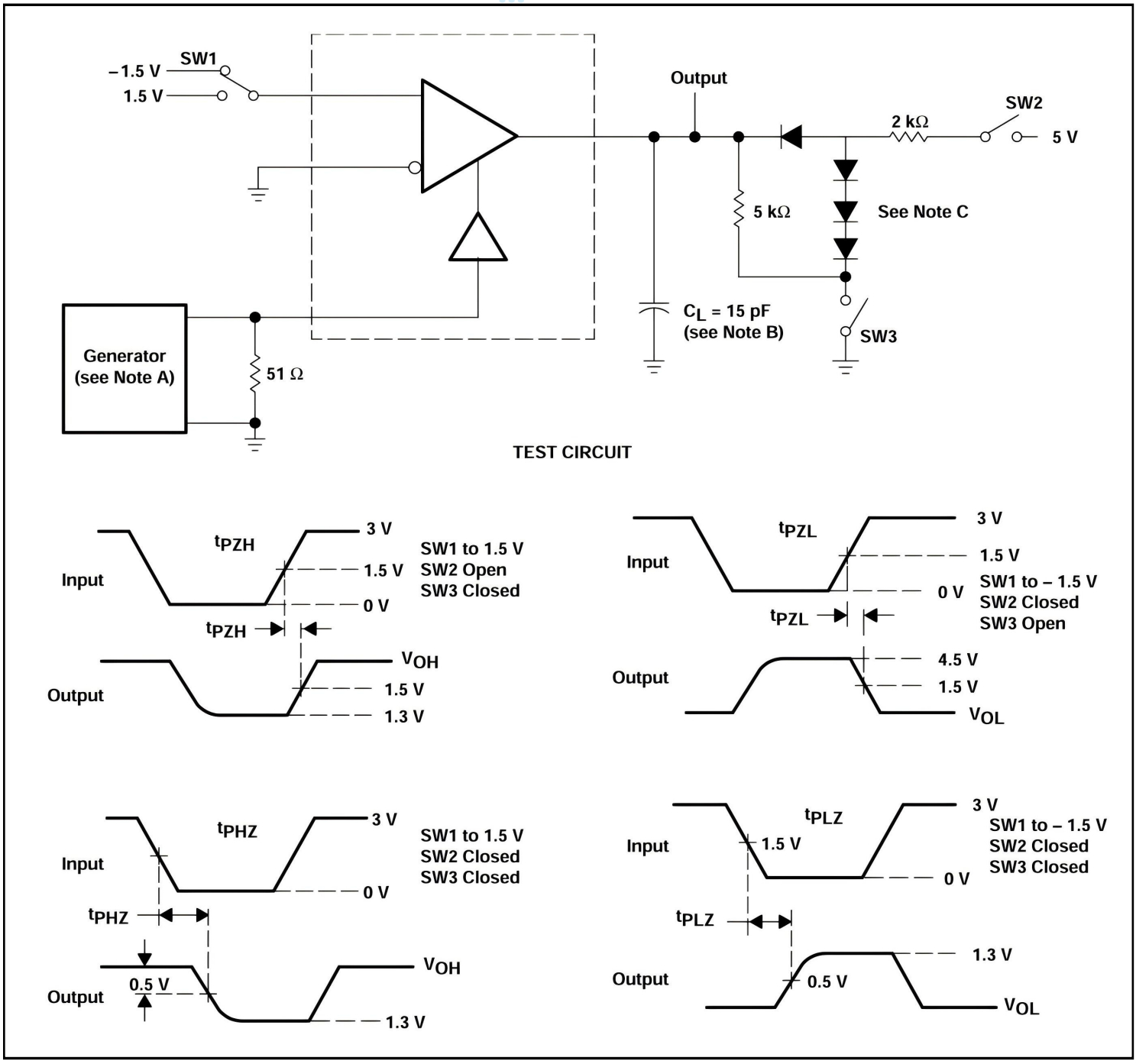


Fig 3. Test Circuit and Voltage Waveforms

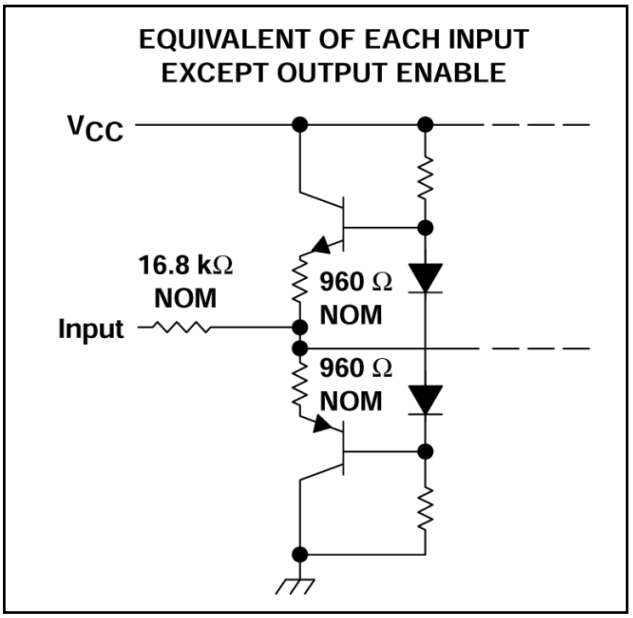
A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, t_r ≤ 6 ns, t_f ≤ 6 ns.
B. C_L includes probe and stray capacitance.
C. All diodes are 1N916 or equivalent.

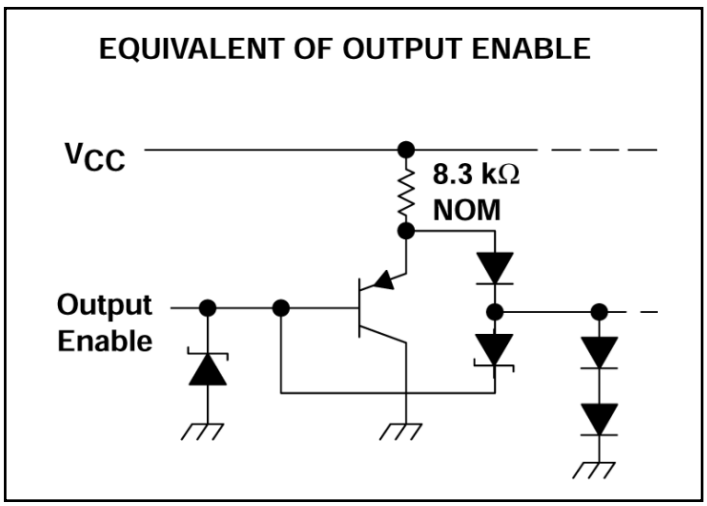
Detailed Description
Device Functional Modes

Function Table (Each Receiver)

DIFFERENTIAL INPUTS	ENABLE	OUTPUT
A-B		Y
VID≤0.2V	H	H
-0.2V<VID<0.2V	H	?
VID≤-0.2V	H	L
Irrelevant	L	Z
Open	H	?

(1) H = high level, L = low level, Z = high impedance (off), ? = indeterminate





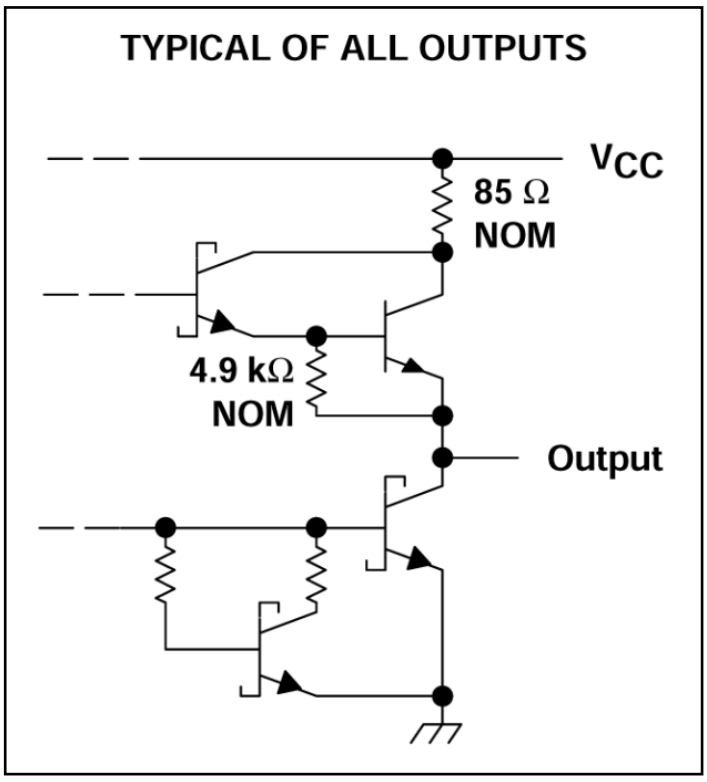
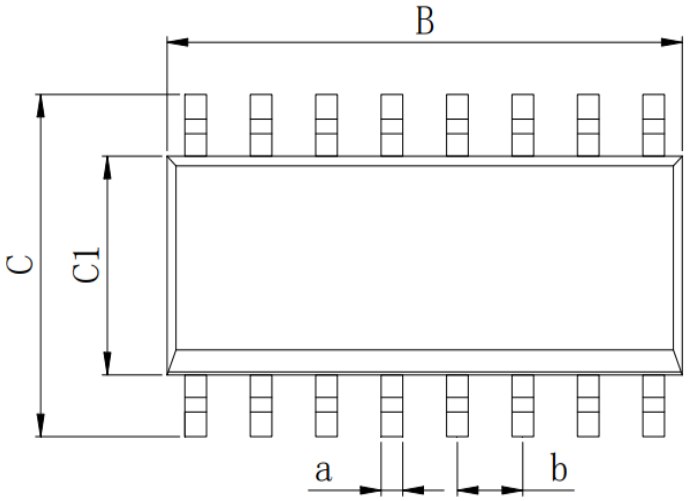
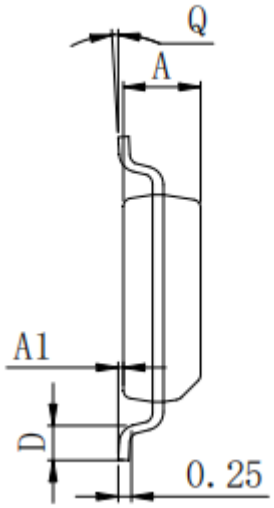


Fig 4. Schematics of Inputs and Outputs

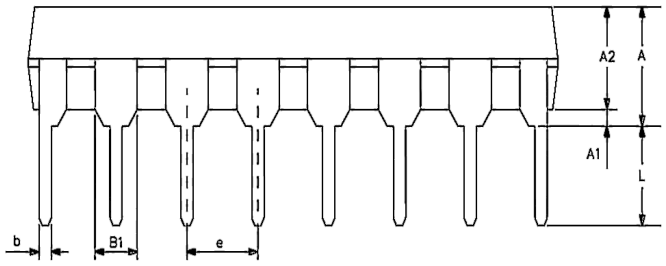
Package SOP16

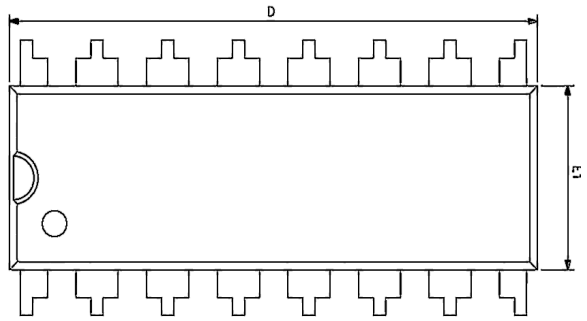


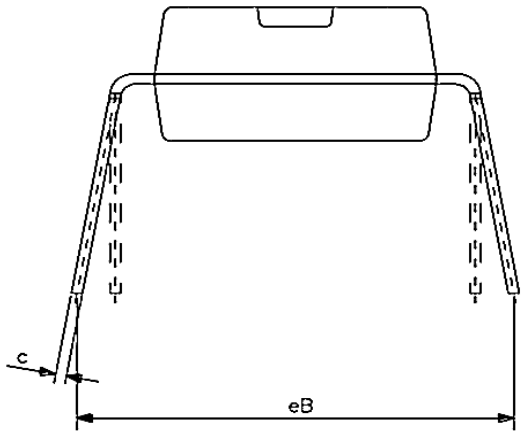


SYMBOL	MIN./mm	MAX./mm
A	1.35	1.55
A1	0.05	0.2
B	9.80	10.00
C	5.80	6.20
C1	3.80	4.00
D	0.40	0.80
Q	0°	8°
a	0.35	0.45
b	1.27BSC	

Package DIP16







SIZE / SYMBOL	MIN./mm	MAX./mm
A2	3.20	3.60
A1	0.51	___
A	3.60	5.33
L	3.00	3.60
b	0.36	0.56
B1	1.52	
D	18.80	19.94
E1	6.20	6.60
e	2.54	
C	0.20	0.36
eB	7.62	9.30
R	0.20TYP	
R1	0.30TYP	
θ	0°	8°
θ1	45°TYP	
02	12°TYP	
03	0°	8°
04	0°	10°

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