

1. General Description

The NXS0108 is an 8-bit, dual supply translating transceiver with auto direction sensing, that enables bidirectional voltage level translation. It features two 8-bit input-output ports (An and Bn), one output enable input (OE) and two supply pins ($V_{CC(A)}$ and $V_{CC(B)}$). $V_{CC(A)}$ can be supplied at any voltage between 1.3 V and 5.5 V and $V_{CC(B)}$ can be supplied at any voltage between 1.65 V and 5.5 V, making the device suitable for translating between any of the voltage nodes (1.8 V, 2.5 V, 3.3 V and 5.0 V). Pins An and OE are referenced to $V_{CC(A)}$ and pins Bn are referenced to $V_{CC(B)}$. A LOW level at pin OE causes the outputs to assume a high-impedance OFF-state. This device is fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

2. Features and Benefits

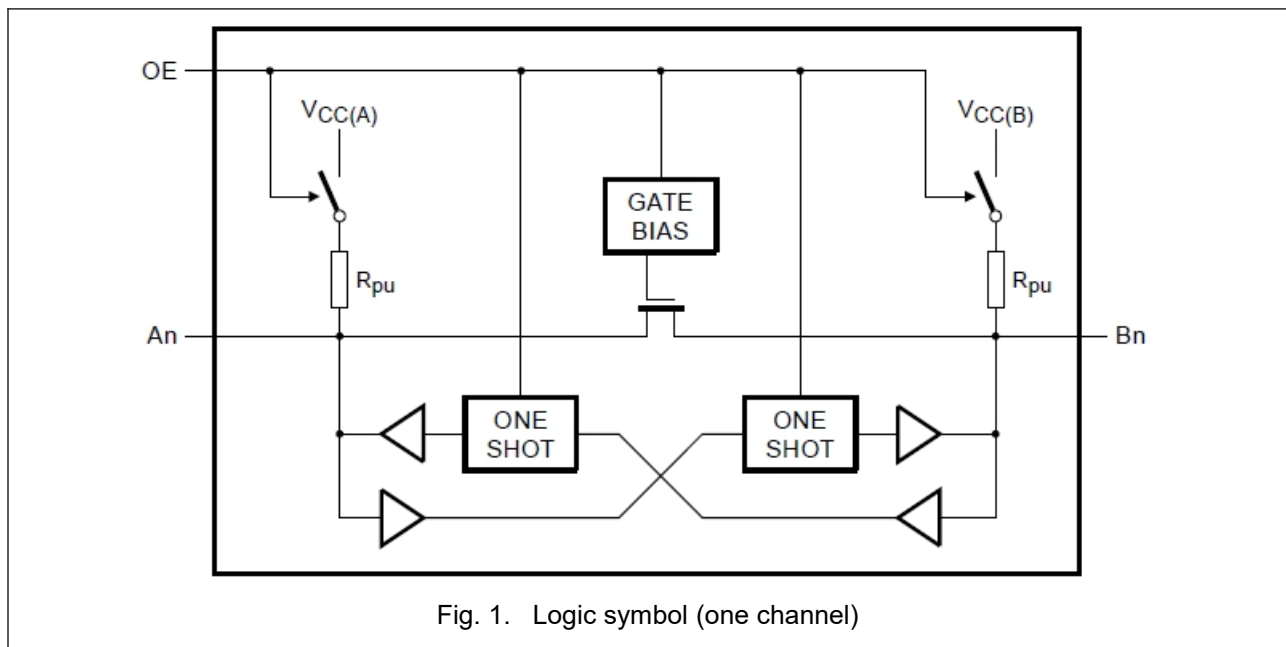
- Wide supply voltage range:
 - $V_{CC(A)}$: 1.3 V to 5.5 V and $V_{CC(B)}$: 1.65 V to 5.5 V
- Maximum data rates:
 - Push-pull: 40 Mbps
 - Open-drain: 2 Mbps
- I_{OFF} circuitry provides partial Power-down mode operation
- Inputs accept voltages up to 5.5 V
- No power-supply sequencing required – V_{CCA} or V_{CCB} can be ramped first
- Latch-up performance exceeds 100 mA per JESD 78B Class II
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2500 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering Information

Table 1. Ordering information

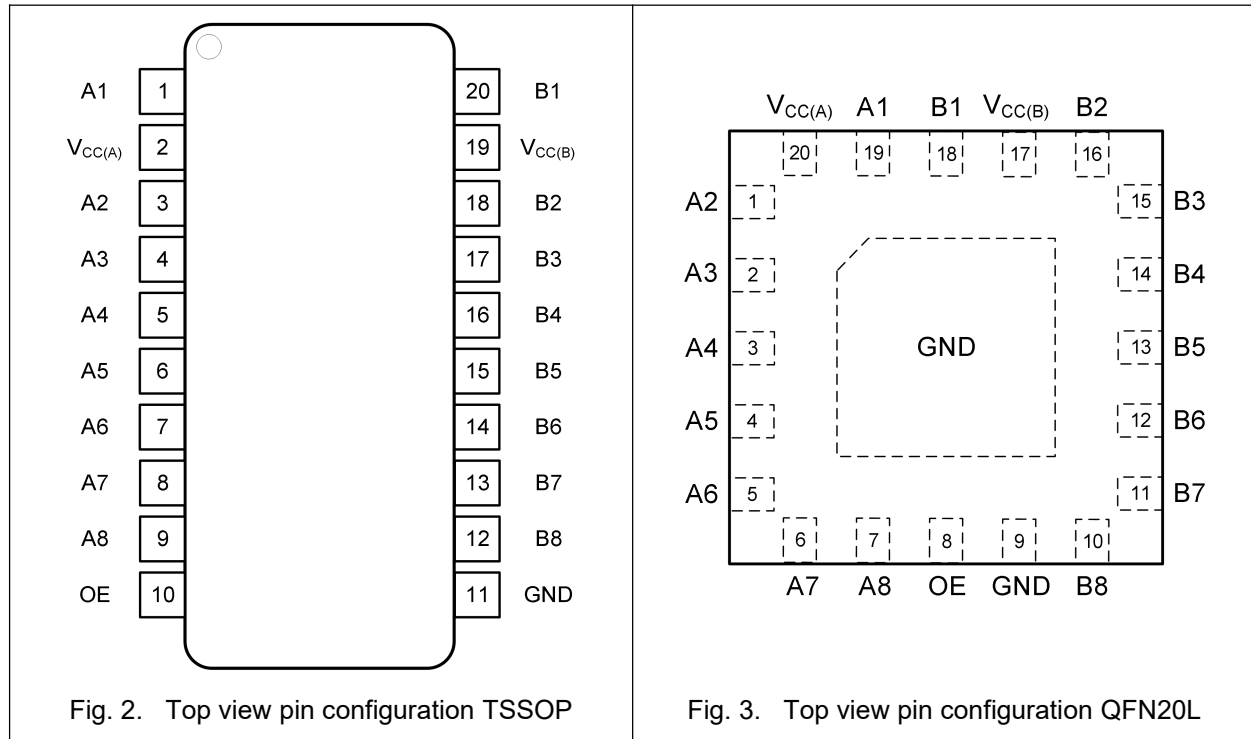
Type number	Package		
	Name	Description	Quantity
NXS0108PW	TSSOP-20L	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	2500
NXS0108UD	QFN3x3-20L	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 3 × 3 × 0.8 mm	3000

4. Function Diagram



5. Pinning Information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin		Description
	TSSOP20L	QFN20L	
$V_{CC(A)}$	2	20	supply voltage A
A1,A2,A3,A4,A5,A6,A7,A8	1,3,4,5,6,7,8,9	19,1,2,3,4,5,6,7	data input or output (referenced to $V_{CC(A)}$)
GND	11	9	ground (0V)
OE	10	8	output enable input (active HIGH; referenced to $V_{CC(A)}$)
B8,B7,B6,B5,B4,B3,B2,B1	12,13,14,15,16,17,18,20	10,11,12,13,14,15,16,18	data input or output (referenced to $V_{CC(B)}$)
$V_{CC(B)}$	19	17	supply voltage B

6. Functional Description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state

Supply voltage		Input	Input/output	
$V_{CC(A)}$ [1]	$V_{CC(B)}$	OE	An	Bn
1.3 V to 5.5 V	1.65 V to 5.5 V	L	Z	Z
1.3 V to 5.5 V	1.65 V to 5.5 V	H	input or output	output or input
GND [2]	GND [2]	X	Z	Z

[1] $V_{CC(A)}$ must be less than or equal to $V_{CC(B)}$.

[2] When either $V_{CC(A)}$ or $V_{CC(B)}$ is at GND level, the device goes into power-down mode.

7. Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Table 5. Absolute Maximum Ratings

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND.

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(A)}$	supply voltage A		-0.5	6.5	V
$V_{CC(B)}$	supply voltage B		-0.5	6.5	V
V_I	input voltage	OE [1]	-0.5	6.5	V
		An, Bn; Power-down or 3-state mode [1]	-0.5	6.5	V
		An, Bn; Active mode [1] [2] [3]	-0.5	$V_{CCI}+0.5$	V
V_O	output voltage	An, Bn; Power-down or 3-state mode [1]	-0.5	6.5	V
		An, Bn; Active mode [1] [3] [4]	-0.5	$V_{CCO}+0.5$	V
I_{IK}	input clamping current	$V_I < 0$ V	-50		mA
I_{OK}	output clamping current	$V_O < 0$ V	-50		mA
I_O	output current	$V_O = 0$ V to V_{CCO} [4]		± 50	mA
I_{CC}	supply current	$I_{CC(A)}$ or $I_{CC(B)}$		100	mA
I_{GND}	ground current		-100		mA
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to $+125$ °C		250	mW
T_{stg}	storage temperature		-65	150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] V_{CCI} is the supply voltage associated with the input.

[3] $V_{CCI} + 0.5$ V or $V_{CCO} + 0.5$ V should not exceed 6.5 V.

[4] V_{CCO} is the supply voltage associated with the output.

8. Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. EnergyMath does not recommend exceeding them or designing to Absolute Maximum Ratings.

Table 6. Recommended Operating Conditions[1] [2]

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(A)}$	supply voltage A		1.3	5.5	V
$V_{CC(B)}$	supply voltage B		1.65	5.5	V
V_i	input voltage	OE	0	5.5	V
		Power-down or 3-state mode			
		An	0	5.5	V
		Bn	0	5.5	V
		Active mode			V
		An, Bn [3]	0	V_{CCI}	V
V_o	output voltage	Power-down or 3-state mode			V
		An	0	5.5	V
		Bn	0	5.5	V
		Active mode			V
		An, Bn [4]	0	V_{CCO}	V
T_{amb}	ambient temperature		-40	125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	A or B port; push-pull driving			
		$V_{CC(A)} = 1.3 \text{ V to } 5.5 \text{ V};$ $V_{CC(B)} = 1.65 \text{ V to } 5.5 \text{ V}$		10	ns/V
		OE input			
		$V_{CC(A)} = 1.3 \text{ V to } 5.5 \text{ V};$ $V_{CC(B)} = 1.65 \text{ V to } 5.5 \text{ V}$		10	ns/V

[1] The A and B sides of an unused I/O pair must be held in the same state, both at V_{CCI} or both at GND.

[2] $V_{CC(A)}$ must be less than or equal to $V_{CC(B)}$.

[3] V_{CCI} is the supply voltage associated with the input.

[4] V_{CCO} is the supply voltage associated with the output.

9. Static Characteristics

Table 7. Typical supply current

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); Tamb = 25 °C.

V _{CC(A)}	V _{CC(B)}								Unit
	1.8 V		2.5 V		3.3 V		5.0 V		
	I _{CC(A)}	I _{CC(B)}	I _{CC(A)}	I _{CC(B)}	I _{CC(A)}	I _{CC(B)}	I _{CC(A)}	I _{CC(B)}	
1.3 V	0.1	0.3	0.1	0.9	0.1	1.9	0.1	5.6	μA
1.5 V	0.1	0.1	0.1	0.7	0.1	1.7	0.1	5	μA
1.8 V	0.1	0.1	0.1	0.5	0.1	1.5	0.1	4.6	μA
2.5 V			0.1	0.1	0.1	0.8	0.1	3.8	μA
3.3 V					0.1	0.1	0.1	2.8	μA

Table 8. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).[1]

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
V_{IH}	HIGH-level input voltage	A port						
		$V_{CC(A)} = 1.3 \text{ V to } 1.95 \text{ V};$ $V_{CC(B)} = 1.65 \text{ V to } 5.5 \text{ V}$	$V_{CC(A)} - 0.2$		$V_{CC(A)}$	$V_{CC(A)} - 0.2$	$V_{CC(A)}$	V
		$V_{CC(A)} = 2.3 \text{ V to } 5.5 \text{ V};$ $V_{CC(B)} = 2.3 \text{ V to } 5.5 \text{ V}$	$V_{CC(A)} - 0.4$		$V_{CC(A)}$	$V_{CC(A)} - 0.4$	$V_{CC(A)}$	V
		B port						
		$V_{CC(A)} = 1.3 \text{ V to } 5.5 \text{ V};$ $V_{CC(B)} = 1.65 \text{ V to } 5.5 \text{ V}$	$V_{CC(B)} - 0.4$		$V_{CC(B)}$	$V_{CC(B)} - 0.4$	$V_{CC(B)}$	V
		OE input						
V_{IL}	LOW-level input voltage	$V_{CC(A)} = 1.3 \text{ V to } 5.5 \text{ V};$ $V_{CC(B)} = 1.65 \text{ V to } 5.5 \text{ V}$	$0.65V_{CC(A)}$		$V_{CC(A)}$	$0.65V_{CC(A)}$	$V_{CC(A)}$	V
		A or B port						
		$V_{CC(A)} = 1.3 \text{ V to } 5.5 \text{ V};$ $V_{CC(B)} = 1.65 \text{ V to } 5.5 \text{ V}$	0		0.15	0	0.15	V
		OE input						
V_{OH}	HIGH-level output voltage	$V_{CC(A)} = 1.3 \text{ V to } 5.5 \text{ V};$ $V_{CC(B)} = 1.65 \text{ V to } 5.5 \text{ V}$	0		$0.35V_{CC(A)}$	0	$0.35V_{CC(A)}$	V
		A port; $I_O = -20 \mu A; V_I \geq V_{CC(B)} - 0.4 \text{ V}$						
		$V_{CC(A)} = 1.3 \text{ V to } 5.5 \text{ V};$ $V_{CC(B)} = 1.65 \text{ V to } 5.5 \text{ V}$	$0.67V_{CC(A)}$			$0.67V_{CC(A)}$		V
		B port; $I_O = -20 \mu A; V_I \geq V_{CC(A)} - 0.2 \text{ V}$						
V_{OH}	HIGH-level output voltage	$V_{CC(A)} = 1.3 \text{ V to } 5.5 \text{ V};$ $V_{CC(B)} = 1.65 \text{ V to } 5.5 \text{ V}$	$0.67V_{CC(B)}$			$0.67V_{CC(B)}$		V

NXS0108

Dual supply translating transceiver; open drain; auto direction sensing

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
V_{OL}	LOW-level output voltage	A or B port; IO = 1 mA; VI ≤ 0.15 V						
		$V_{CC(A)} = 1.3 \text{ V to } 5.5 \text{ V};$ $V_{CC(B)} = 1.65 \text{ V to } 5.5 \text{ V}$			0.4		0.4	V
I_{OZ}	OFF-state output current	A or B port; $V_{CC(A)} = 1.3 \text{ V to } 5.5 \text{ V};$ $V_{CC(B)} = 1.65 \text{ V to } 5.5 \text{ V}$		±1	±2		±12	μA
I_I	input leakage current	OE input; $V_{CC(A)} = 1.3 \text{ V to } 5.5 \text{ V};$ $V_{CC(B)} = 1.65 \text{ V to } 5.5 \text{ V}$		±1	±2		±12	μA
I_{OFF}	power-off leakage current	A port; VI or VO = 0 V to 5.5 V; $V_{CC(A)} = 0 \text{ V};$ $V_{CC(B)} = 0 \text{ V to } 5.5 \text{ V}$		±1	±2		±12	μA
		B port; VI or VO = 0 V to 5.5 V; $V_{CC(B)} = 0 \text{ V};$ $V_{CC(A)} = 0 \text{ V to } 5.5 \text{ V}$		±1	±2		±12	μA
I_{CC}	supply current	OE = 0 V or $V_{CC(A)}$; An, Bn open						
		$I_{CC(A)}$						
		$V_{CC(A)} = 1.3 \text{ V to } 5.5 \text{ V};$ $V_{CC(B)} = 1.65 \text{ V to } 5.5 \text{ V}$			2.4		15	μA
		$V_{CC(A)} = 5.5 \text{ V};$ $V_{CC(B)} = 0 \text{ V}$			2.2		15	μA
		$V_{CC(A)} = 0 \text{ V};$ $V_{CC(B)} = 5.5 \text{ V}$			-1		-8	μA
		$I_{CC(B)}$						
		$V_{CC(A)} = 1.3 \text{ V to } 5.5 \text{ V};$ $V_{CC(B)} = 1.65 \text{ V to } 5.5 \text{ V}$			12		30	μA
		$V_{CC(A)} = 5.5 \text{ V};$ $V_{CC(B)} = 0 \text{ V}$			-1		-5	μA
		$V_{CC(A)} = 0 \text{ V};$ $V_{CC(B)} = 5.5 \text{ V}$			1		6	μA
		$I_{CC(A)} + I_{CC(B)}$						
		$V_{CC(A)} = 1.3 \text{ V to } 5.5 \text{ V};$ $V_{CC(B)} = 1.65 \text{ V to } 5.5 \text{ V}$			14.4		45	μA
C_I	input capacitance	OE input; $V_{CC(A)} = 3.3 \text{ V};$ $V_{CC(B)} = 3.3 \text{ V}$		2				pF
$C_{I/O}$	input/output capacitance	A port; $V_{CC(A)} = 3.3 \text{ V};$ $V_{CC(B)} = 3.3 \text{ V}$						
		enabled		10				pF
		disabled		4				pF
		B port; $V_{CC(A)} = 3.3 \text{ V};$ $V_{CC(B)} = 3.3 \text{ V}$						

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Dual supply translating transceiver; open drain; auto direction sensing

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
		enabled		10				pF
		disabled		7				pF

[1] $V_{CC(A)}$ must be less than or equal to $V_{CC(B)}$.

[2] All typical values are measured at $T_{amb} = 25^{\circ}\text{C}$.

10. Dynamic Characteristics

Table 9. Dynamic characteristics for temperature range -40 °C to +85 °C

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 7.

Symbol	Parameter	Conditions	V _{CC(B)}						Unit
			2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	
V _{CC(A)} = 1.8 V ± 0.15 V									
t _{PHL}	HIGH to LOW propagation delay	A to B		4.6		4.7		5.8	ns
t _{PLH}	LOW to HIGH propagation delay	A to B		7.1		6.8		7.0	ns
t _{PHL}	HIGH to LOW propagation delay	B to A		4.4		4.5		4.7	ns
t _{PLH}	LOW to HIGH propagation delay	B to A		5.3		4.5		0.5	ns
t _{en}	enable time	OE to A, B [1]		200		200		200	ns
t _{dis}	disable time	OE to A, B; no external load [1]		35		35		35	ns
		OE to A; see Fig.5		140		140		145	ns
		OE to B; see Fig.5		125		175		125	ns
t _{TLH}	LOW to HIGH output transition time	A port	3.2	9.5	2.3	9.3	1.8	7.6	ns
		B port	3.3	10.8	2.7	9.1	2.7	7.6	ns
t _{THL}	HIGH to LOW output transition time	A port	2.0	5.9	1.9	6.0	1.7	13.3	ns
		B port	2.9	7.6	2.8	7.5	2.8	10.0	ns
t _{sk(O)}	output skew time	between channels [3]		0.7		0.7		0.7	ns
t _W	pulse width	data inputs	41		41		41		ns
f _{data}	data rate			40		40		40	Mbps
V _{CC(A)} = 2.5 V ± 0.2 V									

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Dual supply translating transceiver; open drain; auto direction sensing

Symbol	Parameter	Conditions	V _{CC(B)}						Unit
			2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	
t _{PHL}	HIGH to LOW propagation delay	A to B		3.2		3.3		3.4	ns
t _{PLH}	LOW to HIGH propagation delay	A to B		3.5		4.4		4.6	ns
t _{PHL}	HIGH to LOW propagation delay	B to A		3.0		3.6		4.3	ns
t _{PLH}	LOW to HIGH propagation delay	B to A		2.5		1.6		0.7	ns
t _{en}	enable time	OE to A, B [1]		200		200		200	ns
t _{dis}	disable time	OE to A, B; no external load [1] [2]		35		35		35	ns
		OE to A; see Fig.5		105		105		105	ns
		OE to B; see Fig.5		125		175		120	ns
t _{TLH}	LOW to HIGH output transition time	A port	2.8	7.5	2.6	6.6	1.8	6.5	ns
		B port	3.2	8.5	2.9	7.3	2.4	6.3	ns
t _{THL}	HIGH to LOW output transition time	A port	1.9	5.7	1.9	5.5	1.8	5.3	ns
		B port	2.2	7.8	2.4	6.7	2.6	6.6	ns
t _{sk(O)}	output skew time	between channels [3]		0.7		0.7		0.7	ns
t _W	pulse width	data inputs	41		41		41		ns
f _{data}	data rate			40		40		40	Mbps
V _{CC(A)} = 3.3 V ± 0.3 V									
t _{PHL}	HIGH to LOW propagation delay	A to B				2.4		3.1	ns
t _{PLH}	LOW to HIGH propagation delay	A to B				4.2		4.4	ns
t _{PHL}	HIGH to LOW propagation delay	B to A				2.5		3.3	ns
t _{PLH}	LOW to HIGH propagation delay	B to A				2.5		2.6	ns
t _{en}	enable time	OE to A, B [1]				200		200	ns
t _{dis}	disable time	OE to A, B; no external Load [1] [2]				35		35	ns
		OE to A; see Fig.5				150		150	ns
		OE to B; see Fig.5				170		120	ns
t _{TLH}	LOW to HIGH	A port			2.3	6.2	1.9	6.3	ns

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Dual supply translating transceiver; open drain; auto direction sensing

Symbol	Parameter	Conditions	V _{CC(B)}						Unit
			2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	
	output transition time	B port			2.5	6.9	2.1	7.4	ns
t _{THL}	HIGH to LOW output transition time	A port			2.0	5.4	1.9	5.0	ns
		B port			2.3	7.4	2.4	7.6	ns
t _{sk(O)}	output skew time	between channels [3]				0.7		0.7	ns
t _w	pulse width	data inputs			41		41		ns
f _{data}	data rate					40		40	Mbps

[1] t_{en} is the same as t_{PZL} and t_{PZH} ; t_{dis} is the same as t_{PLZ} and t_{PHZ} .

[2] These values are guaranteed by design.

[3] Skew between any two outputs of the same package switching in the same direction.

Table 10. Dynamic characteristics for temperature range -40 °C to +125 °C

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 7.

Symbol	Parameter	Conditions	V _{CC(B)}						Unit
			2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	
V _{CC(A)} = 1.8 V ± 0.15 V									
t _{PHL}	HIGH to LOW propagation delay	A to B		5.8		5.9		7.3	ns
t _{PLH}	LOW to HIGH propagation delay	A to B		8.5		8.5		8.8	ns
t _{PHL}	HIGH to LOW propagation delay	B to A		5.5		5.7		5.9	ns
t _{PLH}	LOW to HIGH propagation delay	B to A		6.7		5.7		0.7	ns
t _{en}	enable time	OE to A, B [1]		200		200		200	ns
t _{dis}	disable time	OE to A, B; no external load [1]		45		45		45	ns
		OE to A; see Fig.5		140		140		145	ns
		OE to B; see Fig.5		125		175		125	ns
t _{TLH}	LOW to HIGH output transition time	A port	3.2	11.9	2.3	11.7	1.8	9.5	ns
		B port	3.3	13.5	2.7	11.4	2.7	9.5	ns
t _{THL}	HIGH to LOW output transition time	A port	2.0	7.4	1.9	7.5	1.7	16.7	ns
		B port	2.9	9.5	2.8	9.4	2.8	12.5	ns
t _{sk(O)}	output skew time	between channels [3]		0.8		0.8		0.8	ns

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Symbol	Parameter	Conditions	V _{CC(B)}						Unit
			2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	
t _W	pulse width	data inputs	50		41		41		ns
f _{data}	data rate			40		40		40	Mbps
V _{CC(A)} = 2.5 V ± 0.2 V									
t _{PHL}	HIGH to LOW propagation delay	A to B		4.0		4.2		4.3	ns
t _{PLH}	LOW to HIGH propagation delay	A to B		4.4		5.2		5.5	ns
t _{PHL}	HIGH to LOW propagation delay	B to A		3.8		4.5		5.4	ns
t _{PLH}	LOW to HIGH propagation delay	B to A		3.2		2.0		0.9	ns
t _{en}	enable time	OE to A, B [1]		200		200		200	ns
t _{dis}	disable time	OE to A, B; no external load [1]		45		45		45	ns
		OE to A; see Fig.5		105		105		105	ns
		OE to B; see Fig.5		125		175		120	ns
t _{TLH}	LOW to HIGH output transition time	A port	2.8	9.3	2.6	8.3	1.8	7.8	ns
		B port	3.2	10.4	2.9	9.7	2.4	8.3	ns
t _{THL}	HIGH to LOW output transition time	A port	1.9	7.2	1.9	6.9	1.8	6.7	ns
		B port	2.2	9.8	2.4	8.4	2.6	8.3	ns
t _{sk(O)}	output skew time	between channels [3]		0.8		0.8		0.8	ns
t _W	pulse width	data inputs	50		41		41		ns
f _{data}	data rate			40		40		40	Mbps
V _{CC(A)} = 3.3 V ± 0.3 V									
t _{PHL}	HIGH to LOW propagation delay	A to B				3.0		3.9	ns
t _{PLH}	LOW to HIGH propagation delay	A to B				5.3		5.5	ns
t _{PHL}	HIGH to LOW propagation delay	B to A				3.2		4.2	ns
t _{PLH}	LOW to HIGH propagation delay	B to A				3.2		3.3	ns
t _{en}	enable time	OE to A, B [1]				200		200	ns
t _{dis}	disable time	OE to A, B; no external Load [1]				45		45	ns

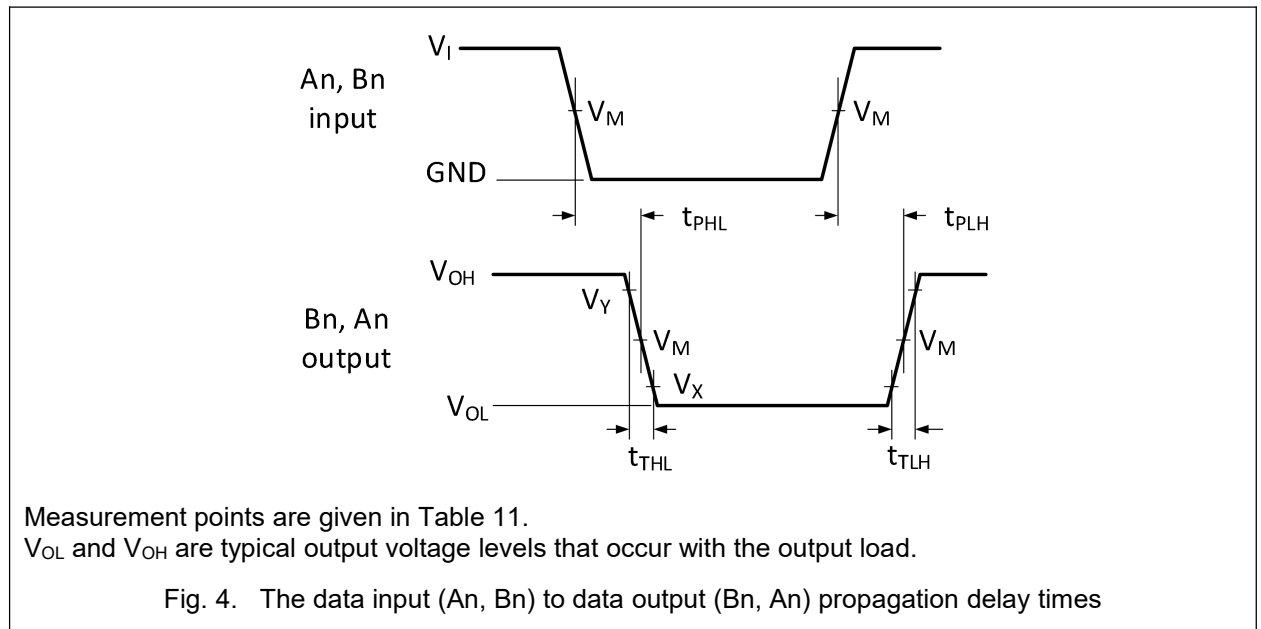
Symbol	Parameter	Conditions	V _{CC(B)}						Unit
			2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	
		[2]							
		OE to A; see Fig.5				150		150	ns
		OE to B; see Fig.5				170		120	ns
t _{TLH}	LOW to HIGH output transition time	A port			2.3	7.0	1.9	7.4	ns
		B port			2.5	8.0	2.1	9.3	ns
t _{THL}	HIGH to LOW output transition time	A port			2.0	6.8	1.9	6.3	ns
		B port			2.3	9.3	2.4	9.5	ns
t _{sk(O)}	output skew time	between channels [3]				0.8		0.8	ns
t _w	pulse width	data inputs			41		41		ns
f _{data}	data rate					40		40	Mbps

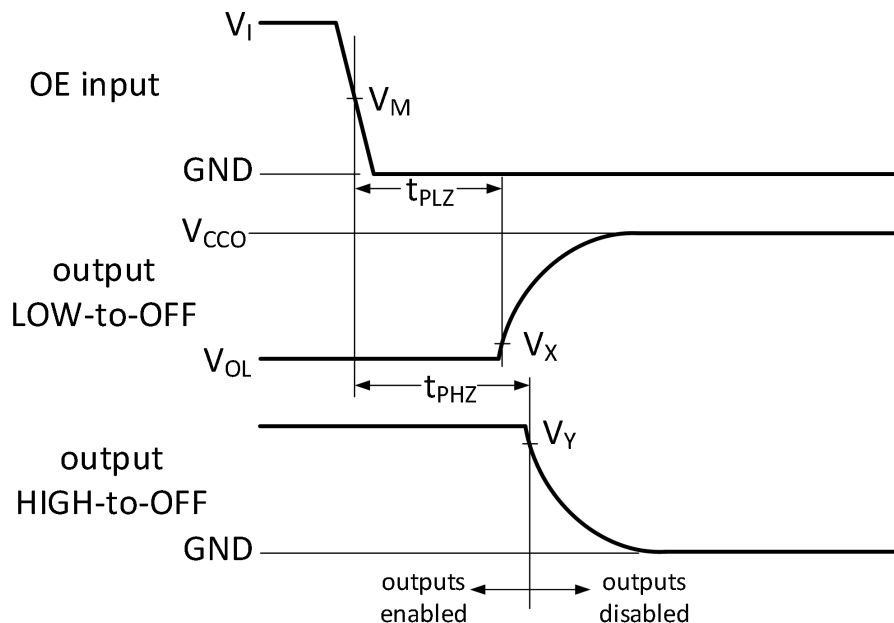
[1] t_{en} is the same as t_{pZL} and t_{pZH} ; t_{dis} is the same as t_{pLZ} and t_{pPHZ} .

[2] These values are guaranteed by design.

[3] Skew between any two outputs of the same package switching in the same direction.

10.1. Waveforms and test circuit



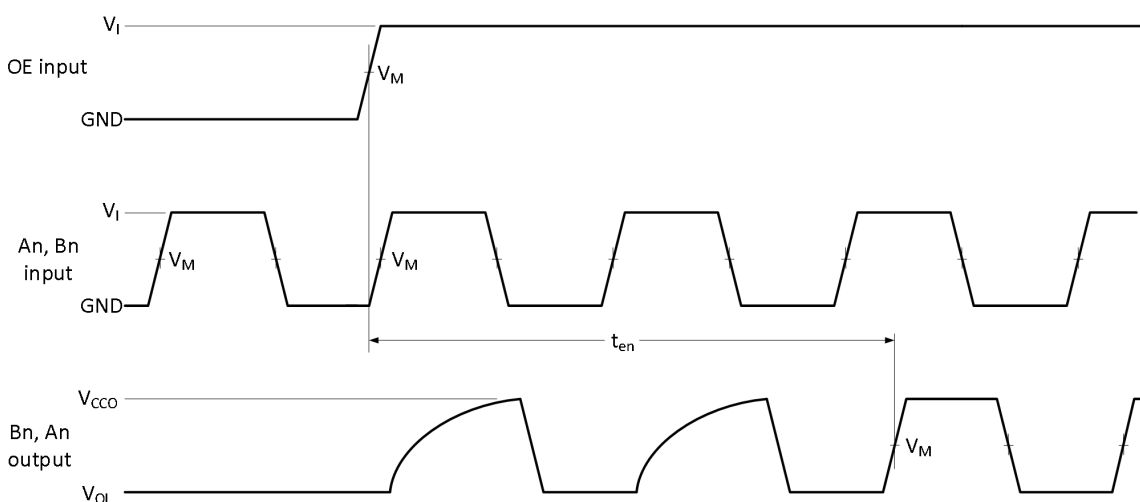


Measurement points are given in Table 11.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

V_{CCO} is the supply voltage associated with the output.

Fig. 5. Disable times



(1) The enable time (t_{en}) indicates the amount of time the user must allow for one one-shot circuitry to become operational after OE is taken HIGH. See also Section 11.6

Measurement points are given in Table 11.

V_{OL} is a typical output voltage level that occur with the output load.

V_{CCO} is the supply voltage associated with the output.

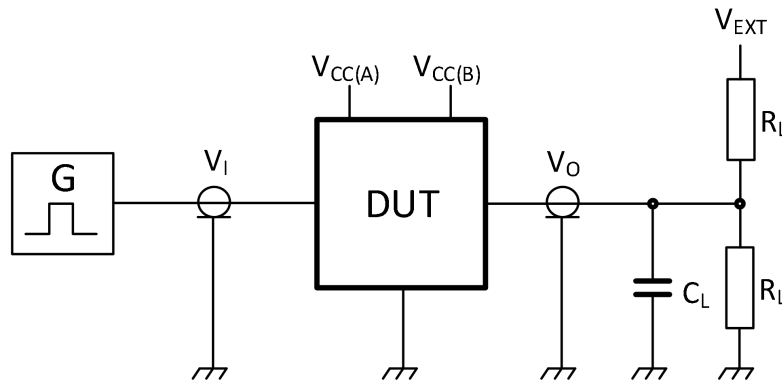
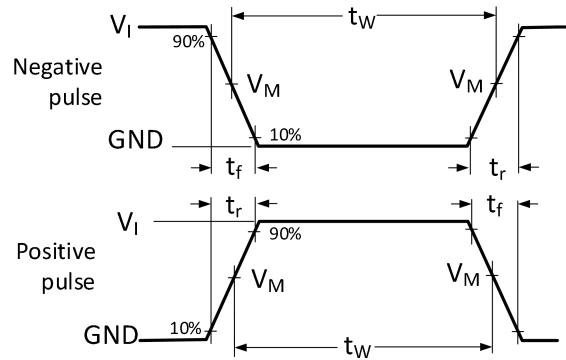
Fig. 6. Enable times

Table 11. Measurement points

Supply Voltage	Input	Output		
V_{CCO}	V_M	V_M	V_X	V_Y
$1.8\text{ V} \pm 0.15\text{ V}$	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.15\text{ V}$	$V_{OH} - 0.15\text{ V}$
$2.5\text{ V} \pm 0.2\text{ V}$	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.15\text{ V}$	$V_{OH} - 0.15\text{ V}$
$3.3\text{ V} \pm 0.3\text{ V}$	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.3\text{ V}$	$V_{OH} - 0.3\text{ V}$
$5.0\text{ V} \pm 0.5\text{ V}$	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.3\text{ V}$	$V_{OH} - 0.3\text{ V}$

[1] V_{CCI} is the supply voltage associated with the input.

[2] V_{CCO} is the supply voltage associated with the output.



Test data is given in Table 12.

All input pulses are supplied by generators having the following characteristics:

$PRR \leq 10\text{ MHz}$; $Z_o = 50\ \Omega$; $dV/dt \geq 1.0\text{ V/ns}$.

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

V_{EXT} = External voltage for measuring switching times.

Fig. 7. Test circuit for measuring switching times

NXS0108

Dual supply translating transceiver; open drain; auto direction sensing

Table 12. Test data

Supply voltage		Input		Load		V _{EXT}		
V _{CC(A)}	V _{CC(B)}	V _I [1]	$\Delta t/\Delta V$	C _L	R _L [2]	t _{PLH} , t _{PHL}	t _{PZH} , t _{PHZ}	t _{PZL} , t _{PLZ}
1.3 V to 5.5 V	1.65 V to 5.5 V	V _{CCI}	≤1.0 ns/V	15 pF	50 kΩ, 1MΩ	open	open	2V _{CCO}

[1] V_{CCI} is the supply voltage associated with the input.

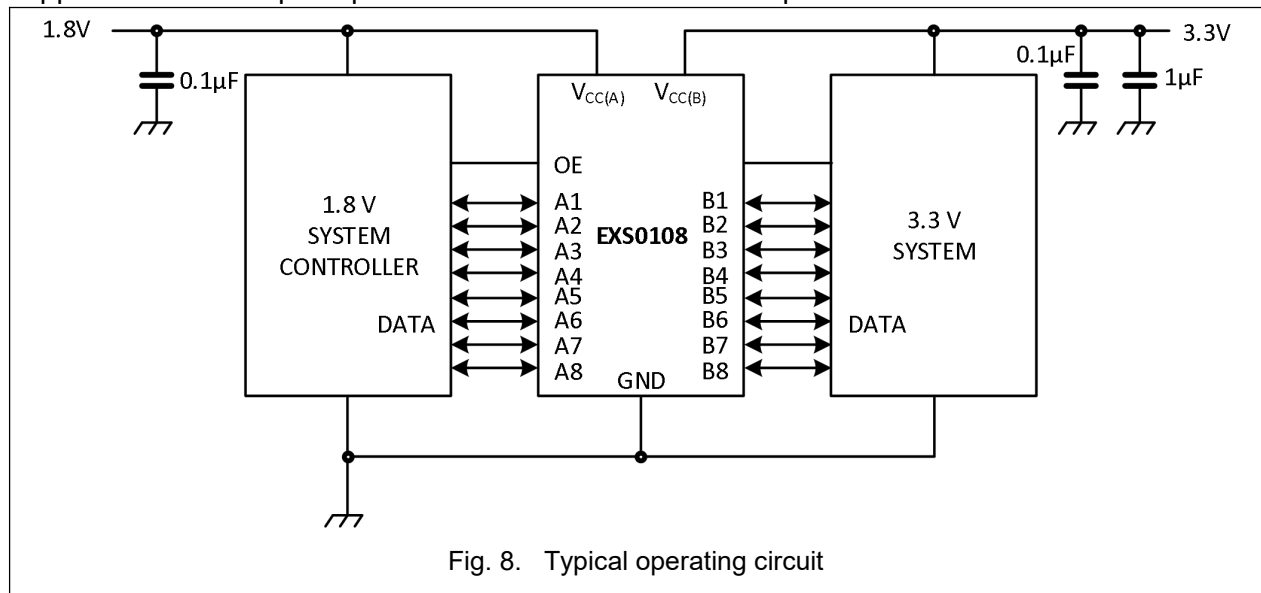
[2] For measuring data rate, pulse width, propagation delay and output rise and fall measurements, R_L = 1 MΩ. For measuring enable and disable times, R_L = 50 kΩ.

[3] V_{CCO} is the supply voltage associated with the output.

11. Application information

11.1. Applications

Voltage level-translation applications. The NXS0108 can be used in point-to-point applications to interface between devices or systems operating at different supply voltages. The device is primarily targeted at I²C or 1-wire which use open-drain drivers, it may also be used in applications where push-pull drivers are connected to the ports.



11.2. Architecture

The architecture of the NXS0108 is shown in Fig. 1. The device does not require an extra input signal to control the direction of data flow from A to B or B to A.

The NXS0108 is a "switch" type voltage translator, it employs two key circuits to enable voltage translation:

1. A pass-gate transistor (N-channel) that ties the ports together.

2. An output edge-rate accelerator that detects and accelerates rising edges on the I/O pins.

The gate bias voltage of the pass gate transistor (T3) is set at approximately one threshold voltage above the V_{CC} level of the low-voltage side. During a LOW-to-HIGH transition the output one-shot accelerates the output transition by switching on the PMOS transistors (T1, T2) bypassing the 10 k Ω pull-up resistors and increasing current drive capability. The one-shot is activated once the input transition reaches approximately $0.5V_{CC}$; it is de-activated approximately 50 ns after the output reaches $0.5V_{CC}$. During the acceleration time the driver output resistance is between approximately 50 Ω and 70 Ω .

To avoid signal contention and minimize dynamic I_{CC} , the user should wait for the one-shot circuit to turn-off before applying a signal in the opposite direction. Pull-up resistors are included in the device for DC current sourcing capability.

11.3. Input driver requirements

As the NXS0108 is a switch type translator, properties of the input driver directly effect the output signal. The external open-drain or push-pull driver applied to an I/O determines the static current sinking capability of the system; the max data rate, HIGH-to-LOW output transition time (t_{THL}) and propagation delay (t_{PHL}) are dependent upon the output impedance and edge-rate of the external driver. The limits provided for these parameters in the datasheet assume a driver with output impedance below 50 Ω is used.

11.4. Output load considerations

The maximum lumped capacitive load that can be driven is dependant upon the one-shot pulse duration. In cases with very heavy capacitive loading there is a risk that the output will not reach the positive rail within the one-shot pulse duration. To avoid excessive capacitive loading and to ensure correct triggering of the one-shot it's recommended to use short trace lengths and low capacitance connectors on NXS0108 PCB layouts. To ensure low impedance termination and avoid output signal oscillations and one-shot re-triggering, the length of the PCB trace should be such that the round trip delay of any reflection is within the one-shot pulse duration.

11.5. Power up

During operation $V_{CC(A)}$ must never be higher than $V_{CC(B)}$, however during power-up $V_{CC(A)} \geq V_{CC(B)}$ does not damage the device, so any power supply can be ramped up first. There is no special power-up sequencing required. The NXS0108 includes circuitry that disables all output ports when either $V_{CC(A)}$ or $V_{CC(B)}$ is switched off.

11.6. Enable and disable

An output enable input (OE) is used to disable the device. Setting OE to LOW causes all I/Os to assume the high-impedance OFF-state. The disable time (t_{dis} with no external load) indicates

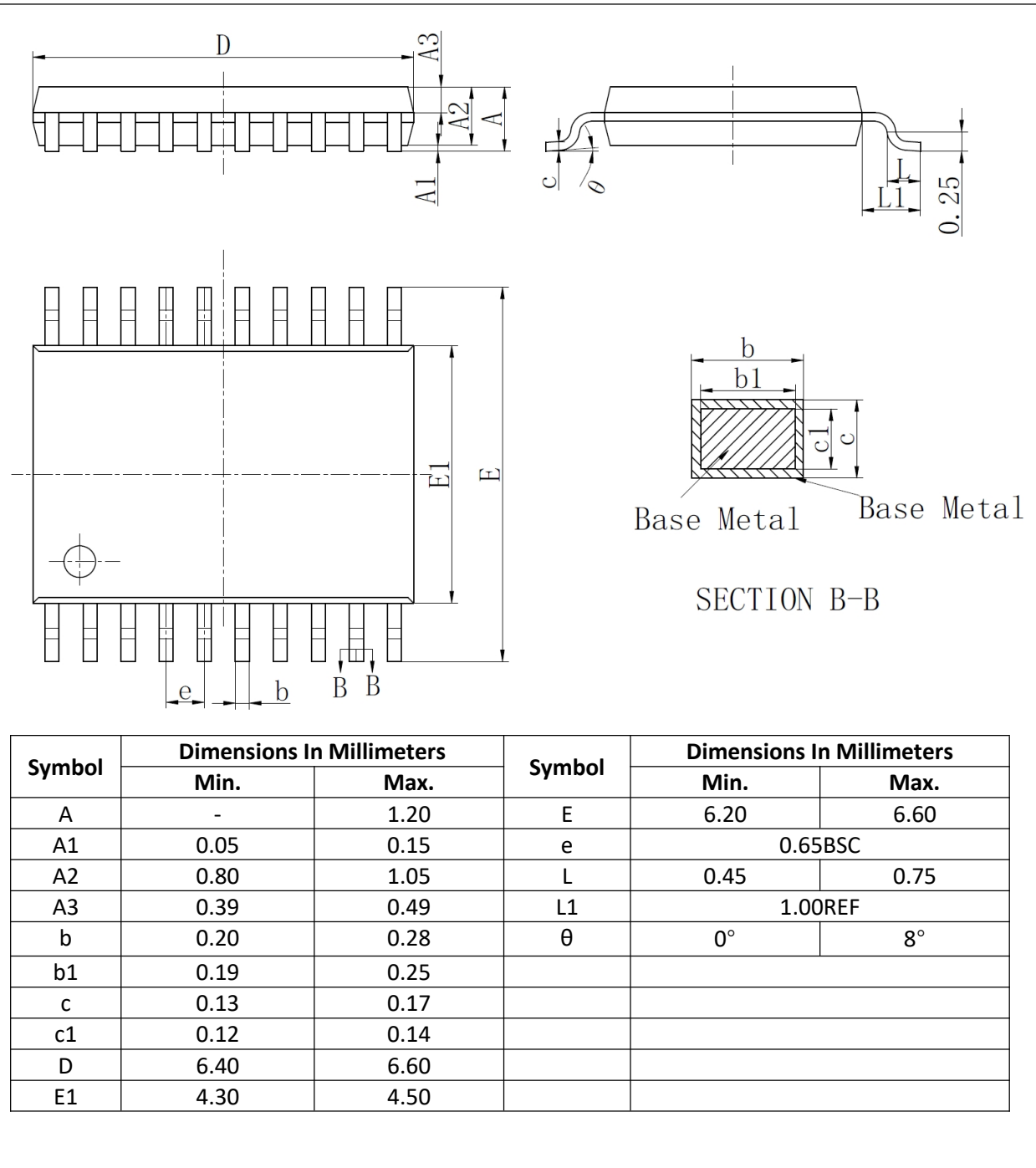
the delay between when OE goes LOW and when outputs actually become disabled. The enable time (t_{en}) indicates the amount of time the user must allow for one one-shot circuitry to become operational after OE is taken HIGH. To ensure the high-impedance OFF-state during power-up or power-down, pin OE should be tied to GND through a pull-down resistor, the minimum value of the resistor is determined by the current-sourcing capability of the driver.

11.7. Pull-up or pull-down resistors on I/O lines

Each A port I/O has an internal 10 k Ω pull-up resistor to $V_{CC(A)}$, and each B port I/O has an internal 10 k Ω pull-up resistor to $V_{CC(B)}$. If a smaller value of pull-up resistor is required, an external resistor must be added parallel to the internal 10 k Ω , this will effect the V_{OL} level. When OE goes LOW the internal pull-ups of the NXS0108 are disabled.

12. Package Outline

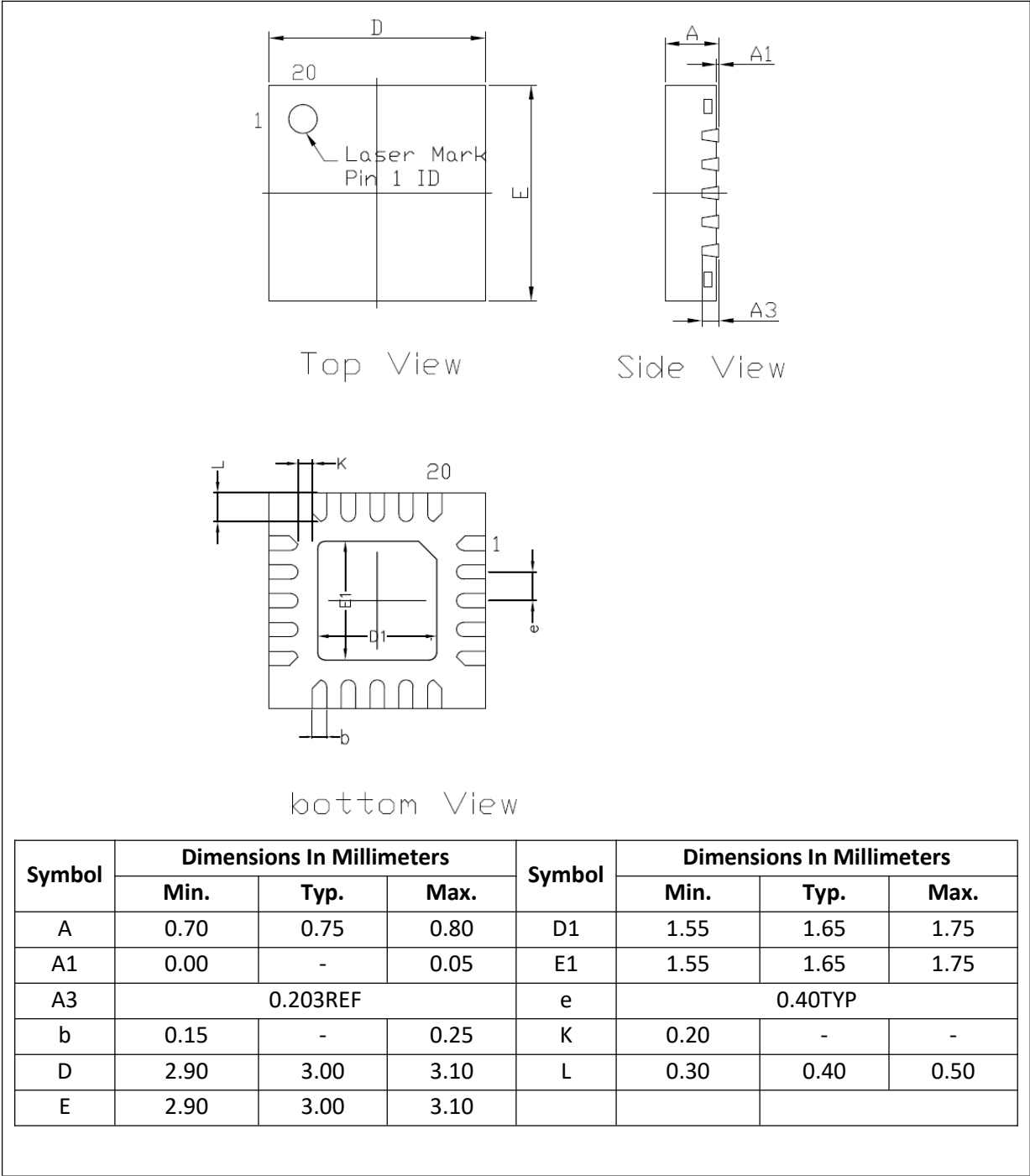
TSSOP-20L



NXS0108

Dual supply translating transceiver; open drain; auto direction sensing

QFN3x3-20L



13. Abbreviations

Table 13. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
CDM	Charged Device Model
I ² C	Inter-Integrated Circuit
PCB	Printed Circuit Board
PRR	Pulse Rate Repetition

14. Revision History

Table 14. Revision history

Document ID	Release Date	Data sheet status	Change notice	Supersedes
NXS0108 Rev. 1.0	Aug 08, 2024	Draft datasheet		