74HC595 8-Bit Shift Registers With 3-State Output Registers

1. General Description

1.1 Description

The 74HC595 devices contain an 8-bit, serial-in,parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state outputs.Separate clocks are provided for both the shift and storage register. The shift register has a direct overriding clear($\overline{SRCLR}$) input, serial (SER) input,and serial outputs for cascading. When the output-enable ($\overline{OE}$)input is high, the outputs are in the high-impedance state.

1.2 Features

- 8-Bit serial-in, parallel-out shift
- Wide operating voltage range of 2V to 6V
- High-current 3-state outputs can drive up to 15 LS-TTL loads
- Low power consumption, 10uA max I_{CC}
- ±6mA output drive at 5V
- Low input current of 1uA max
- Shift register has direct clear

1.3 Device Information

PART NUMBER	PACKAGE
74HC595	DIP
	SOP
	SSOP
	TSSOP

2. Connection Diagrams and Pin Description

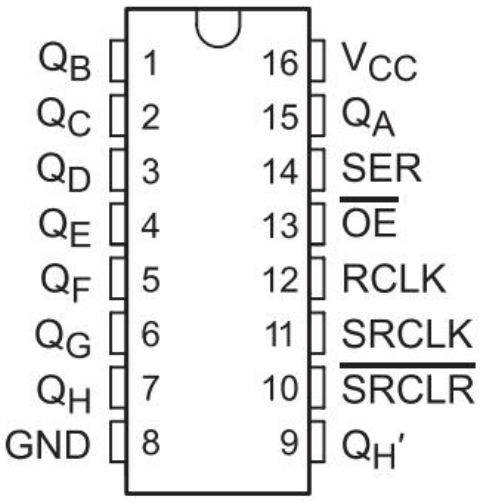


Figure 2.1 Top View

PIN No.	NAME	I/O	FUNCTION
1	Q_B	O	Data Output
2	Q_C	O	Data Output
3	Q_D	O	Data Output
4	Q_E	O	Data Output
5	Q_F	O	Data Output
6	Q_G	O	Data Output
7	Q_H	O	Data Output
8	GND		Ground
9	Q_H'	O	Data Output
10	$\overline{SRCLR}$	I	$\overline{SRCLR}$ Input
11	SRCLK	I	SRCLC Input
12	RCLK	I	RCLK Input
13	$\overline{OE}$	I	Output Enable
14	SER	I	SER Input
15	Q_A	O	Data Output
16	VCC		Supply Voltage

3. System Diagram

3.1 Logic Diagram

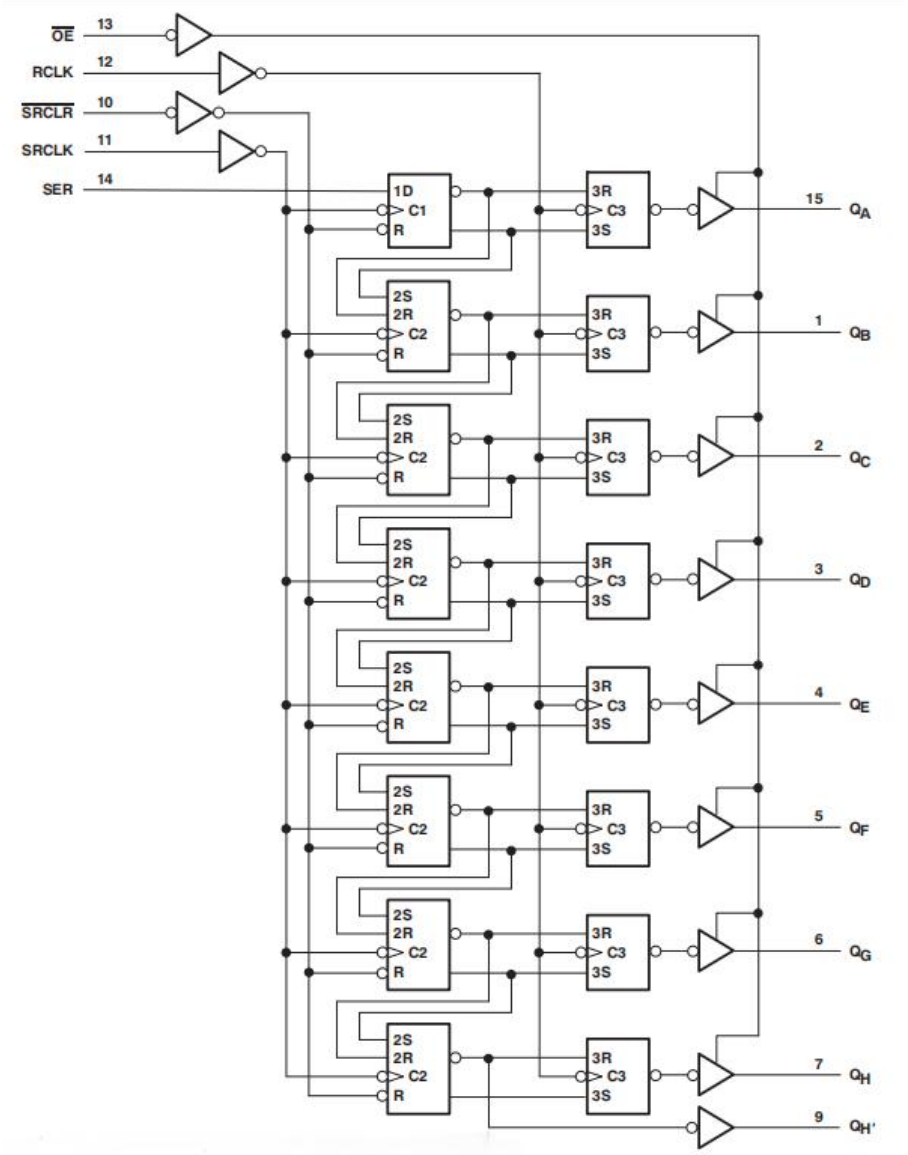


Figure 3.1：74HC595 Logic Diagram

3.2 Function Table

Input					Function
SER	SRCLK	$\overline{SRCLR}$	RCLK	$\overline{OE}$	
X	X	X	X	1	Outputs Q_A-Q_H are disabled
X	X	X	X	0	Outputs Q_A-Q_H are enabled
X	X	0	X	X	Shift register is cleared
0	↑	1	X	X	First stage of the shift register goes low,other stages store the data of previous stage, respectively
1	↑	1	X	X	First stage of the shift register goes high,other stages store the data of previous stage, respectively
X	X	X	↑	X	Shift-register data is stored in the storage register

X = don’t care, 1≡High State, 0≡Low State,↑=positive-going transition,↓=negative-going transition

4. Specifications

4.1 Absolute Maximum Ratings

Symbol	Parameter	MIN	MAX	Unit
V_{CC}	Supply Voltage	-0.5	7	V
P_D	Power Dissipation		500	mW
T_J	Junction Temperature		125	℃
T_{OP}	Operating Temperature	-40	85	℃

Absolute maximum ratings are those values beyond which the device could be permanently damaged,These are stress ratings only,which do not imply functional operation of the device at these or any other conditions beyond those indicated under normal operating conditions.

4.2 Recommended Operating Conditions

Symbol	Parameter	Test Condition	MIN	NOM	MAX	Unit
V_{CC}	Supply Voltage		2	5	6	V
V_{IH}	High Level Input Voltage	V_{CC}=2V	1.5			V
		V_{CC}=4.5V	3.15			V
		V_{CC}=6V	4.2			V
V_{IL}	Low Level Input Voltage	V_{CC}=2V			0.5	V
		V_{CC}=4.5V			1.35	V
		V_{CC}=6V			1.8	V
V_I	Input voltage		0		V_{CC}	V

4.3 Electrical Characteristics

(T_a=25℃, voltages are referenced to GND (ground=0V), unless otherwise specified)

Symbol	Parameter	Test Condition	MIN	TYP	MAX	Unit
V_{OH}	High Level Output Voltage	V_{CC}=2V,I_O=-20uA	1.9	--	--	V
		V_{CC}=4.5V,I_O=-20uA	4.4	--	--	V
		V_{CC}=6V,I_O=-20uA	5.9	--	--	V
		V_{CC}=4.5V,I_O=-4mA(Q_H')	4.0	--	--	V
		V_{CC}=4.5V,I_O=-6mA(Q_A-Q_H)	4.0	--	--	V
		V_{CC}=6V,I_O=-5.2mA(Q_H')	5.5	--	--	V
		V_{CC}=6V,I_O=-7.8mA(Q_A-Q_H)	5.5	--	--	V
V_{OL}	Low Level Output Voltage	V_{CC}=2V,I_O=20uA	--	--	0.1	V
		V_{CC}=4.5V,I_O=20uA	--	--	0.1	V
		V_{CC}=6V,I_O=20uA	--	--	0.1	V
		V_{CC}=4.5V,I_O=4mA(Q_H')	--	--	0.26	V
		V_{CC}=4.5V,I_O=6mA(Q_A-Q_H)	--	--	0.26	V
		V_{CC}=6V,I_O=5.2mA(Q_H')	--	--	0.26	V
		V_{CC}=6V,I_O=7.8mA(Q_A-Q_H)	--	--	0.26	V
I_I	Input Leakage Current	V_{CC}=6V,V_I=V_{CC} or GND	--	0	±1	uA
I_{OZ}	High Impedance Output Leakage Current	V_{CC}=6V,V_O=V_{CC} or GND	--	0	±2	uA
I_{CC}	Quiescent Supply Current	V_{CC}=6V,V_I=V_{CC}/GND	--	0	10	uA

5. Timing Diagrams

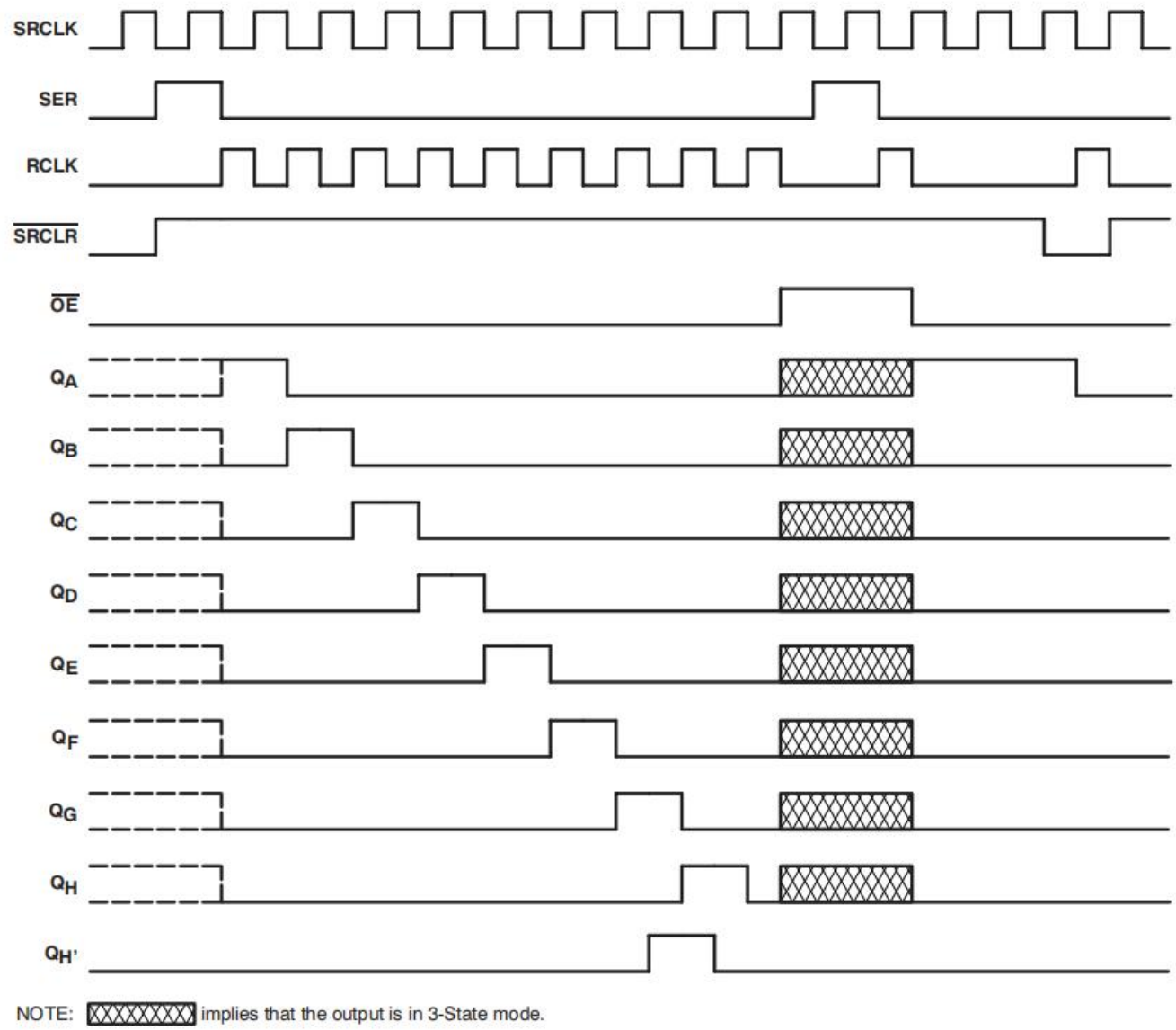


Figure 5.1：Timing diagrams for 74HC595

6. Application Information

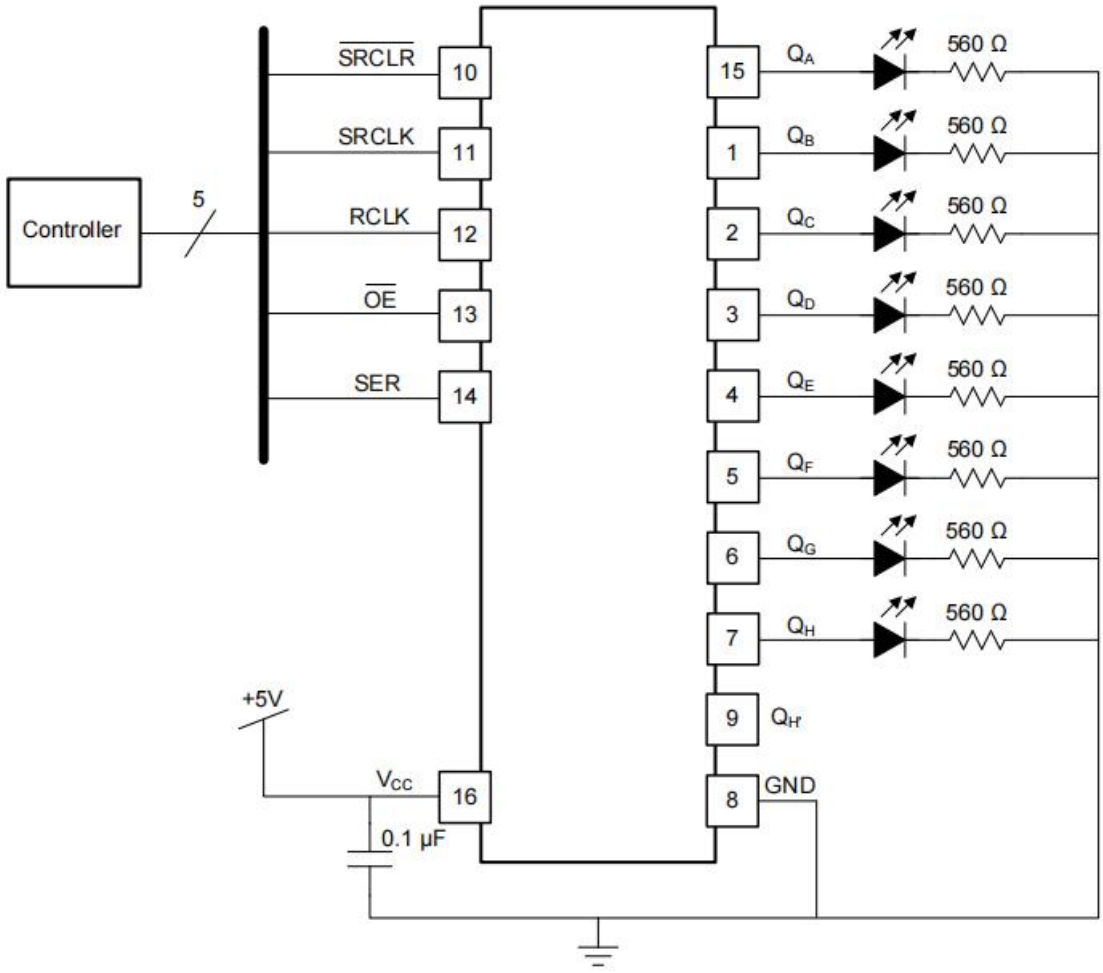


Figure 6.1：Typical application schematic

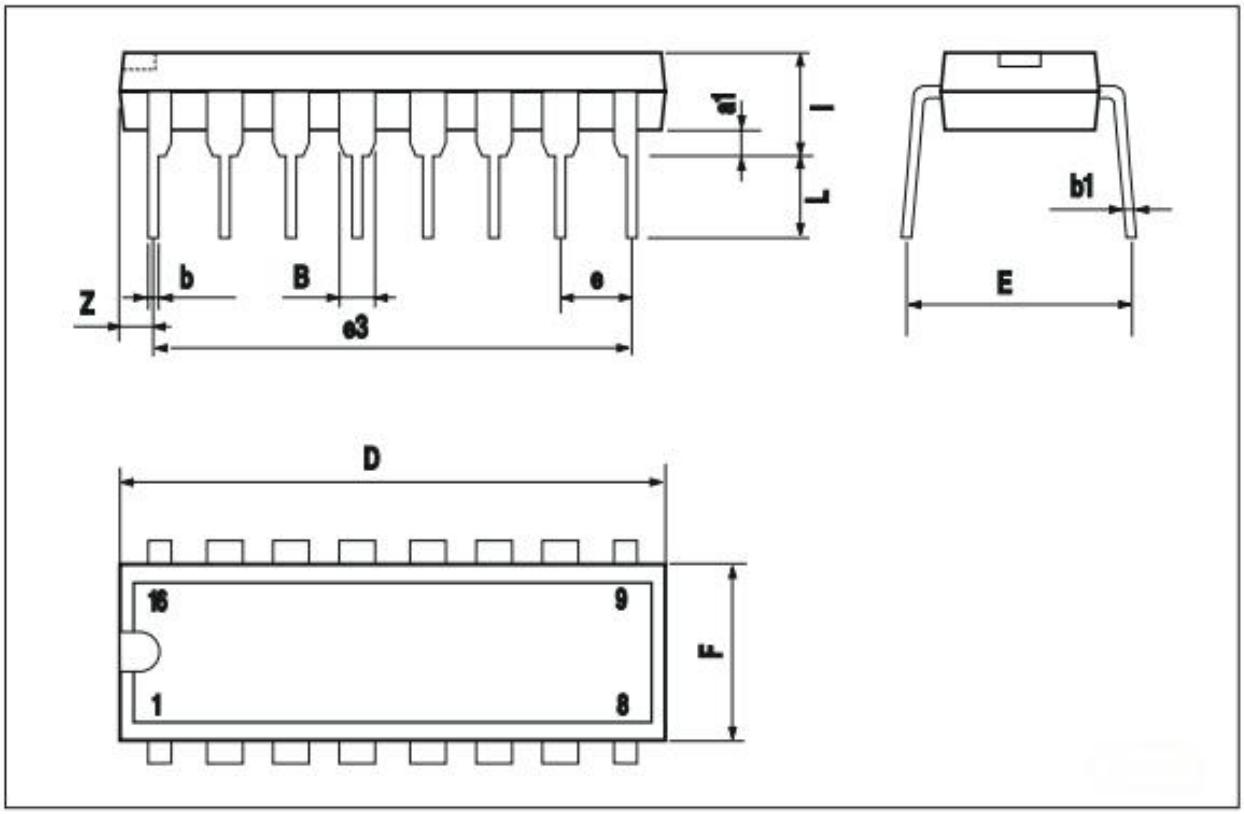
7. Ordering Information

Orderable Device	Package Type	Pins	Packing	Package Qty
74HC595ND16ACTBE	DIP	16	Tube	25
74HC595NS16ACRDQ	SOP	16	Tape & Reel	4000
74HC595SS16ACRBQ	SSOP	16	Tape & Reel	2000
74HC595TS16ACRDQ	TSSOP	16	Tape & Reel	4000

8. Package Information

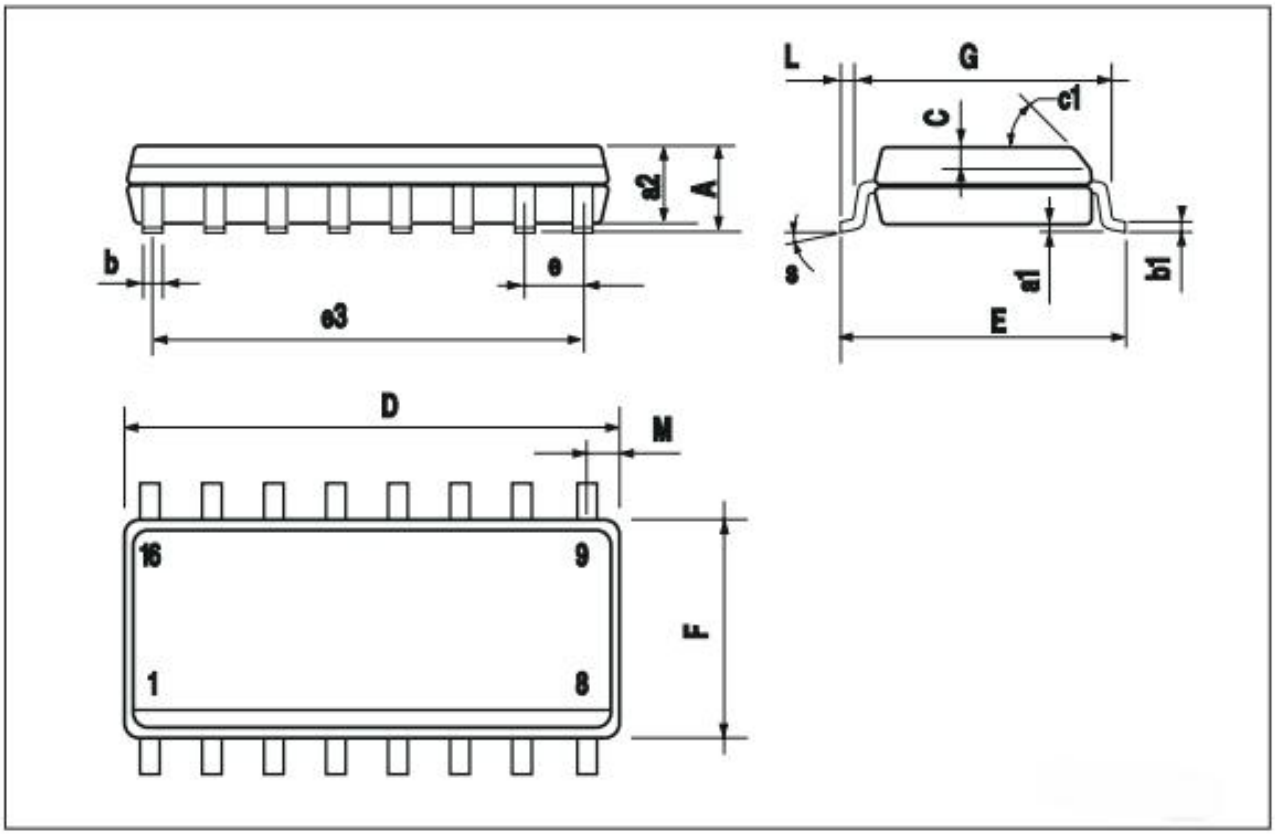
8.1 DIP16

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050

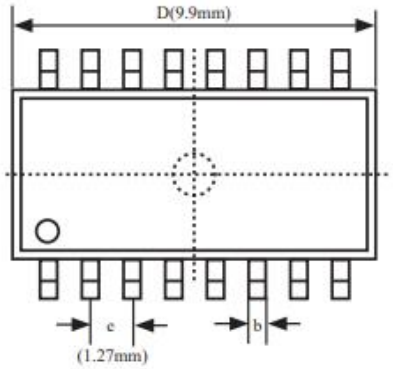


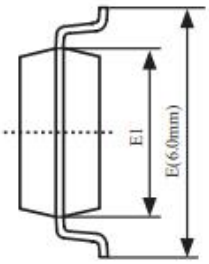
8.2 SOP16

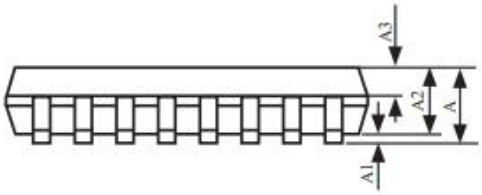
Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.068
a1	0.1		0.25	0.004		0.010
a2			1.64			0.063
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					

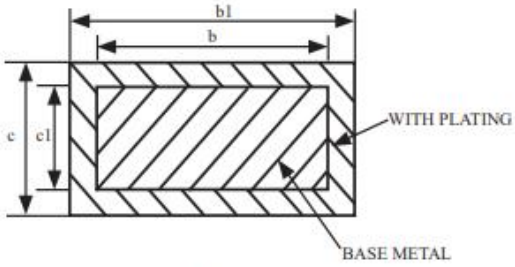


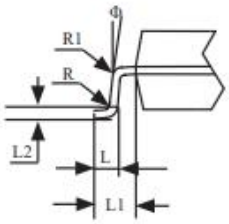
8.3 SSOP16











COMMON DIMENSIONS (UNITS OF MEASURE = MILLMETER)			
SYMBOL	MIN	NOM	MAX
A	1.35	1.60	1.75
A1	0.10	0.15	0.25
A2	1.25	1.45	1.65
A3	0.55	0.65	0.75
b1	0.36	-	0.49
b	0.35	0.40	0.45
c	0.16	-	0.25
c1	0.15	0.20	0.25
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
L	0.45	0.60	0.80
L1		1.04	
L2		0.25	
R	0.07	-	-
R1	0.07	-	-
Φ	6^0	8^0	10^0

8.4 TSSOP16

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0079
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030