74HC165 8-Bit Parallel-Load Shift Registers

1. General Description

1.1 Description

The 74HC165 devices are 8-bit parallel-load shift registers that, when clocked, shift the data toward a serial (Q_H) output. Parallel-in access to each stage is provided by eight individual direct data (A−H) inputs that are enabled by a low level at the shift/load (SH/$\overline{LD}$) input. The 74HC165 devices also feature a clock-inhibit (CLK INH) function and a complementary serial ($\overline{Q}_H$) output.

Clocking is accomplished by a low-to-high transition of the clock (CLK) input while SH/$\overline{LD}$ is held high and CLK INH is held low. The functions of CLK and CLK INH are interchangeable. Because a low CLK and a low-to-high transition of CLK INH also accomplish clocking, CLK INH must be changed to the high level only while CLK is high. Parallel loading is inhibited when SH/$\overline{LD}$ is held high. While SH/$\overline{LD}$ is low, the parallel inputs to the register are enabled independently of the levels of the CLK, CLK INH, or serial (SER) inputs.

1.2 Features

- Wide operating voltage range of 2V to 6V
- Outputs Can Drive Up to 10 LSTTL
- Low Power Consumption, 10-μA Maximum ICC at 25℃
- ±4mA Output Drive at 5 V
- Low Input Current of 1-μA Maximum at 25℃
- Complementary Outputs
- Direct Overriding Load (Data) Inputs
- Gated Clock Inputs
- Parallel-to-Serial Data Conversion

1.3 Device Information

PART NUMBER	PACKAGE
74HC165	DIP
	SOP
	TSSOP

2. Connection Diagrams and Pin Description

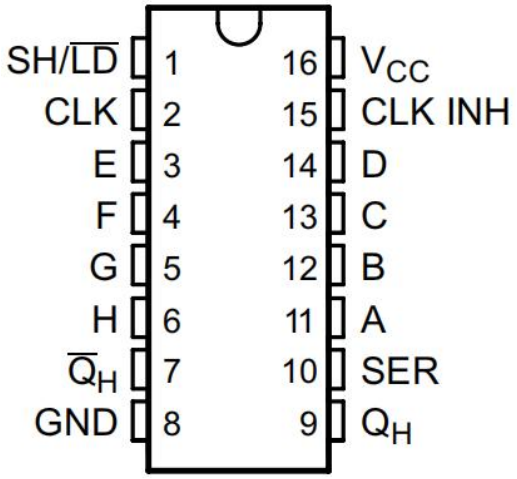


Figure 2.1 Top View

NAME	PIN	I/O	DESCRIPTION
SH/$\overline{LD}$	1	I	Shift or Load input, When High Data, shifted. When Low data is loaded from parallel inputs
CLK	2	I	Clock input
E	3	I	Parallel Input
F	4	I	Parallel Input
G	5	I	Parallel Input
H	6	I	Parallel Input
$\overline{Q}_H$	7	O	Complementary Serial Output
GND	8	-	Ground
Q_H	9	O	Serial Output
SER	10	I	Serial Input
A	11	I	Parallel Input
B	12	I	Parallel Input
C	13	I	Parallel Input
D	14	I	Parallel Input
CLK INH	15	I	Clock Inhibit, when High No change in output
VCC	16	-	Power Pin

3. System Diagram

3.1 Logic Diagram

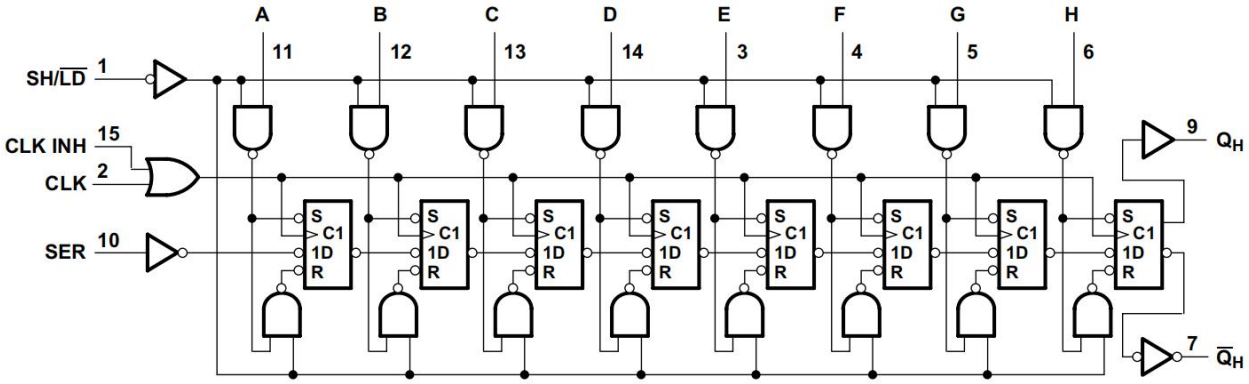


Figure 3.1：74HC165 Logic Diagram

3.2 Truth Table

INPUTS			FUNCTION
SH/$\overline{LD}$	CLK	CLK INH	
0	X	X	Parallel load
1	↑	X	No change
1	X	↑	No change
1	0	↑	Shift(1)
1	↑	0	Shift(1)

1=High State, 0=Low State ,X = Don't Care

(1) Shift : Content of each internal register shifts towards serial output Q_H. Data at SER is shifted into the first register

3.3 Timing Sequence Diagram

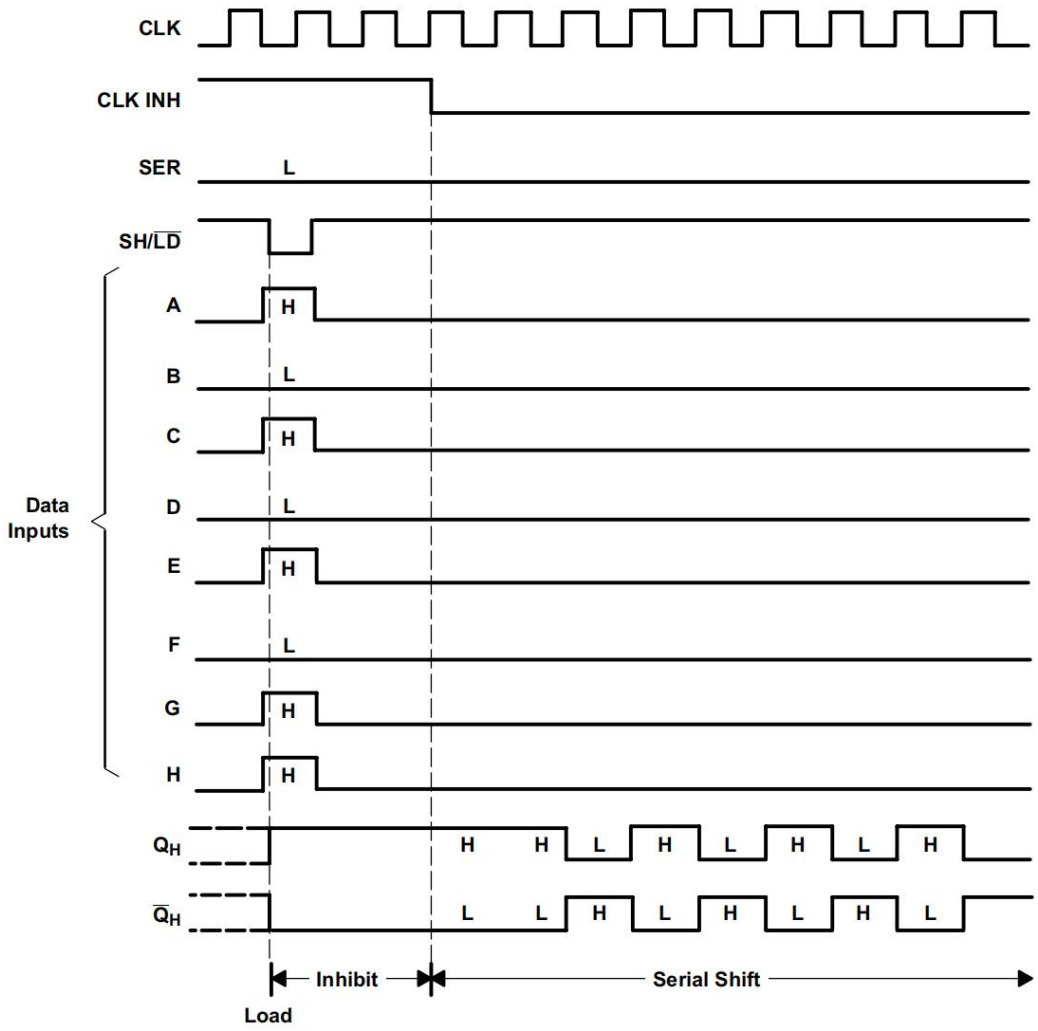


Figure 3.2：74HC165 Timing Sequence

4. Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

Symbol	Parameter	MIN	MAX	Unit
V_{CC}	Supply Voltage	-0.5	7	V
T_{stg}	Storage temperature	-65	150	℃
T_A	Operating free-air temperature	-40	85	℃

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

4.2 Recommended Operating Conditions

T_a=25℃, voltages are referenced to GND (ground=0V), unless otherwise specified(1)

Symbol	Parameter	Test Condition	MIN	NOM	MAX	Unit
V_{CC}	Supply Voltage		2	5	6	V
V_{IH}	High Level Input Voltage	V_{CC}=2V	1.5			V
		V_{CC}=4.5V	3.15			V
		V_{CC}=6V	4.2			V
V_{IL}	Low Level Input Voltage	V_{CC}=2V			0.5	V
		V_{CC}=4.5V			1.35	V
		V_{CC}=6V			1.8	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V

(1) All unused inputs of the device must be held at VCC or GND to ensure proper device operation.

4.3 Electrical Characteristics

4.3.1 DC Specifications

(T_a=25℃, voltages are referenced to GND (ground=0V), unless otherwise specified)

Symbol	Parameter	Test Condition	MIN	TYP	MAX	Unit
V_{OH}	High Level Output Voltage	V_{CC}=2V,I_O=-20uA	1.9	--	--	V
		V_{CC}=4.5V,I_O=-20uA	4.4	--	--	V
		V_{CC}=6V,I_O=-20uA	5.9	--	--	V
		V_{CC}=4.5V,I_O=-4mA	4.0	--	--	V
		V_{CC}=6V,I_O=-5.2mA	5.5	--	--	V
V_{OL}	Low Level Output Voltage	V_{CC}=2V,I_O=20uA	--	--	0.1	V
		V_{CC}=4.5V,I_O=20uA	--	--	0.1	V
		V_{CC}=6V,I_O=20uA	--	--	0.1	V
		V_{CC}=4.5V,I_O=4mA	--	--	0.26	V
		V_{CC}=6V,I_O=5.2mA	--	--	0.26	V
I_I	Input Leakage Current	V_{CC}=6V,V_I=V_{CC} or GND	--	--	±1	uA
I_{CC}	Quiescent Supply Current	V_{CC}=6V,V_I=V_{CC}/GND	--	--	10	uA

5. Typical Application

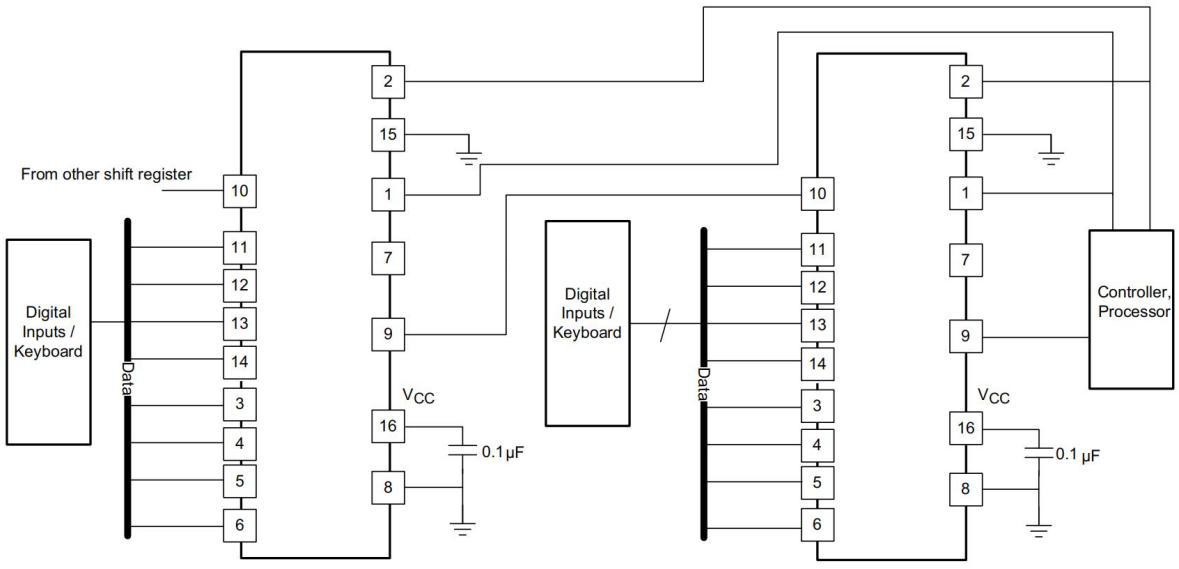


Figure 5.1：Typical Application Diagram

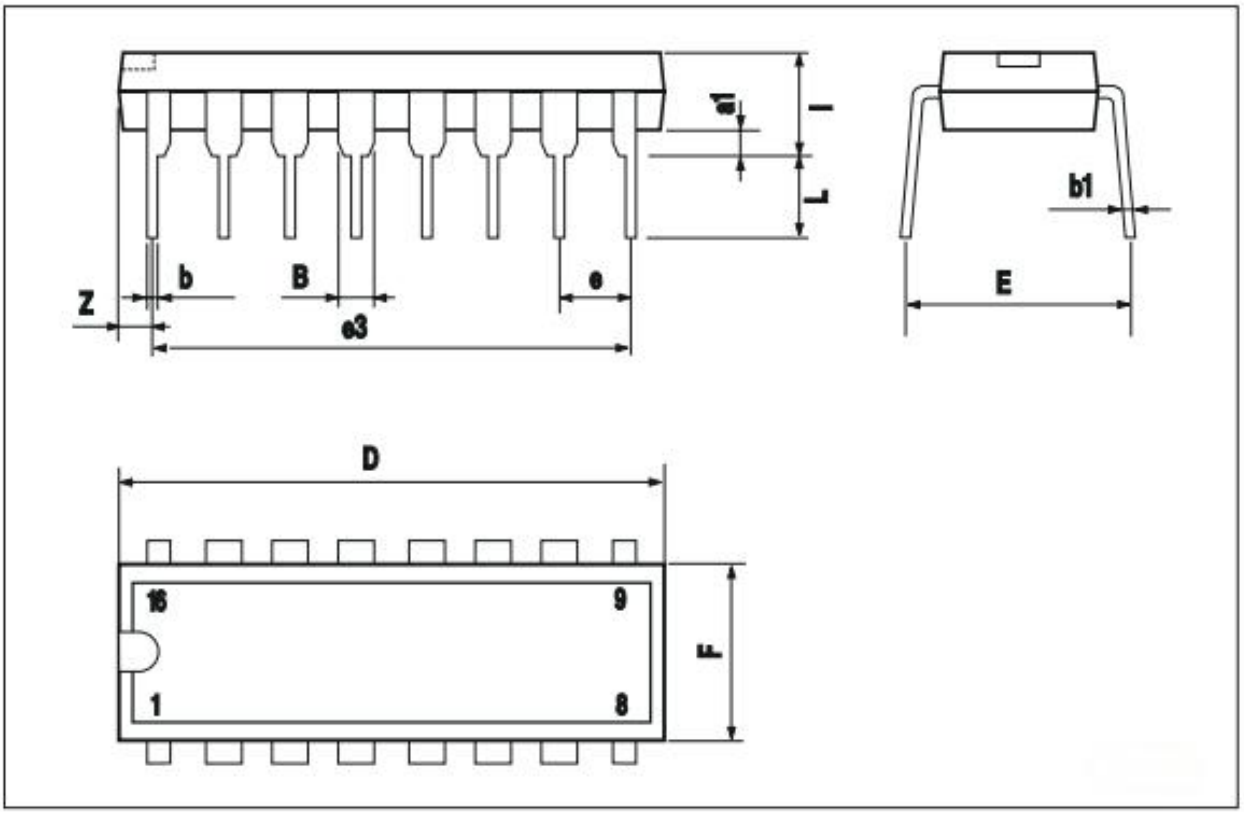
6. Ordering Information

Orderable Device	Package Type	Pins	Packing	Package Qty
74HC165ND16ATBE	DIP	16	Tube	25
74HC165NS16ARDQ	SOP	16	Tape & Reel	4000
74HC165TS16ARDQ	TSSOP	16	Tape & Reel	4000

7. Package Information

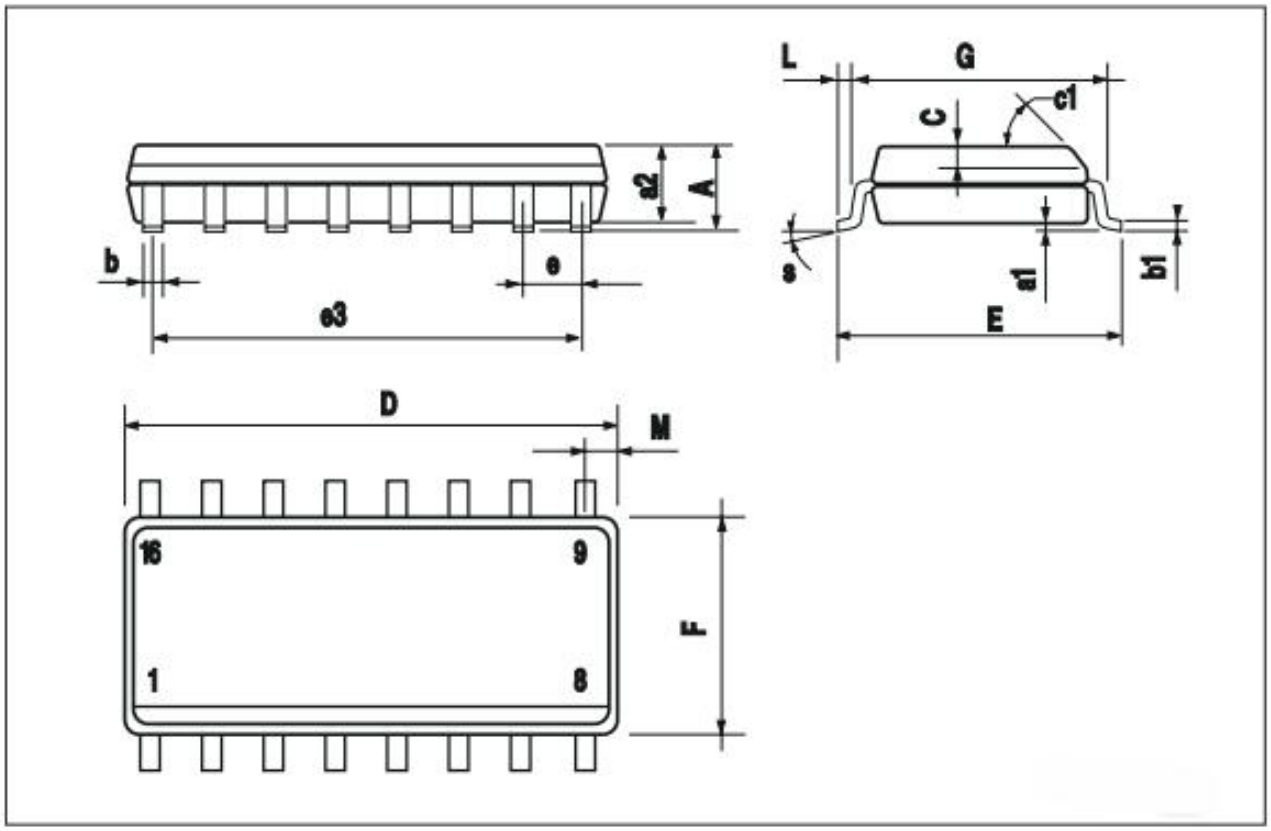
7.1 DIP16

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



7.2 SOP16

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.068
a1	0.1		0.25	0.004		0.010
a2			1.64			0.063
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



7.3 TSSOP16

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0079
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030