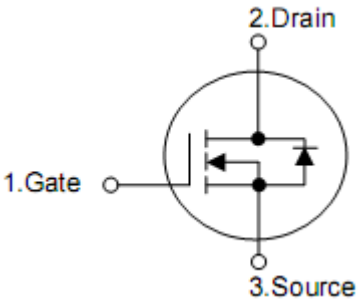
1. Features

- Uses advanced SGT technology
- $R_{DS(on)}$=4.7mΩ(typ.) @ V_{GS}=10V
- Super Low Gate Charge
- Green Device Available
- Excellent CdV/dt effect decline
- Advanced high cell density Trench technology
- 100% ΔV_{ds} TESTED
- 100% UIS TESTED

2. Pin configuration

TO-252



Pin	Function
1	Gate
2	Drain
3	Source

3. Ordering Information

Part Number	Package	Brand
KCD3008C	TO-252	KIA

4. Absolute maximum ratings

(T_A=25ºC unless otherwise specified)

Parameter		Symbol	Ratings	Unit
Drain-to-Source Voltage (V_{GS}=0V)		V_{DSS}	85	V
Gate-Source voltage (V_{DS}=0V)		V_{GS}	±20	V
Continuous Drain Current [1]	T_C=25ºC	I_D	120	A
	T_C=100ºC	I_D	99	A
Drain Current-Continuous @ Current-Pulsed [2]		$I_{DM(pulse)}$	520	A
Maximum Power Dissipation (T_C=25ºC) [4]		P_D	150	W
Avalanche energy, single pulse [3]		E_{AS}	306	mJ
Junction & Storage Temperature Range		T_J & T_{STG}	-55 to 150	ºC

5. Thermal characteristics

Parameter	Symbol	Ratings	Units
Thermal resistance, Junction-case [1]	$R_{\theta JC}$	1.0	ºC/W

6. Electrical characteristics

(T_A=25°C, unless otherwise notes)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
On/Off States							
Drain-source breakdown voltage	BV_{DSS}	V_{GS}=0V,I_D=250μA		85	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=72V, V_{GS}=0V,	T_C=25ºC	-	-	1	μA
			T_C=55ºC	-	-	5	μA
Gate leakage current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V		-	-	±100	nA
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA ,		2	3	4	V
Drain-source on-resistance 2)	$R_{DS(on)}$	V_{GS}=10V,I_D=50A		-	4.7	5.5	mΩ
Dynamic characteristics							
Gate Resistance	R_G	V_{GS}=0V,V_{DS}=0V F=1MHz		-	2.3	-	Ω
Input capacitance	C_{iss}	V_{DS}=45V,V_{GS}=0V, F=1MHz		-	3700	-	pF
Output capacitance	C_{oss}			-	650	-	pF
Reverse transfer capacitance	C_{rss}			-	25	-	pF
Switching Times							
Turn-on delay time	$t_{d(on)}$	V_{DS}=45V,V_{GS}=10V, I_D=50A,R_G=3Ω		-	20	-	ns
Rise time	t_r			-	40	-	ns
Turn-off delay time	$t_{d(off)}$			-	44	-	ns
Fall time	t_f			-	20	-	ns
Total gate charge	Q_g	V_{DS}=45V,V_{GS}=10V, I_D=50A		-	68	-	nC
Gate-source charge	Q_{gs}			-	19	-	nC
Gate-drain charge	Q_{gd}			-	17	-	nC
Source-Drain Diode Characteristics							
Source-Drain Current(Body Diode) 1),5)	I_{SD}			-	-	120	V
Diode forward voltage 2)	V_{SD}	V_{GS}=0V,I_{SD}=50A		-	-	1.2	V
Reverse recovery time	t_{rr}	T_J=25ºC I_F=20A, di/dt=100A/μs		-	67	-	ns
Reverse recovery charge	Q_{rr}			-	150	-	nC

Notes:
1) The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.
2) The data tested by pulsed , pulse width≤300us , duty cycle≤2%
3) The EAS data shows Max. rating. The test condition is V_{DD}=50V, V_{GS}=10V, L=0.5mH
4) The power dissipation is limited by 150ºC junction temperature
5) The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

7. Typical Characteristics

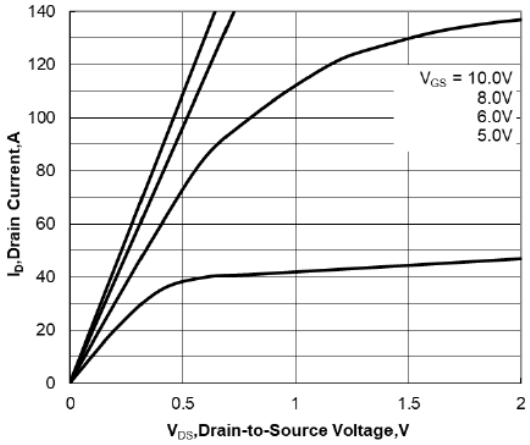


Fig1: Typical Output Characteristics

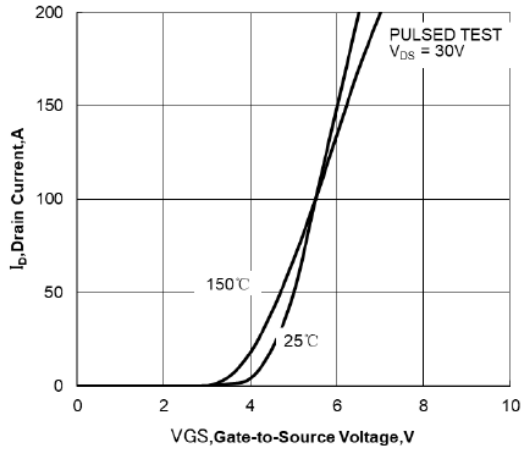


Fig 2: Typical Transfer Characteristics

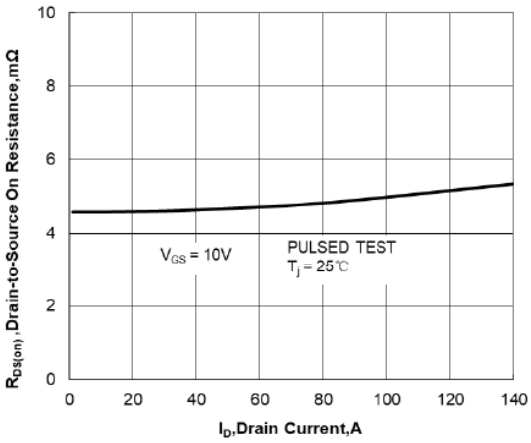


Fig 3: On-Resistance vs. Drain Current

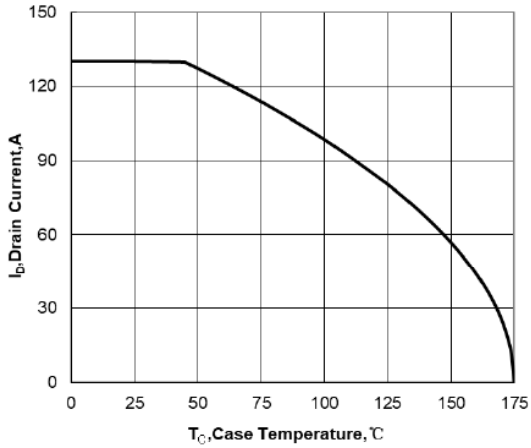


Fig 4: Maximum Continuous Drain Current vs. Case Temperature

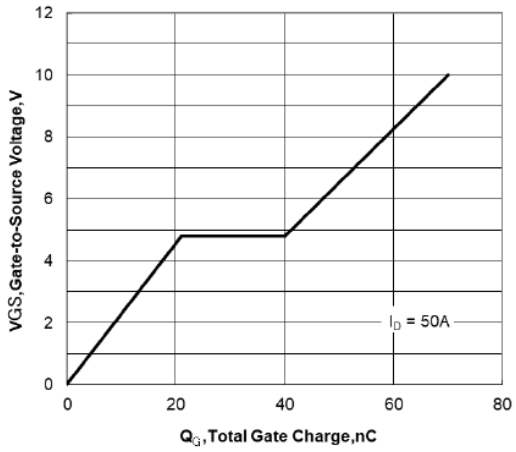


Fig 5: Gate Charge Characteristics

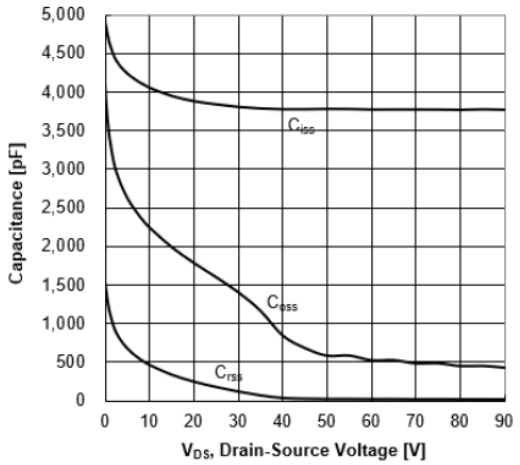


Fig 6: Capacitance Characteristics

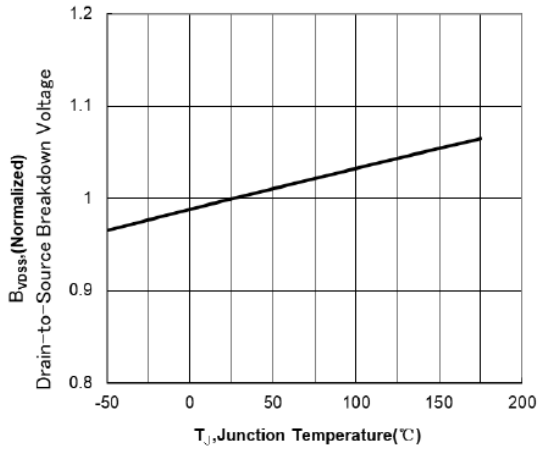


Fig 7: Normalized Breakdown Voltage vs. Junction Temperature

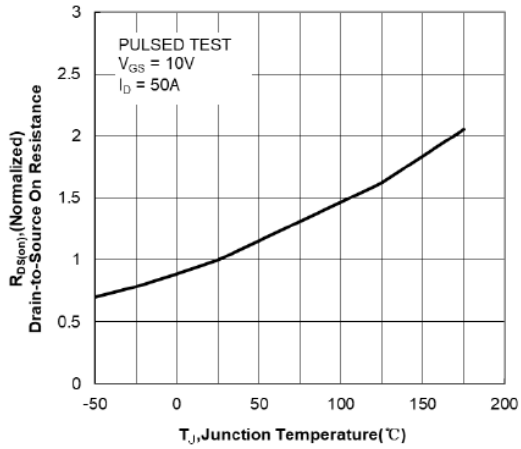


Fig 8: Normalized on Resistance vs. Junction Temperature

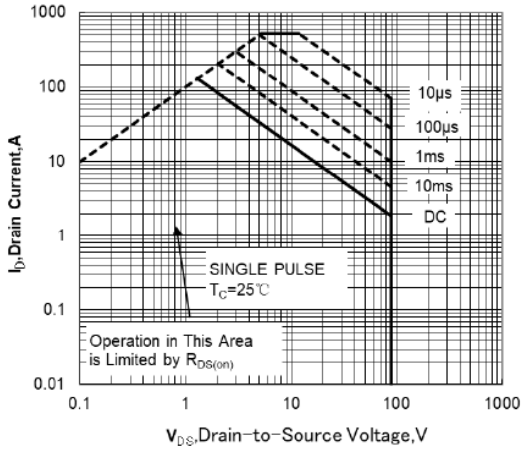


Fig 9: Maximum Safe Operating Area

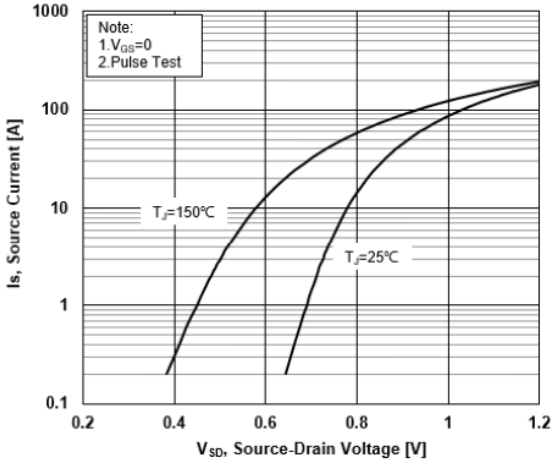


Fig 10: Body Diode Forward Characteristics

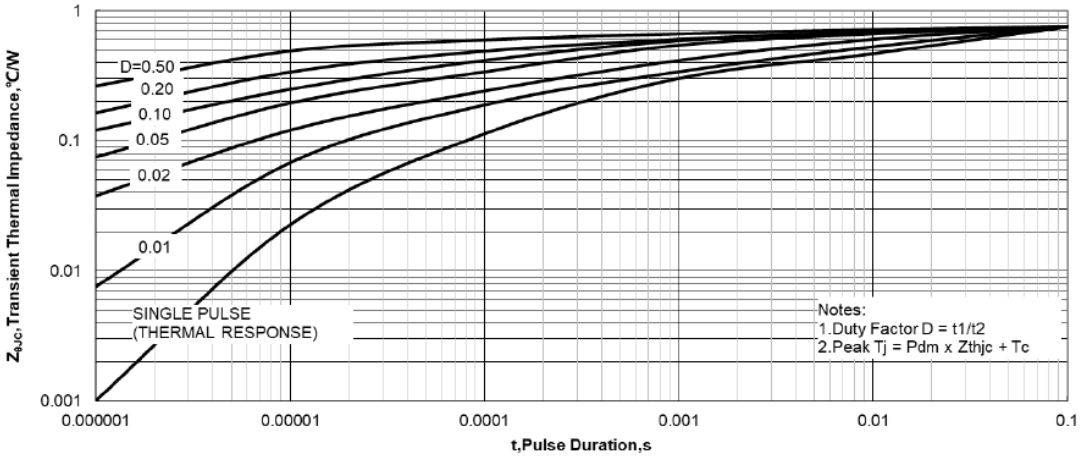


Fig.11: Maximum Effective Transient Thermal Impedance, Junction-to-Case

8. Test Circuit & Waveform

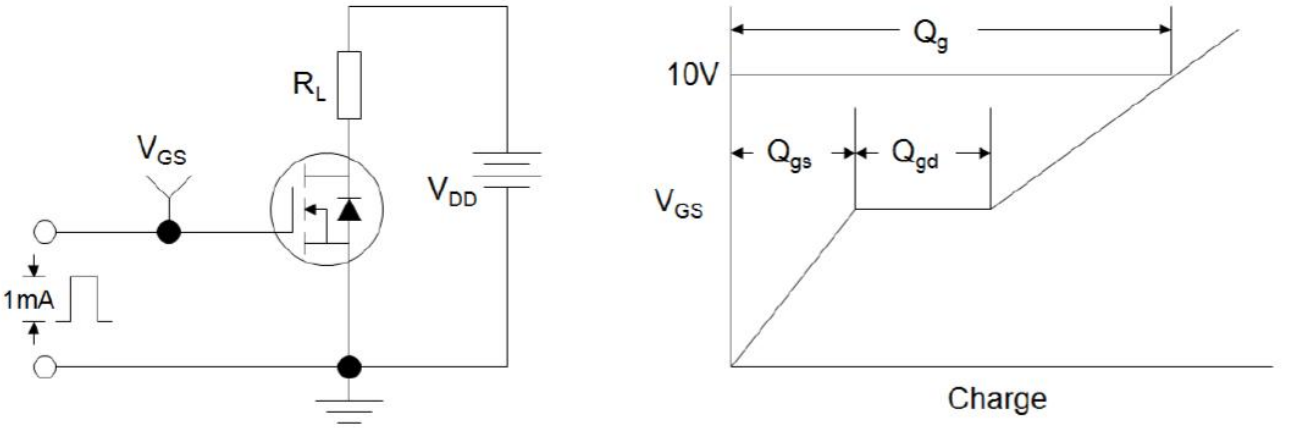


Fig 12: Gate Charge Test Circuit and Waveforms

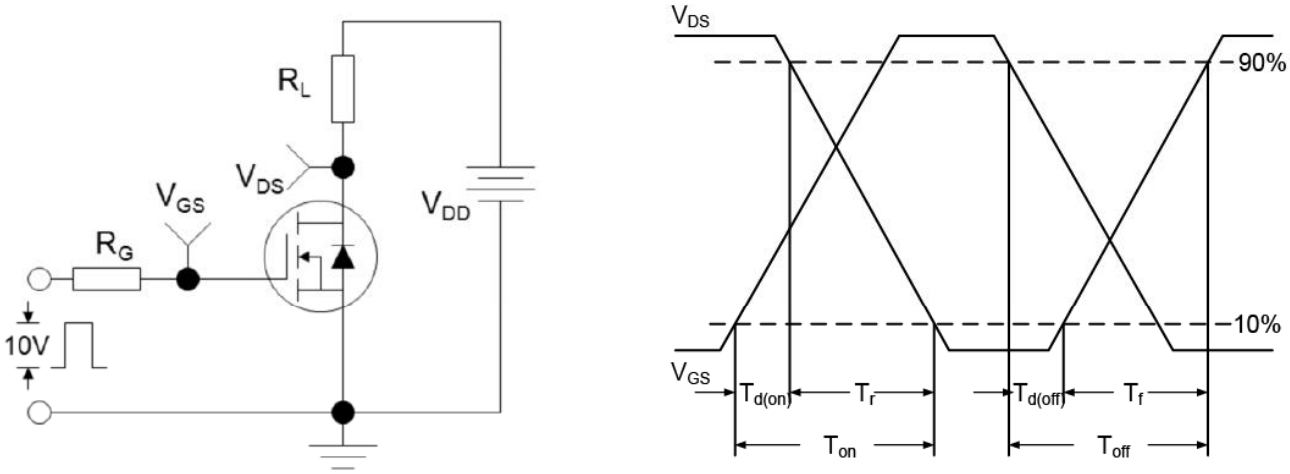


Fig 13: Resistive Switching Test Circuit and Waveforms

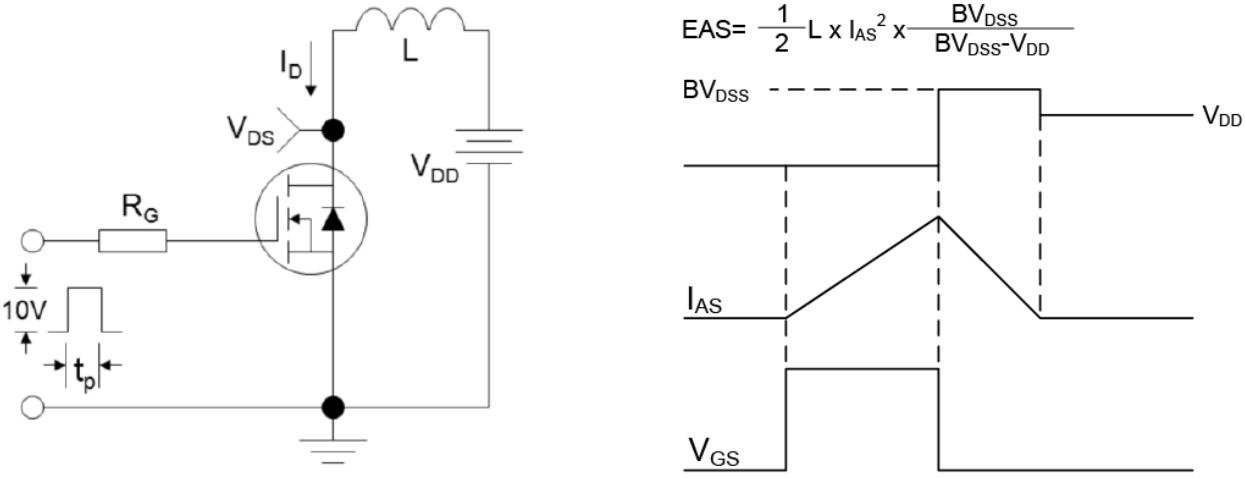


Fig 14: Unclamped Inductive Switching Test Circuit and Waveforms