1. Features

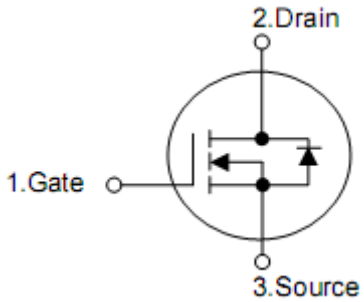
- Proprietary New Planar Technology
- $R_{DS(ON)}$=0.38Ω(typ.) @ V_{GS}=10V
- Low Gate Charge Minimize Switching Loss
- Fast Recovery Body Diode

2. Applications

- Adaptor
- TV Main Power
- SMPS Power Supply
- LCD Panel Power

3. Pin configuration

TO-220F



Pin	Function
1	Gate
2	Drain
3	Source

4. Ordering Information

Part Number	Package	Brand
KNF20N65A	TO-220F	KIA

5. Absolute maximum ratings

(T_C= 25 ºC, unless otherwise specified)

Parameter	Symbol	Ratings	Unit
Drain-to-Source Voltage [1]	V_{DSS}	650	V
Gate-to-Source Voltage	V_{GSS}	±30	V
Continuous Drain Current	I_D	20	A
Continuous Drain Current @ Tc=100ºC	$I_{D\ @\ Tc=100ºC}$	Figure 3	A
Pulsed Drain Current at V_{GS}=10V [2]	I_{DM}	Figure 6	A
Single Pulse Avalanche Energy	EAS	850	mJ
Peak Diode Recovery dv/dt [3]	dv/dt	5.0	V/ns
Power Dissipation	P_D	65	W
Derating Factor above 25ºC	P_D	0.52	W/ºC
Maximum Temperature for Soldering Leads at 0.063in (1.6mm) from Case for 10 seconds, Package Body for 10 seconds	T_L T_{PAK}	300 260	ºC
Operating and Storage Temperature Range	T_J&T_{STG}	-55 to 150	ºC

Caution: Stresses greater than those in the “Absolute Maximum Ratings” may cause permanent damage to the device.

6. Thermal characteristics

Parameter	Symbol	Ratings	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.92	ºC/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	100	ºC/W

7. Electrical characteristics

(T_J=25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-to-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250uA	650	-	-	V
Drain-to-Source Leakage Current	I_{DSS}	V_{DS}=650V, V_{GS}=0V	-	-	1	uA
		V_{DS}=520V, V_{GS}=0V T_J=125°C	-	-	100	uA
Gate-to-Source Leakage Current	I_{GSS}	V_{GS}=±30V, V_{DS}=0V	-	-	±100	nA
Drain-to-Source ON Resistance [4]	$R_{DS(ON)}$	V_{GS}=10V, I_D=10A	-	0.38	0.50	Ω
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS}=V_{GS},I_D=250uA	2.0	-	4.0	V
Forward Transconductance [4]	gfs	V_{DS}=15V,I_D=10A	-	15	-	S
Input Capacitance	C_{iss}	V_{GS}=0V,V_{DS}=25V, f=1.0MHZ	-	2500	-	pF
Reverse Transfer Capacitance	C_{oss}		-	220	-	
Output Capacitance	C_{rss}		-	34	-	
Total Gate Charge	Q_g	V_{DD}=325V,I_D=20A, V_{GS}=0 to 10V	-	62	-	nC
Gate-to-Source Charge	Q_{gs}		-	10	-	
Gate-to-Drain (Miller) Charge	Q_{gd}		-	23	-	
Turn-on Delay Time	$t_{d(ON)}$	V_{DD}=325V, I_D=20A, R_G=25Ω,V_{GS}=10V	-	32	-	nS
Rise Time	t_{rise}		-	180	-	
Turn-Off Delay Time	$t_{d(OFF)}$		-	71	-	
Fall Time	t_{fall}		-	120	-	
Continuous Source Current [4]	I_{SD}	Integral PN-diode in MOSFET	-	-	20	A
Pulsed Source Current [4]	I_{SM}		-	-	80	A
Forward Voltage	V_{SD}	I_S=20A, V_{GS}=0V	-	-	1.5	V
Reverse recovery time	t_{rr}	I_F=20A, V_{GS}=0V di/dt=100A/us,	-	800	-	ns
Reverse recovery charge	Q_{rr}		-	3.5	-	uC

Note:
1) T_J=+25°C to +150°C
2) Repetitive rating; pulse width limited by maximum junction temperature.
3) I_{SD}=20A, di/dt<100A/us, V_{DD}<BV_{DSS}, T_J=+150°C.
4) Pulse width≤380us; duty cycle≤2%.

8. Typical Characteristics

Figure 1. Maximum Effective Thermal Impedance, Junction-to-Case

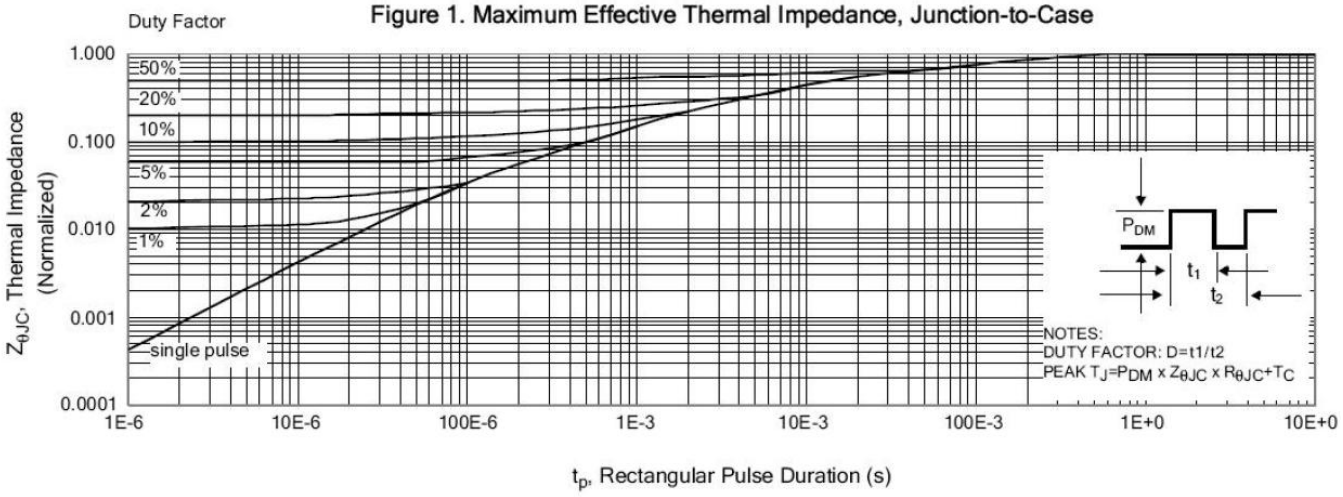


Figure 2. Maximum Power Dissipation vs Case Temperature

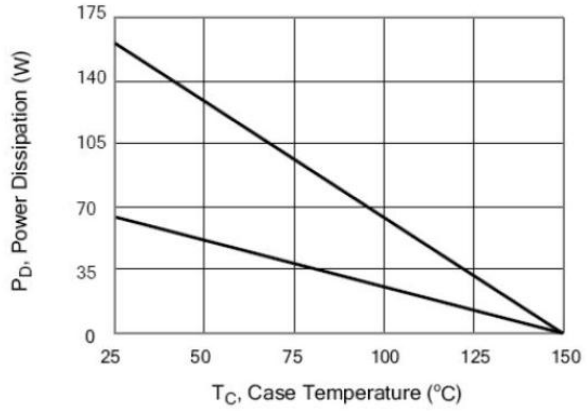


Figure 3. Maximum Continuous Drain Current vs Case Temperature

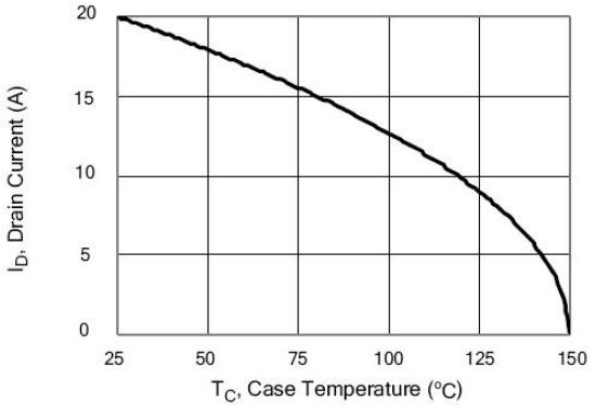


Figure 4. Typical Output Characteristics

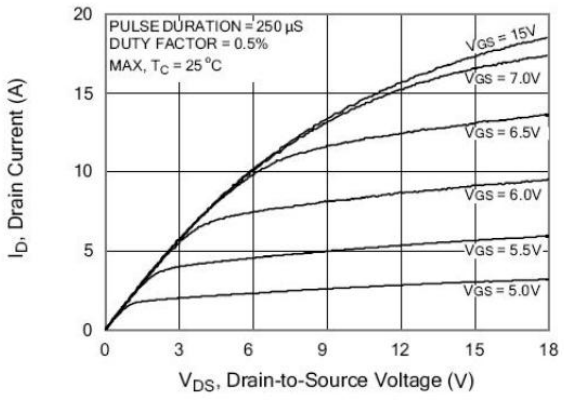


Figure 5. Typical Drain-to-Source ON Resistance vs Gate Voltage and Drain Current

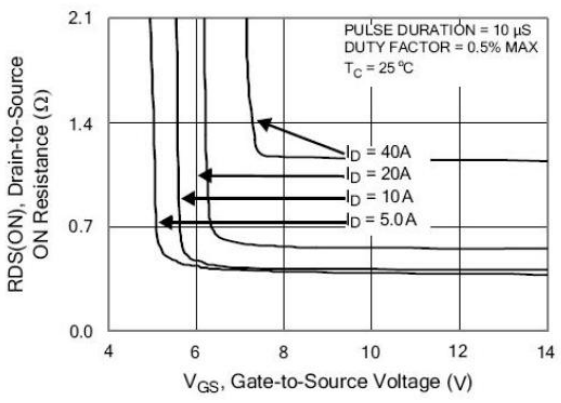


Figure 6. Maximum Peak Current Capability

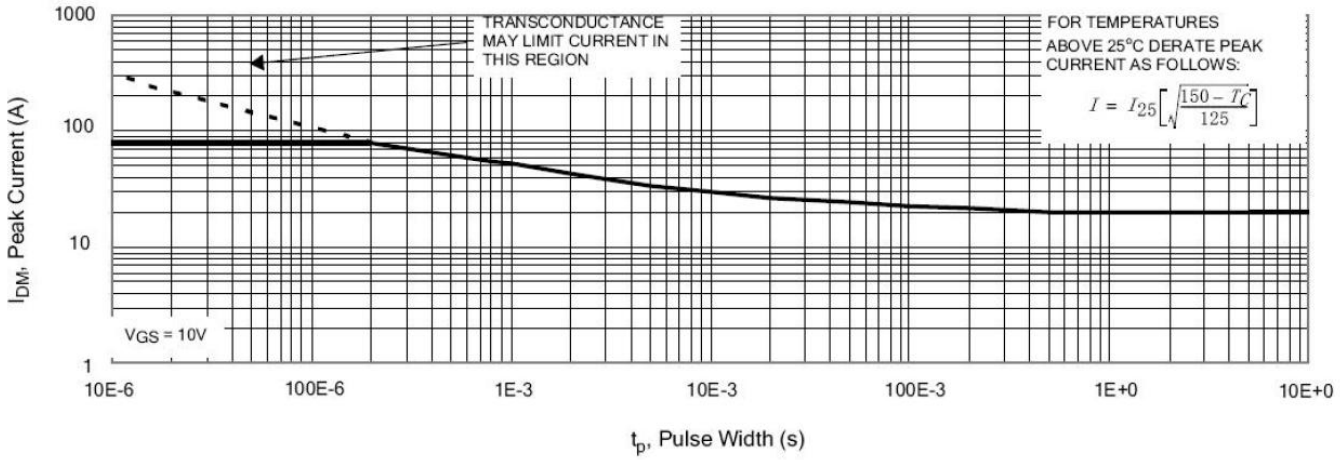


Figure 7. Typical Transfer Characteristics

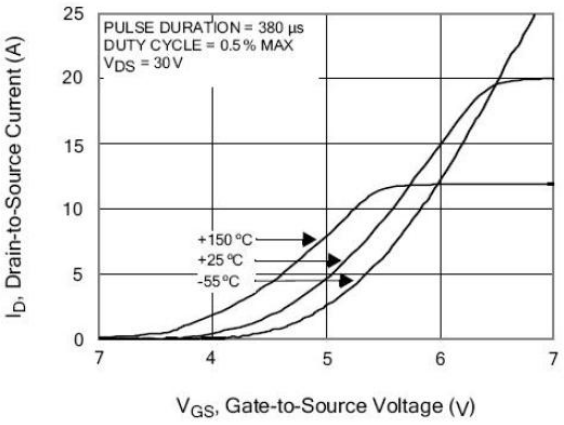


Figure 8. Unclamped Inductive Switching Capability

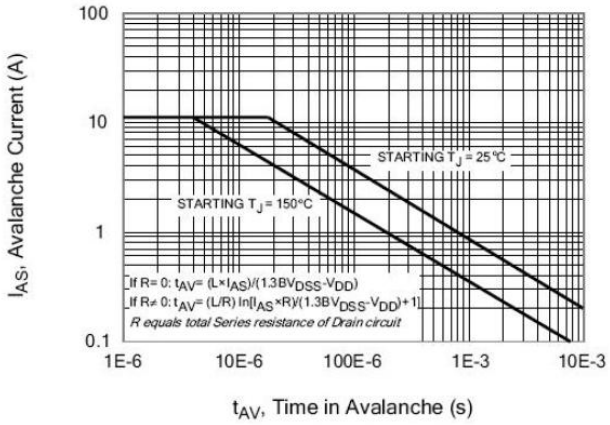


Figure 9. Typical Drain-to-Source ON Resistance vs Drain Current

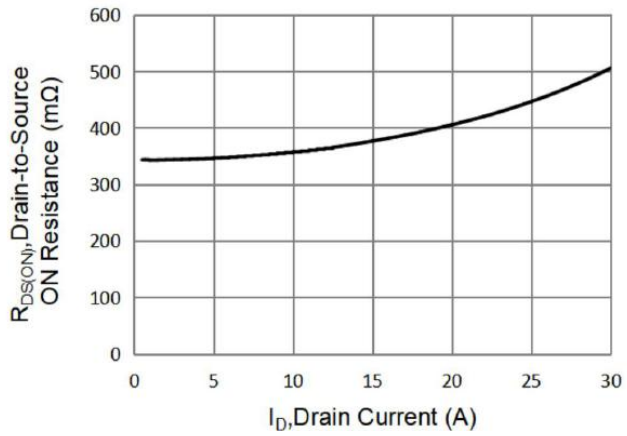


Figure 10. Typical Drain-to-Source ON Resistance vs Junction Temperature

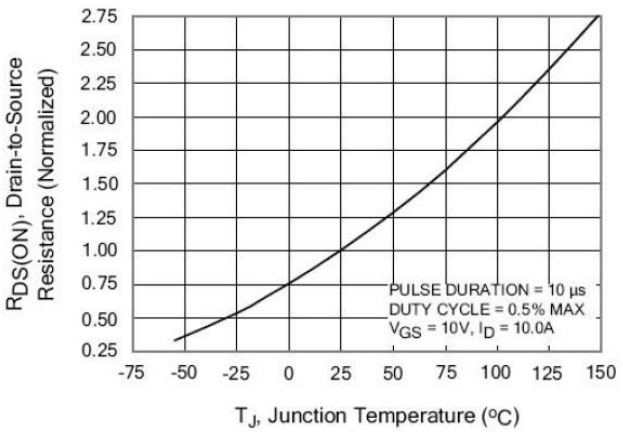


Figure 11. Typical Breakdown Voltage vs Junction Temperature

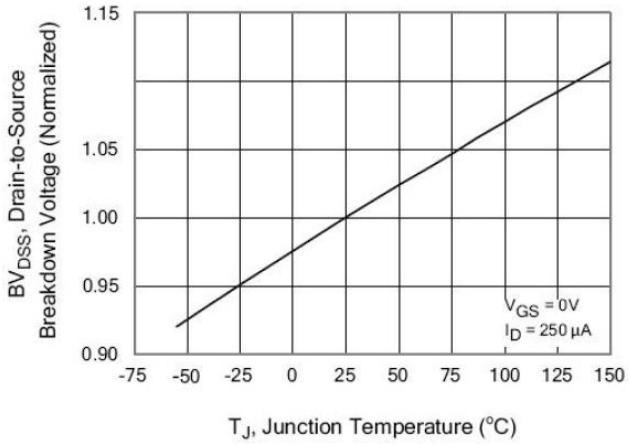


Figure 12. Typical Threshold Voltage vs Junction Temperature

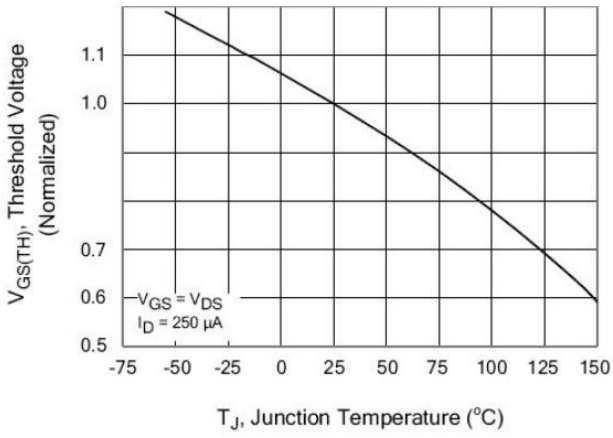


Figure 13. Maximum Forward Bias Safe Operating Area

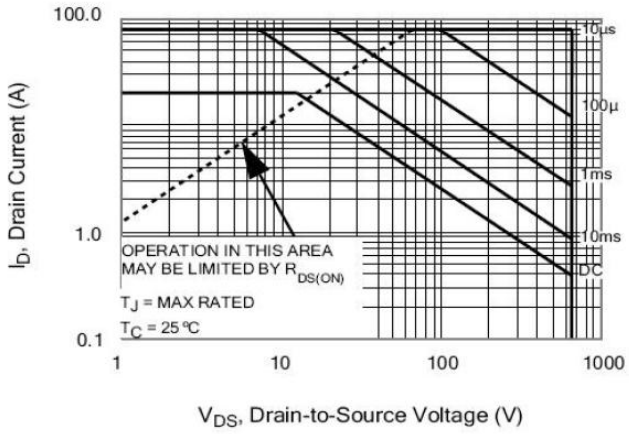


Figure 14. Capacitance vs Vds

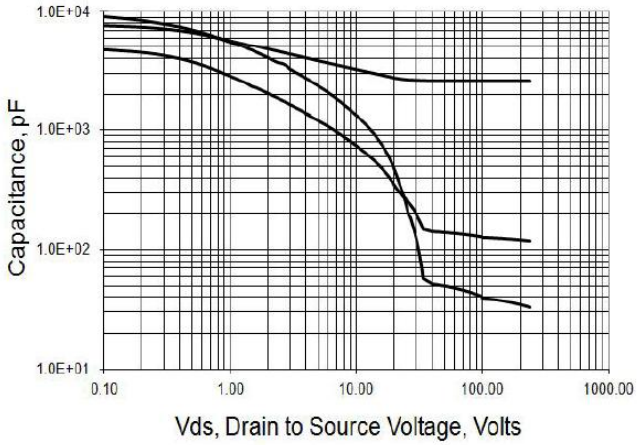


Figure 15 .Typical Gate Charge

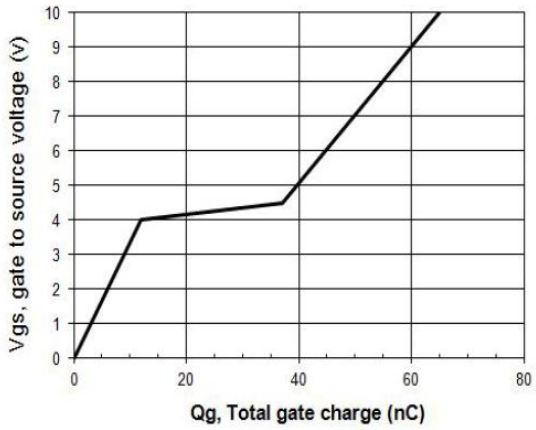
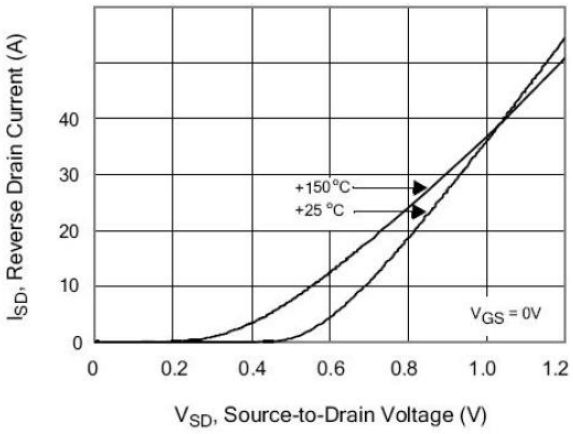


Figure 16. Typical Body Diode Transfer Characteristics



9. Test Circuits and Waveforms

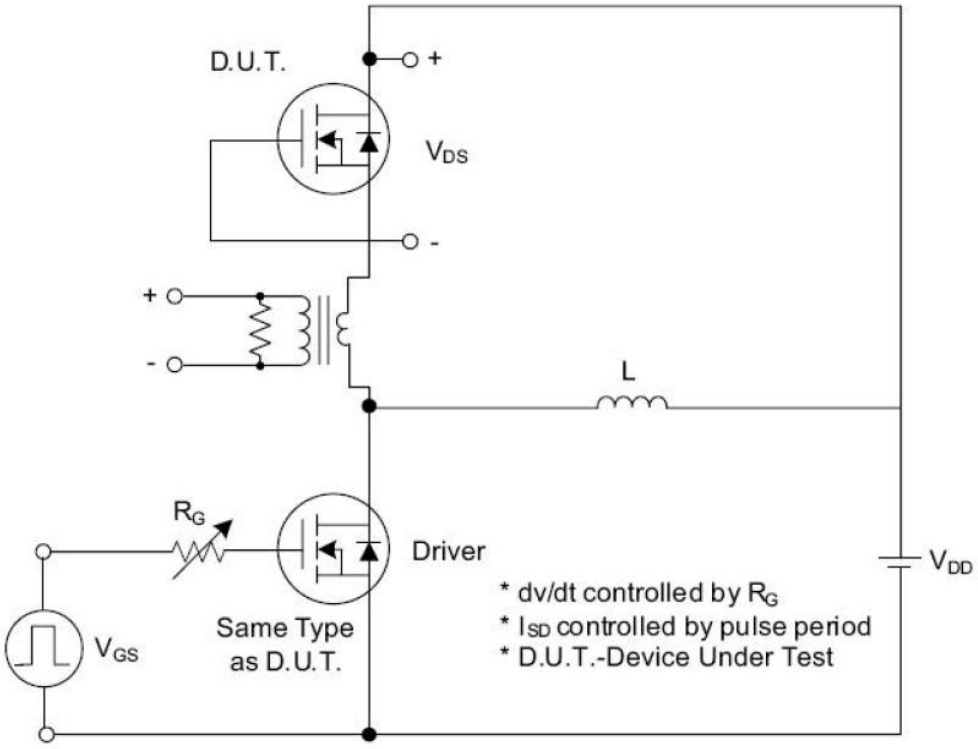


Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit

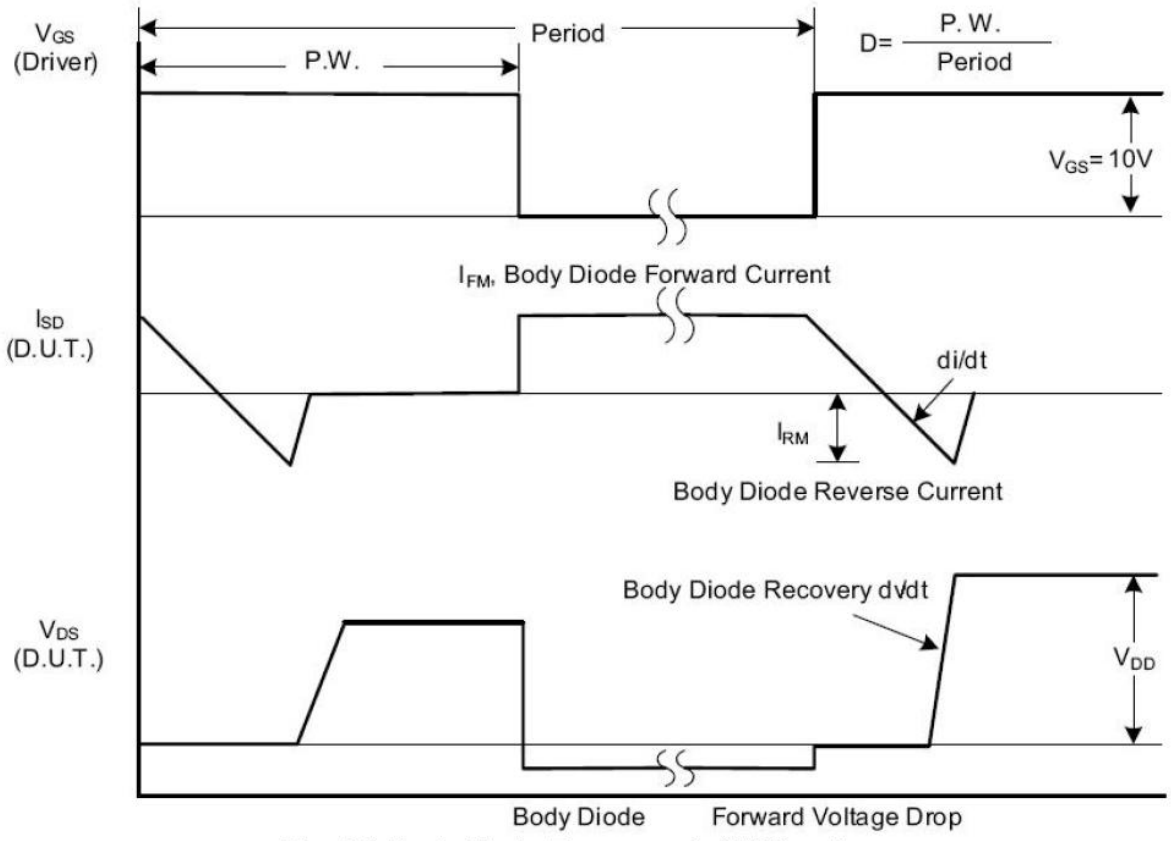


Fig. 1.2 Peak Diode Recovery dv/dt Waveforms

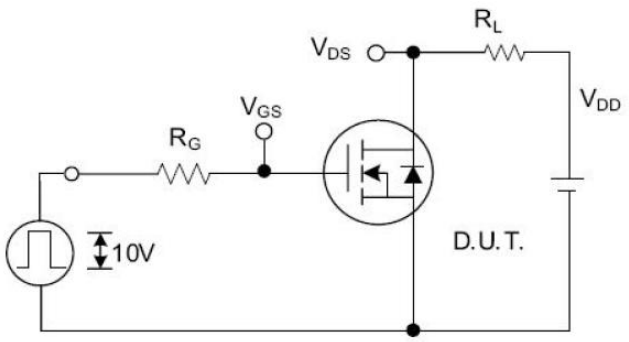


Fig. 2.1 Switching Test Circuit

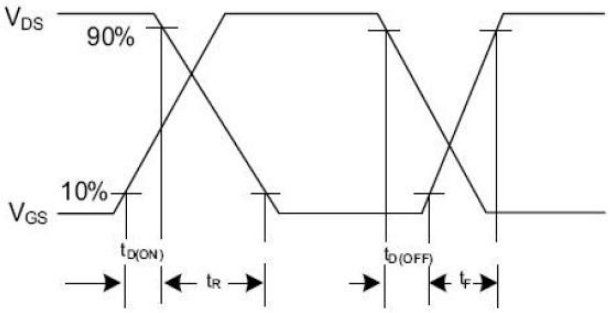


Fig. 2.2 Switching Waveforms

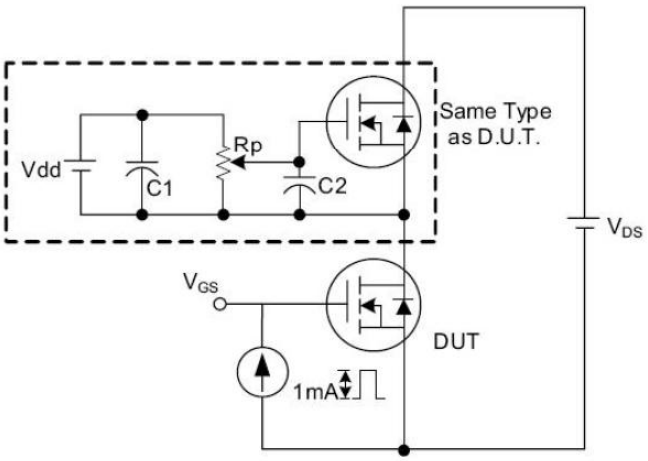


Fig. 3 . 1 Gate Charge Test Circuit

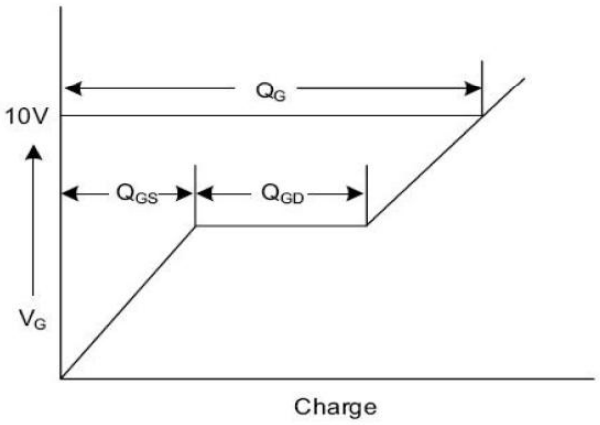


Fig. 3 . 2 Gate Charge Waveform

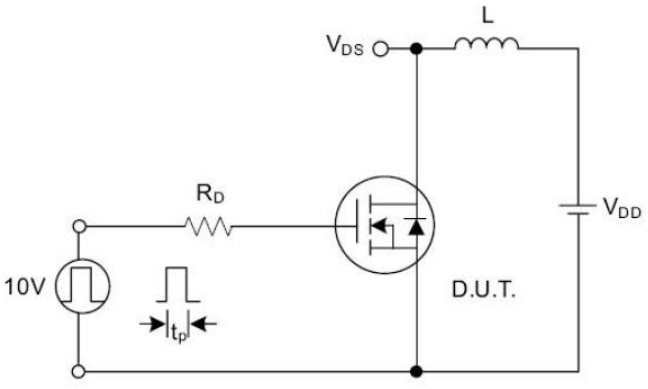


Fig. 4.1 Unclamped Inductive Switching Test Circuit

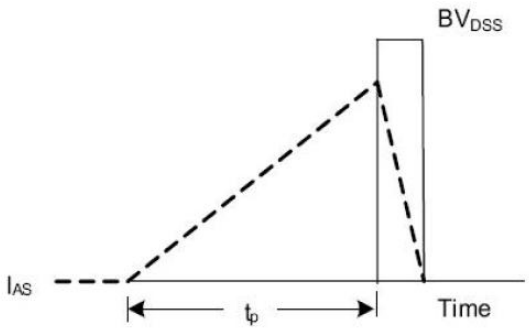


Fig. 4.2 Unclamped Inductive Switching Waveforms