

Product Summary

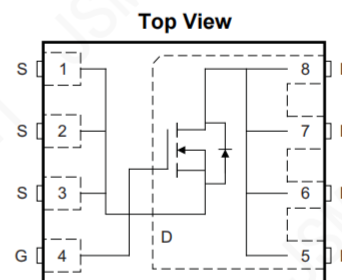
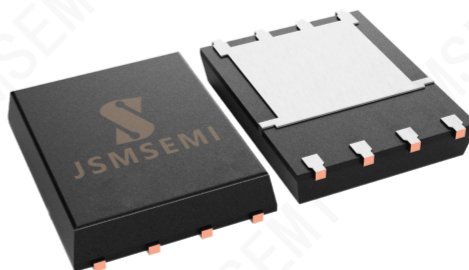
- V_{DS} 40V
- I_D 150A
- $R_{DS(ON)}$ (at $V_{GS}=10V$) <2.2m Ω
- 100% EAS Tested
- 100% ∇V_{DS} Tested

General Description

- Trench Power MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Power switching application
- Uninterruptible power supply
- DC-DC convertor



Absolute Maximum Ratings (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Rating	Unit
Common Ratings			
V_{DSS}	Drain-Source Voltage	40	V
V_{GSS}	Gate-Source Voltage	±20	
I_D^G	Continuous Drain Current	T _C =25°C	150 ^G
		T _C =25°C	205 ^I
		T _C =100°C	100 ^G
I_{DM}^C	Pulsed Drain Current	620	A
I_{DSM}	Continuous Drain Current	T _A =25°C	40
		T _A =70°C	32
P_D^B	Power Dissipation	T _C =25°C	157
		T _C =100°C	62
I_S^G	Diode Continuous Forward Current	150	A
T _{STG} , T _J	Storage Temperature Range	-55 to 150	°C
P_{DSM}	Power Dissipation	T _A =25°C	6.2
		T _A =70°C	4
I_{AS}^C	Single pulsed avalanche Current	47	A
E_{AS}^C	Single pulsed avalanche energy	L=0.3mH	331
$R_{\theta JC}$	Thermal Resistance-Junction to Case	0.8	°C/W
$R_{\theta JA}^{AD}$	Thermal Resistance-Junction to Ambient	t≤10S	20
		Steady State	50

Electrical Characteristics ($T_J=25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	40			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=40\text{V}$, $V_{GS}=0\text{V}$ $T_J=55^{\circ}\text{C}$			1 5	μA
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}$, $V_{GS}=\pm 20\text{V}$			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	1	1.7	2.5	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}$, $I_D=50\text{A}$ $T_J=125^{\circ}\text{C}$		1.5 2.25	2.2 3	m Ω
		$V_{GS}=4.5\text{V}$, $I_D=20\text{A}$		2.2	3.5	
g_{FS}	Forward Transconductance	$V_{DS}=5\text{V}$, $I_D=20\text{A}$		100		S
V_{SD}	Diode Forward Voltage	$I_S=1\text{A}$, $V_{GS}=0\text{V}$		0.7	1	V
I_S	Maximum Body-Diode Continuous Current ^G				150	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}$, $V_{DS}=20\text{V}$, $f=1\text{MHz}$		3200		pF
C_{oss}	Output Capacitance			1600		pF
C_{rss}	Reverse Transfer Capacitance			75		pF
R_g	Gate resistance	$f=1\text{MHz}$	1	2	3.1	Ω
SWITCHING PARAMETERS						
$Q_g(10\text{V})$	Total Gate Charge	$V_{GS}=10\text{V}$, $V_{DS}=20\text{V}$, $I_D=20\text{A}$		46		nC
$Q_g(4.5\text{V})$	Total Gate Charge			23		nC
Q_{gs}	Gate Source Charge			6.2		nC
Q_{gd}	Gate Drain Charge			6.5		nC
Q_{oss}	Output Charge	$V_{GS}=0\text{V}$, $V_{DS}=20\text{V}$		28		nC
$t_{D(on)}$	Turn-On DelayTime	$V_{GS}=10\text{V}$, $V_{DS}=20\text{V}$, $R_L=1\Omega$, $R_{GEN}=3\Omega$		12.5		ns
t_r	Turn-On Rise Time			9.5		ns
$t_{D(off)}$	Turn-Off DelayTime			57.5		ns
t_f	Turn-Off Fall Time			10.5		ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=20\text{A}$, $di/dt=500\text{A}/\mu\text{s}$		20		ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=20\text{A}$, $di/dt=500\text{A}/\mu\text{s}$		60		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^{\circ}\text{C}$. The Power dissipation P_{DSM} is based on $R_{\theta JA} \leq 10\text{s}$ and the maximum allowed junction temperature of 150°C . The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on $T_{J(MAX)}=150^{\circ}\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Single pulse width limited by junction temperature $T_{J(MAX)}=150^{\circ}\text{C}$.

D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using $<300\mu\text{s}$ pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}=150^{\circ}\text{C}$. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^{\circ}\text{C}$.

I. The maximum current rating is silicon limited

Ordering Information

Order number	Package	Marking	Operation Temperature Range	MSL Grade	Ship, Quantity	Green
SH0403BQ-JSM	DFN5060-8L	SH0403BQ	-55 to 150°C	1	T&R,5000	Rohs

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

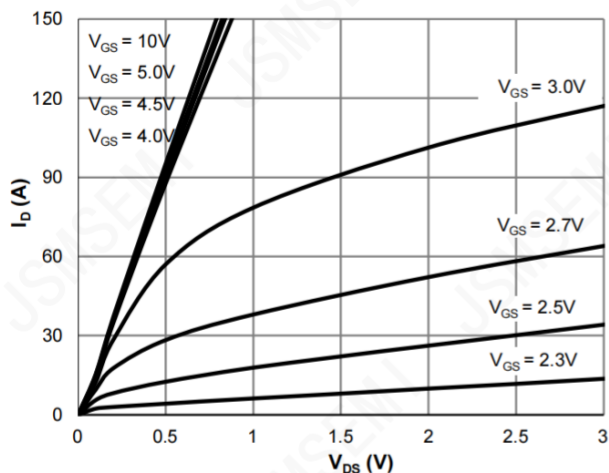


Figure 1: Saturation Characteristics

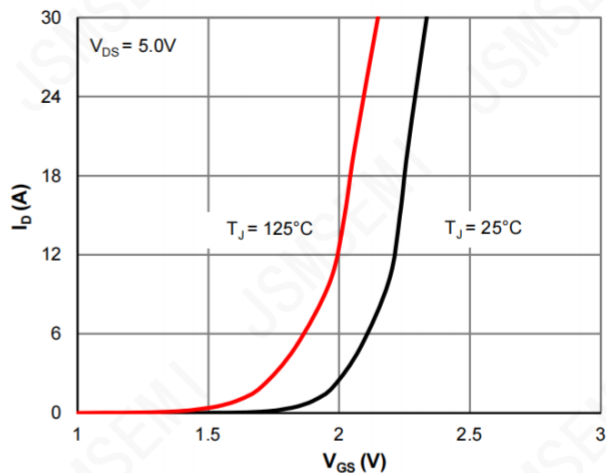


Figure 2: Transfer Characteristics

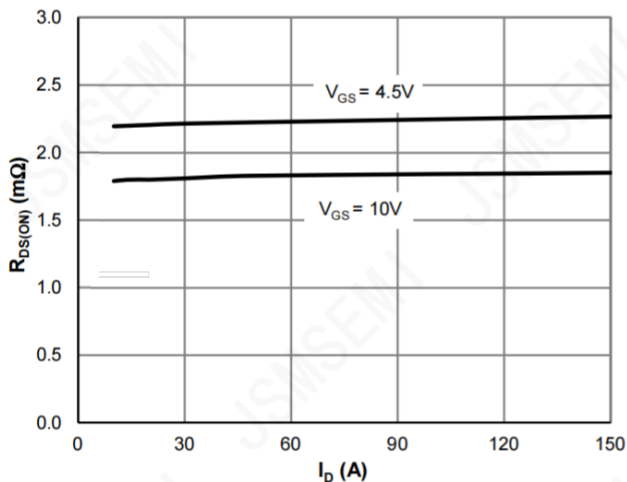


Figure 3: $R_{DS(ON)}$ vs. Drain Current

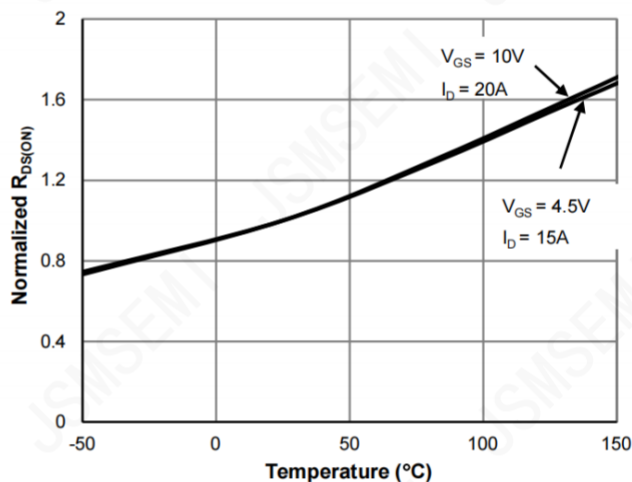


Figure 4: $R_{DS(ON)}$ vs. Junction Temperature

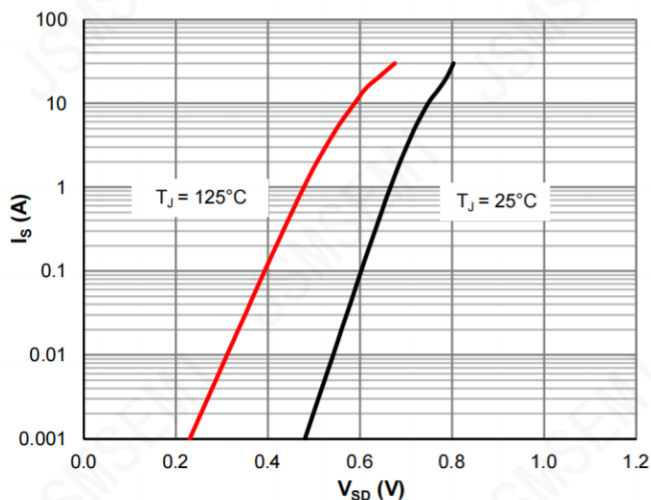


Figure 5: Body-Diode Characteristics

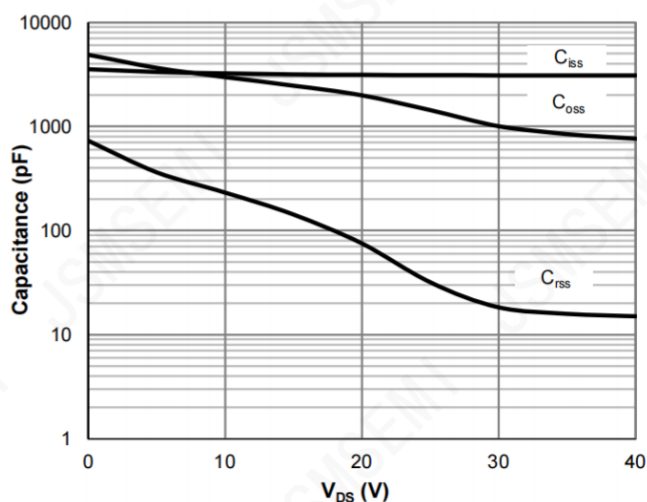


Figure 6: Capacitance Characteristics

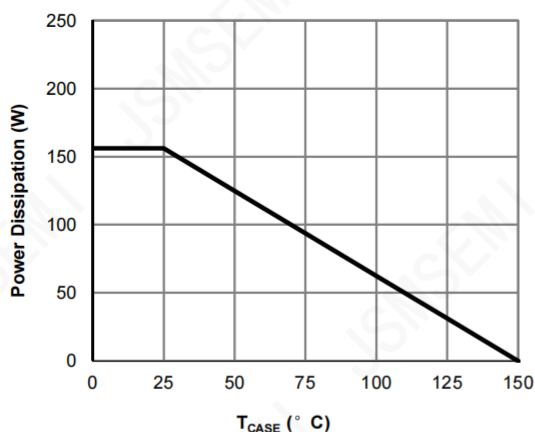


Figure 7: Power De-rating (Note F)

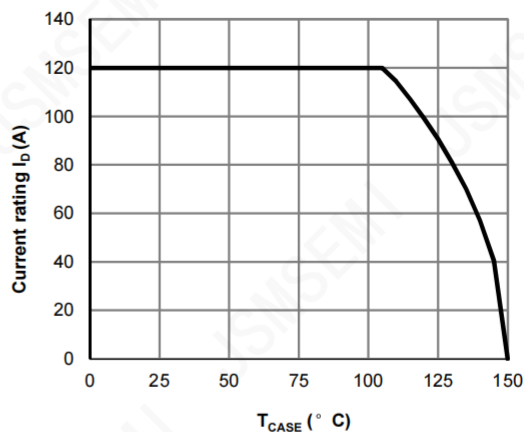


Figure 8: Current De-rating (Note F)

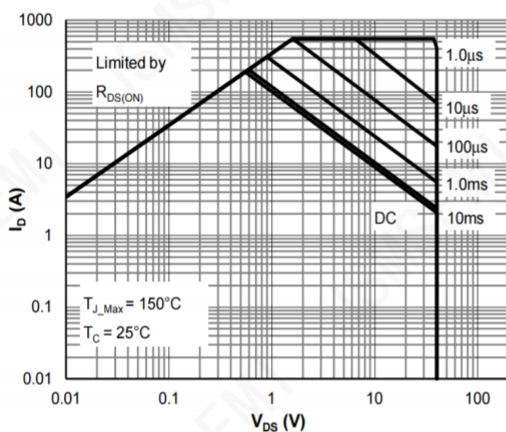


Figure 9: Maximum Safe Operating Area

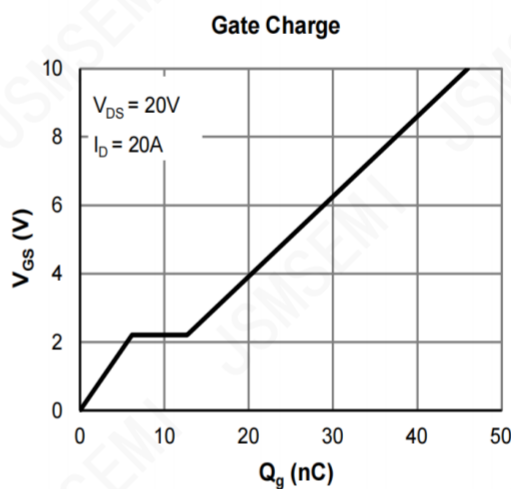


Figure 10: Gate Charge

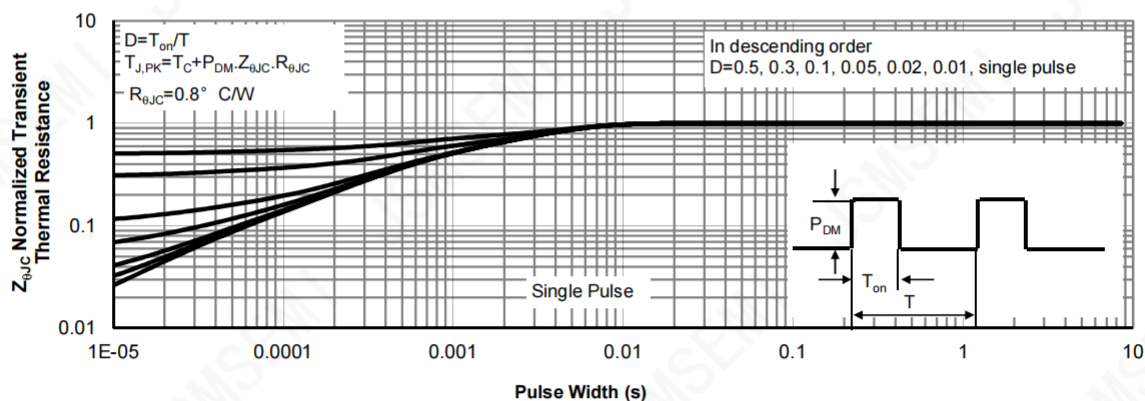


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

Figure A: Gate Charge Test Circuit & Waveforms

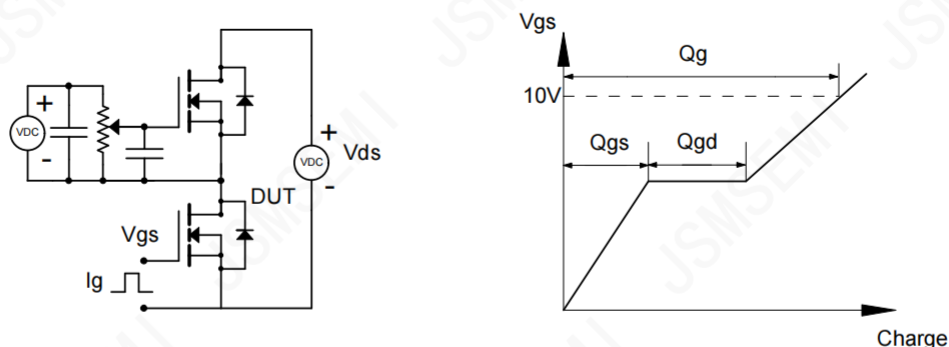


Figure B: Resistive Switching Test Circuit & Waveforms

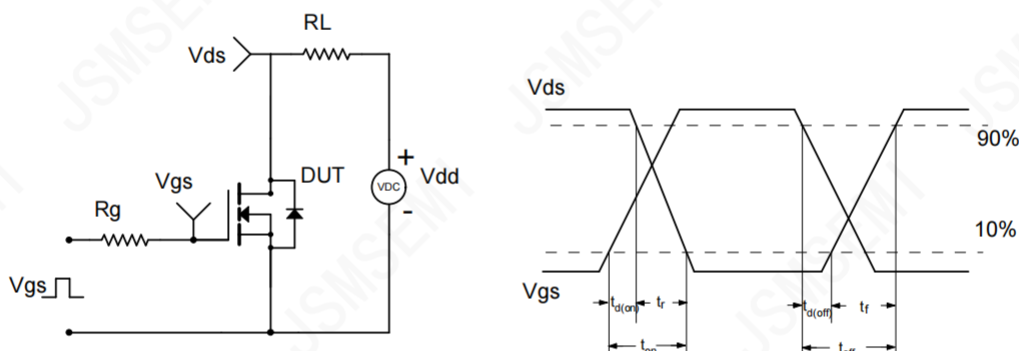


Figure C: nclamped Inductive Switching (UIS) Test Circuit & Waveforms

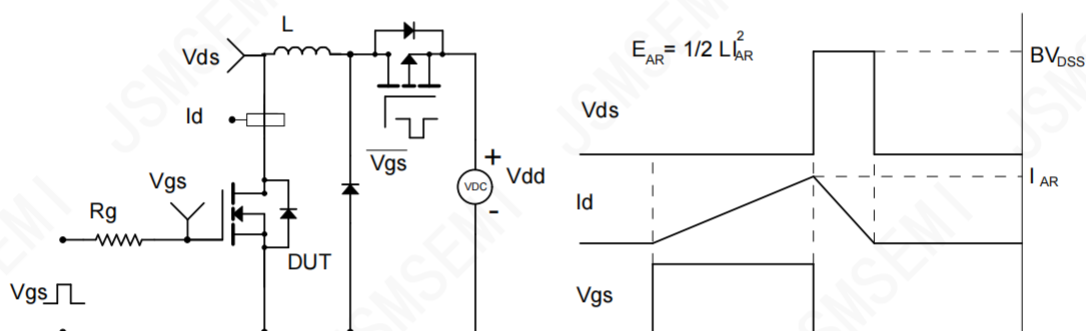
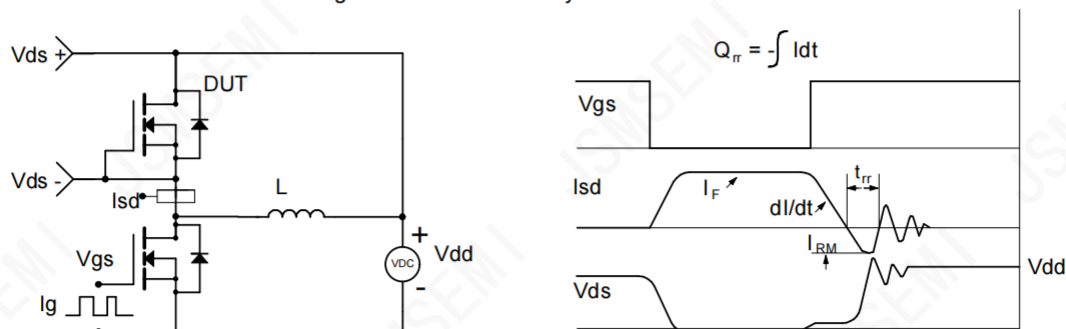
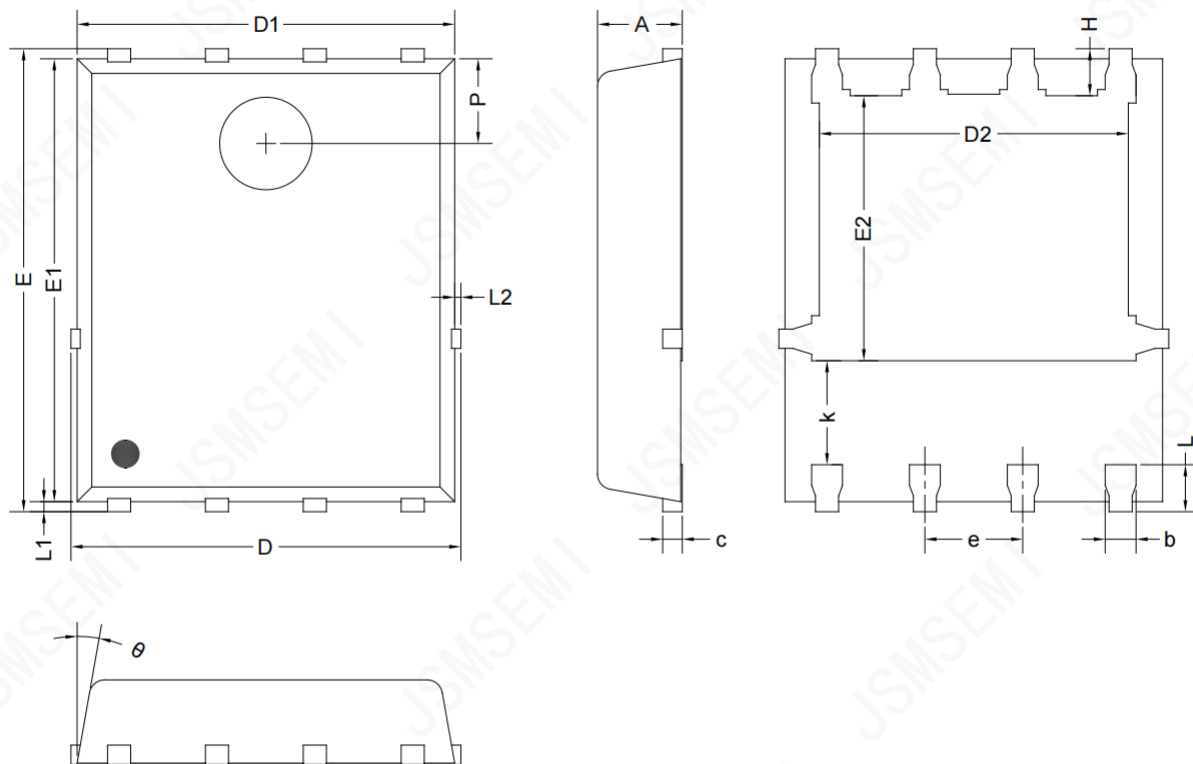


Figure D: Diode Recovery Test Circuit & Waveforms



Package Information

DFN5060-8L



Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	1.000	1.100	1.200
b	0.350	0.400	0.450
c	0.210	0.250	0.340
D	4.800	-	5.100
D1	4.800	4.900	5.000
D2	3.910	4.010	4.110
E	5.900	6.000	6.100
E1	5.700	5.750	5.800
E2	3.340	3.440	3.540
e	1.270 BSC		
H	0.510	0.610	0.710
k	1.100	-	-
L	0.510	0.610	0.710
L1	0.060	0.130	0.200
L2	-	-	0.100
P	1.000	1.100	1.200
θ	8°	10°	12°

NOTE: This drawing is subject to change without notice.

Revision History

Rev.	Change	Date
V1.0	Initial version	6/27/2021

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