Product Summary

$V_{(BR)DSS}$	$R_{DS(on)TYP}$	I_D
60V	36mΩ@10V	4.5A

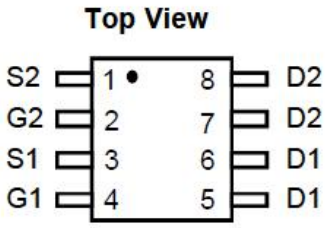
Feature

- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high EAS
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

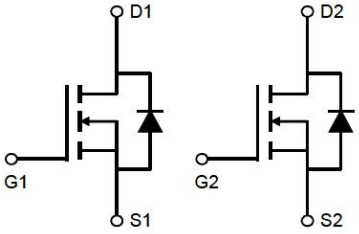
- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

Package

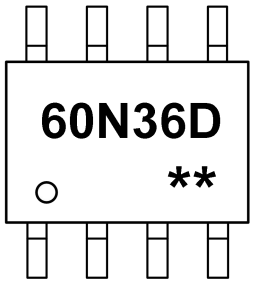


SOP-8

Circuit diagram



Marking



60N36D =Device Code
**** =Week Code**

Absolute maximum ratings (Ta=25℃ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain Current	I_D	4.5	A
Pulsed Drain Current[1)]	I_{DM}	20	A
Power Dissipation	P_D	2	W
Thermal Resistance from Junction to Ambient[2)]	$R_{\theta JA}$	62.5	℃/W
Junction Temperature	T_J	150	℃
Storage Temperature	T_{STG}	-55~ +150	℃

Electrical characteristics (T_A=25 °C, unless otherwise noted)

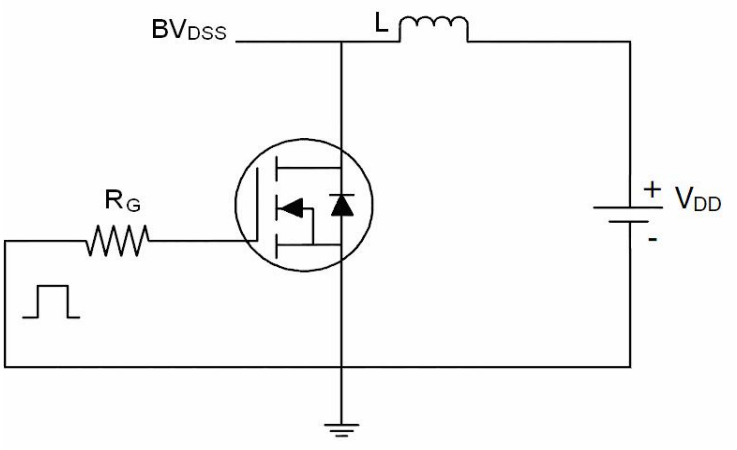
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	60	69	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=60V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics [(3)]						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	1.2	2.0	2.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=4.5A	-	36	45	mΩ
Forward Transconductance	g_{FS}	V_{DS}=5V,I_D=4.5A	11	-	-	S
Dynamic Characteristics [(4)]						
Input Capacitance	C_{lss}	V_{DS}=25V,V_{GS}=0V, F=1.0MHz	-	450	-	PF
Output Capacitance	C_{oss}		-	60	-	PF
Reverse Transfer Capacitance	C_{rss}		-	25	-	PF
Switching Characteristics [(4)]						
Turn-on Delay Time	$t_{d(on)}$	V_{DS}=30V,I_D=4.5A V_{GS}=10V,R_{GEN}=3Ω	-	4.7	-	nS
Turn-on Rise Time	t_r		-	2.3	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	15.7	-	nS
Turn-Off Fall Time	t_f		-	1.9	-	nS
Total Gate Charge	Q_g	V_{DS}=30V,I_D=4.5A, V_{GS}=10V	-	8.5	-	nC
Gate-Source Charge	Q_{gs}		-	1.6	-	nC
Gate-Drain Charge	Q_{gd}		-	2.2	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage [(3)]	V_{SD}	V_{GS}=0V,I_S=4.5A	-	-	1.2	V
Reverse Recovery Time	t_{rr}	T_J = 25°C, I_F =4.5A d_i/d_t = 100A/μs[(3)]	-	25	-	nS
Reverse Recovery Charge	Q_{rr}		-	35	-	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

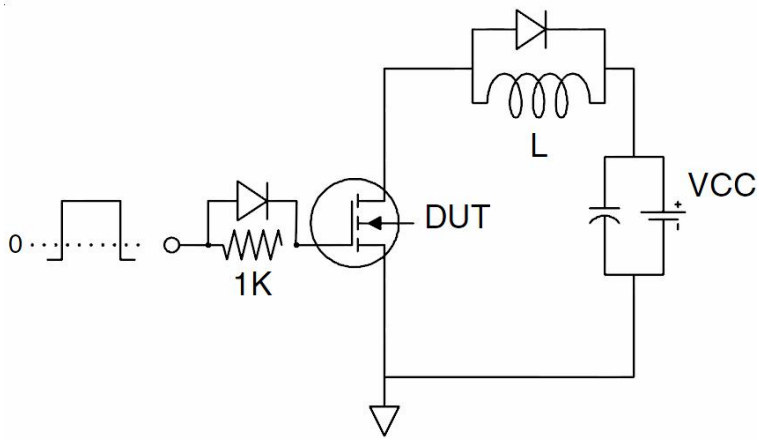
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production

Test Circuits

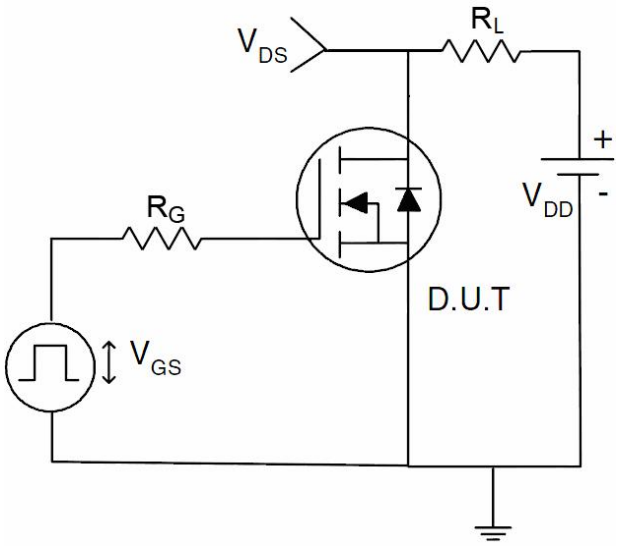
1) EAS Test Circuits



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Characteristics

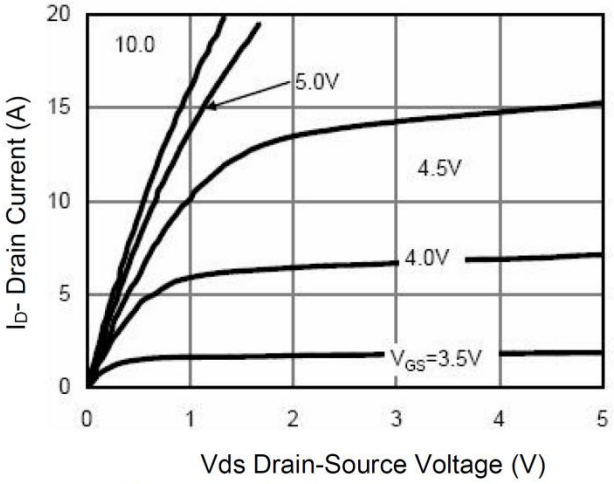


Figure 1 Output Characteristics

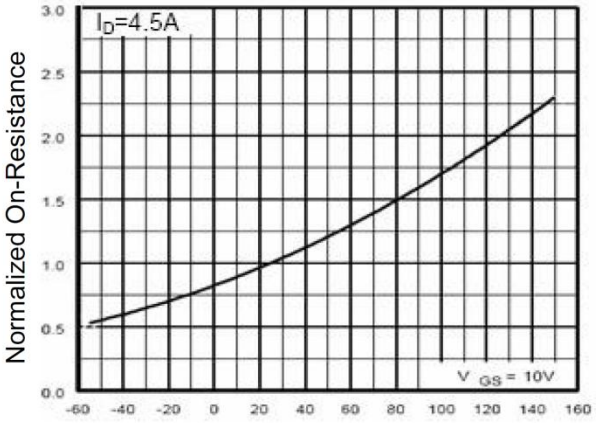


Figure 4 Rdson-JunctionTemperature

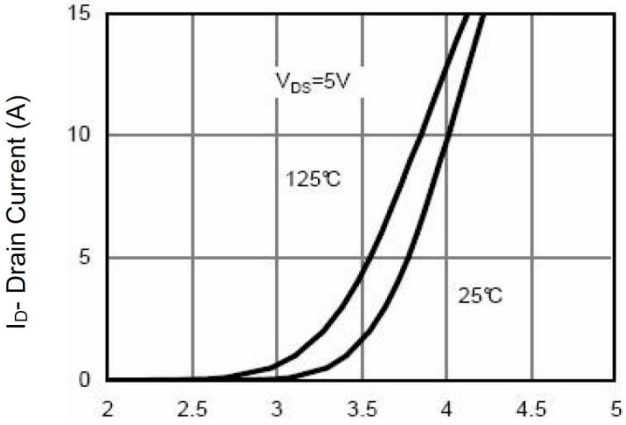


Figure 2 Transfer Characteristics

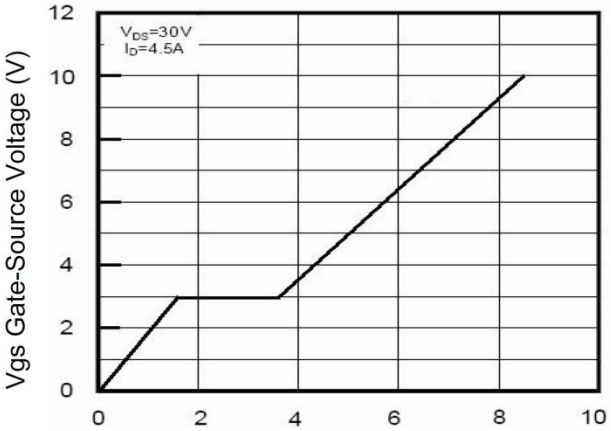


Figure 5 Gate Charge

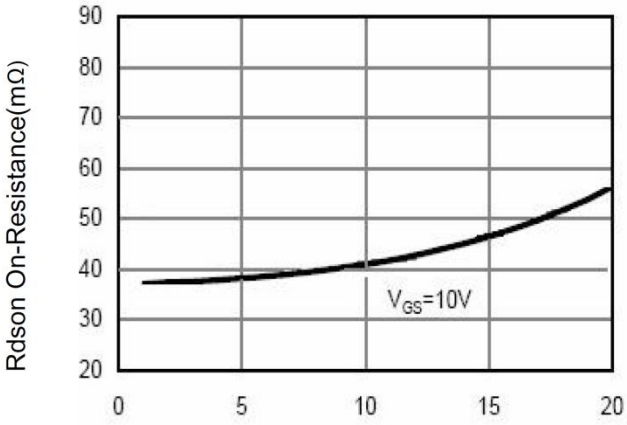


Figure 3 Rdson- Drain Current

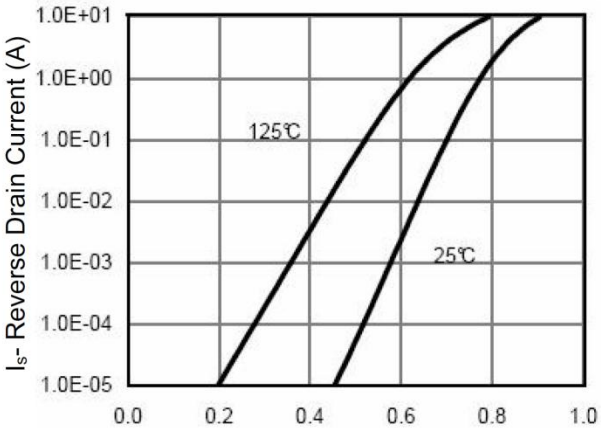


Figure 6 Source- Drain Diode Forward

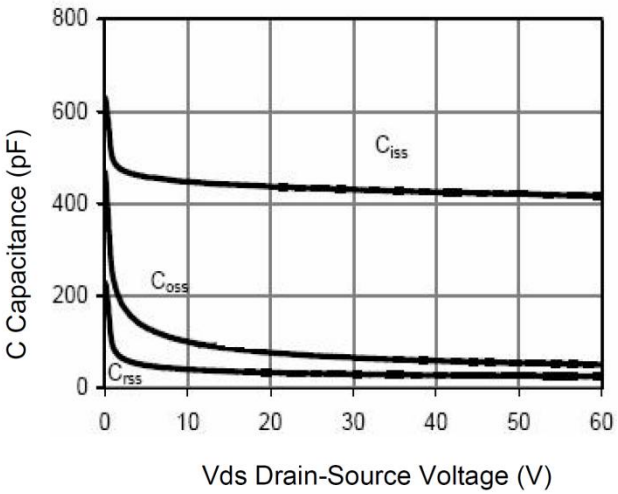


Figure 7 Capacitance vs Vds

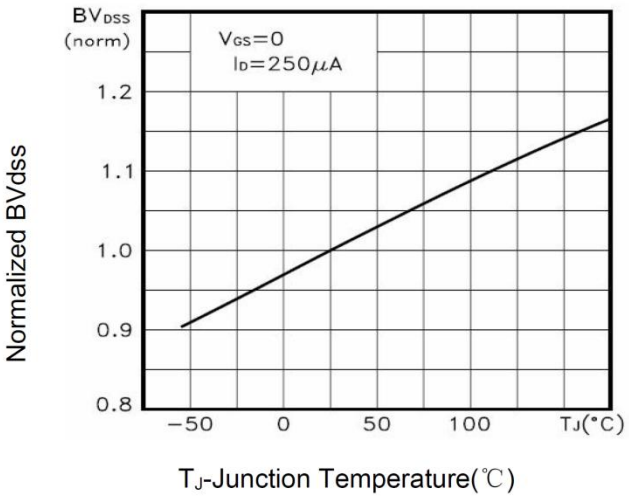


Figure 9 BV_{DSS} vs Junction Temperature

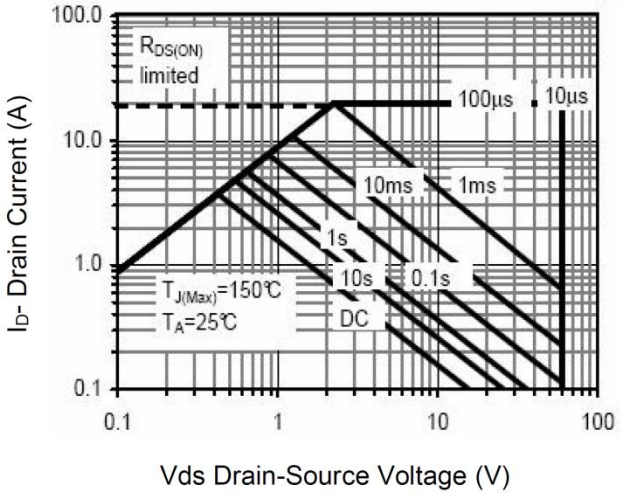


Figure 8 Safe Operation Area

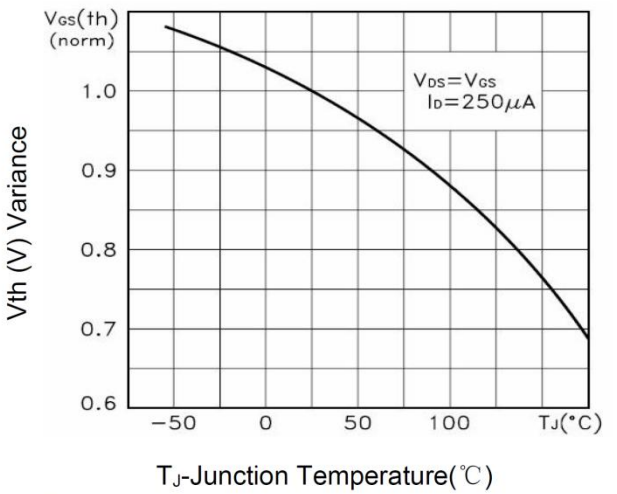


Figure 10 $V_{GS(th)}$ vs Junction Temperature

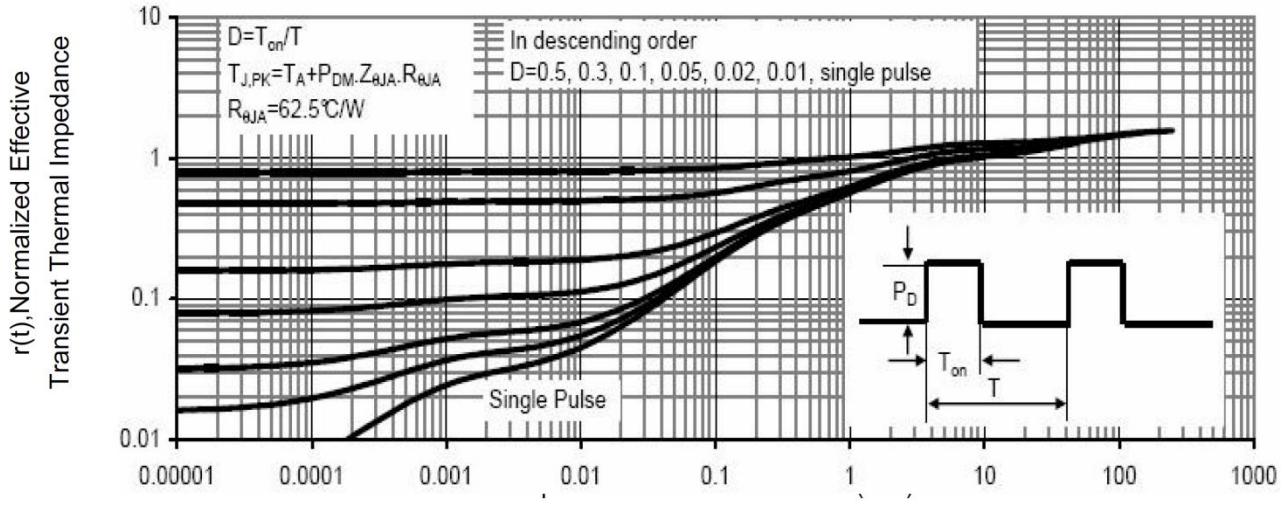
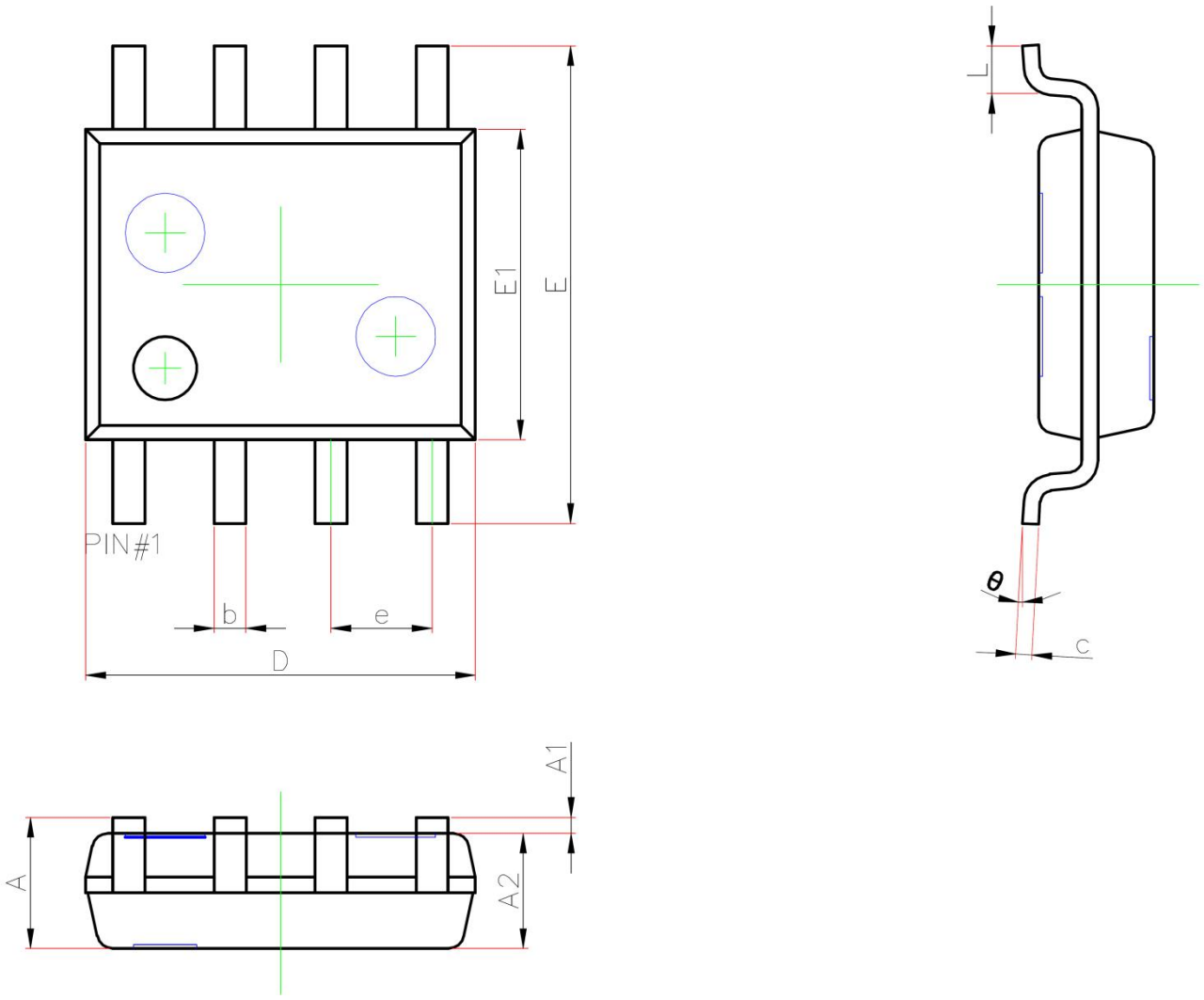


Figure 11 Normalized Maximum Transient Thermal Impedance

SOP-8 Package Information



Symbol	Dimensions In Millimeters	
	Min.	Max.
A	1.35	1.75
A1	0.10	0.25
A2	1.35	1.55
b	0.33	0.51
c	0.17	0.25
D	4.80	5.00
e	1.27 REF.	
E	5.80	6.20
E1	3.80	4.00
L	0.40	1.27
θ	0°	8°