

Product Summary

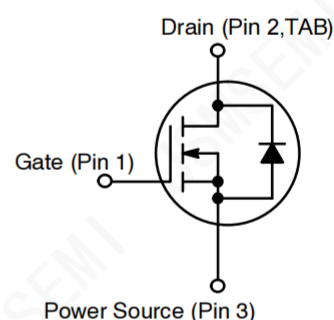
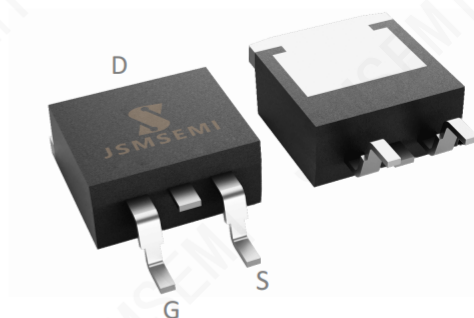
- V_{DS} 100V
- I_D 120A
- $R_{DS(ON)}$ (at $V_{GS}=10V$) $<3.8m\Omega$
- 100% EAS Tested
- 100% ∇V_{DS} Tested

General Description

- Trench Power MOSFET technologygate
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Power switching application
- Uninterruptible power supply
- DC-DC convertor
- Motor drivers



■ Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	100	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current	$T_C=25^\circ\text{C}$	I_D	120	A
	$T_C=100^\circ\text{C}$		120	
Pulsed Drain Current ^A		I_{DM}	480	A
Avalanche energy ^B		EAS	980	mJ
Total Power Dissipation	$T_C=25^\circ\text{C}$	P_D	280	W
	$T_C=100^\circ\text{C}$		120	
Junction and Storage Temperature Range		T_J, T_{STG}	$-55 \sim +150$	$^\circ\text{C}$

■ Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient ^D	Steady-State	$R_{\theta JA}$		40	$^\circ\text{C/W}$
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$		0.45	

Ordering Information

Order number	Package	Marking	Operation Temperature Range	MSL Grade	Ship, Quantity	Green
PSMN3R7-100BSEJ-JSM	TO-263	N3R7-100BSEJ	-55 to 150°C	1	T&R,800	Rohs

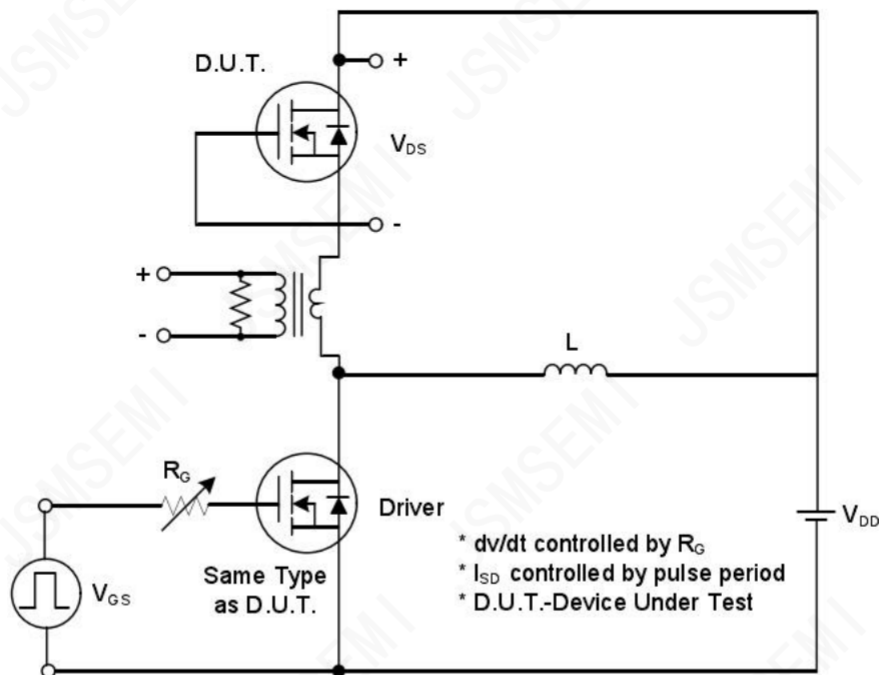
■ Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =250μA	100	-	-	V
		V _{GS} = 0V, I _D =1mA	100	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =100V, V _{GS} =0V	-	-	1	μA
		V _{DS} =100V, V _{GS} =0V, T _J =150°C	-	-	100	
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} =0V	-	-	±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250μA	2.0	3.0	4.0	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =20A	-	3.2	3.8	mΩ
Diode Forward Voltage	V _{SD}	I _S =50A, V _{GS} =0V	-	-	1.2	V
Gate resistance	R _G	f=1MHz	-	1.7	-	Ω
Maximum Body-Diode Continuous Current	I _S		-	-	120	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =50V, V _{GS} =0V, f=1MHz	-	7315	-	pF
Output Capacitance	C _{oss}		-	2656	-	
Reverse Transfer Capacitance	C _{rss}		-	59	-	
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =50V, I _D =20A	-	110	-	nC
Gate-Source Charge	Q _{gs}		-	24	-	
Gate-Drain Charge	Q _{gd}		-	35	-	
Reverse Recovery Charge	Q _{rr}	I _F =20A, di/dt=100A/us	-	209	-	nC
Reverse Recovery Time	t _{rr}		-	90	-	ns
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DD} =50V, I _D =20A R _{GEN} =3Ω	-	25	-	ns
Turn-on Rise Time	t _r		-	45	-	
Turn-off Delay Time	t _{D(off)}		-	88	-	
Turn-off fall Time	t _f		-	53	-	

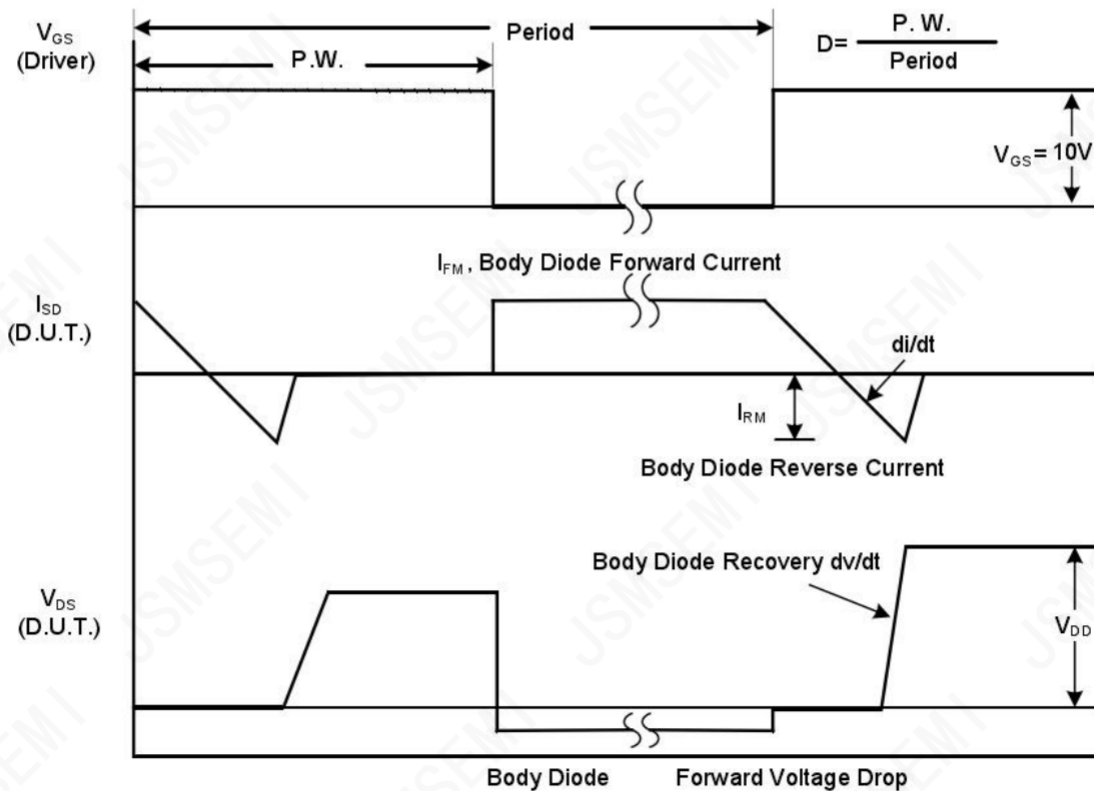
A. Repetitive rating; pulse width limited by max. junction temperature.

 B. $T_J=25^\circ\text{C}$, $V_G=10V$, $R_G=25\Omega$, $L=0.5mH$

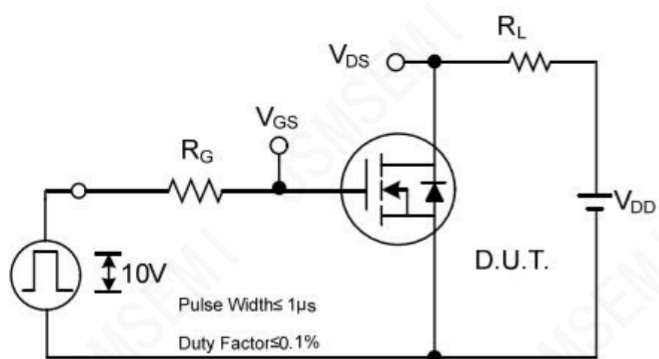
■ RATING AND CHARACTERISTIC CURVES



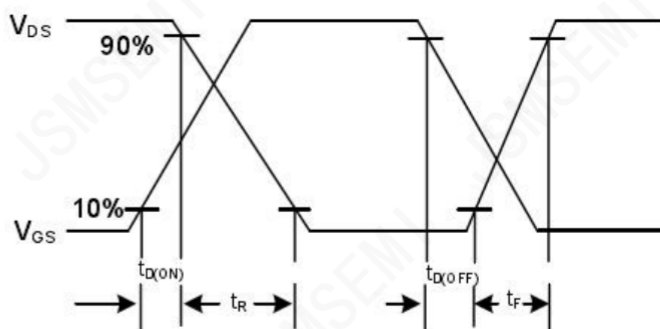
Peak Diode Recovery dv/dt Test Circuit



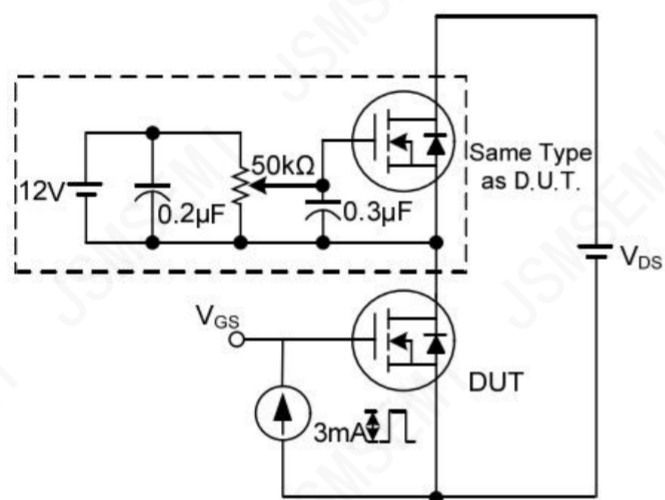
Peak Diode Recovery dv/dt Waveforms



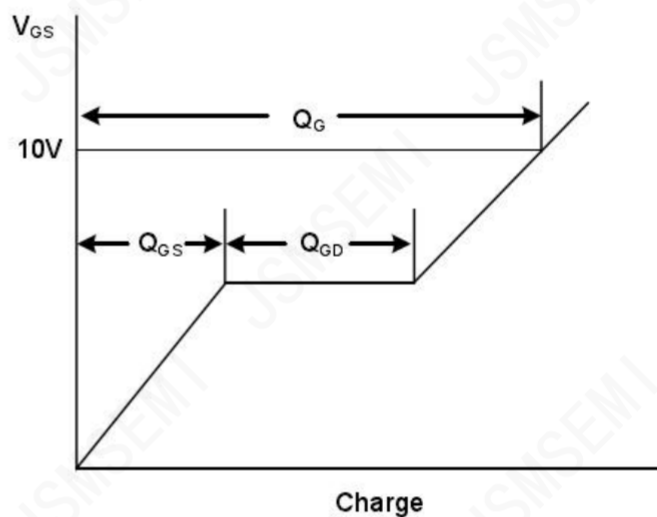
Switching Test Circuit



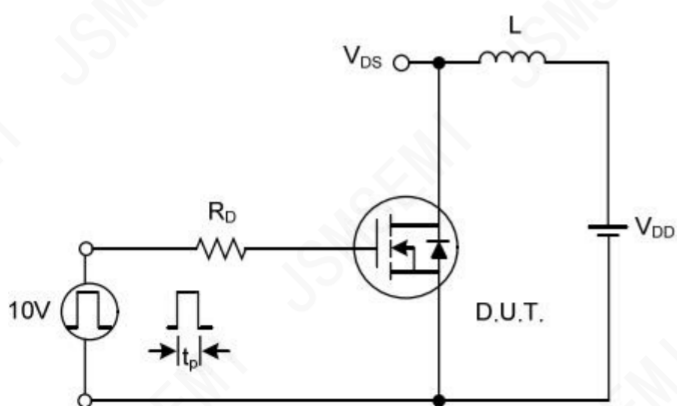
Switching Waveforms



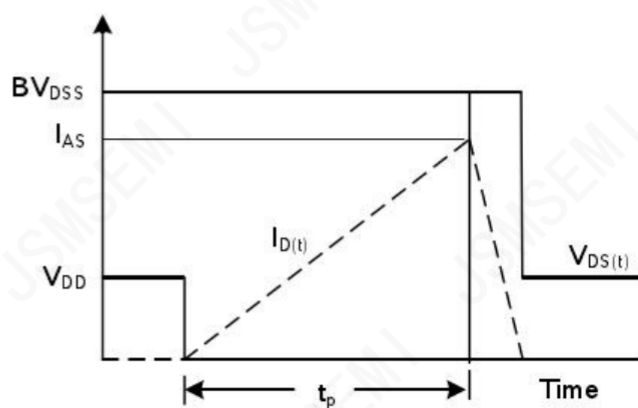
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

■ Typical Electrical and Thermal Characteristics Diagrams

Figure 1: Power De-rating

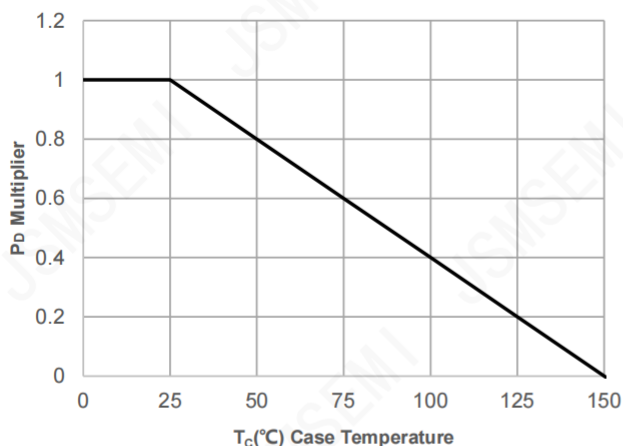


Figure 2: Current De-rating

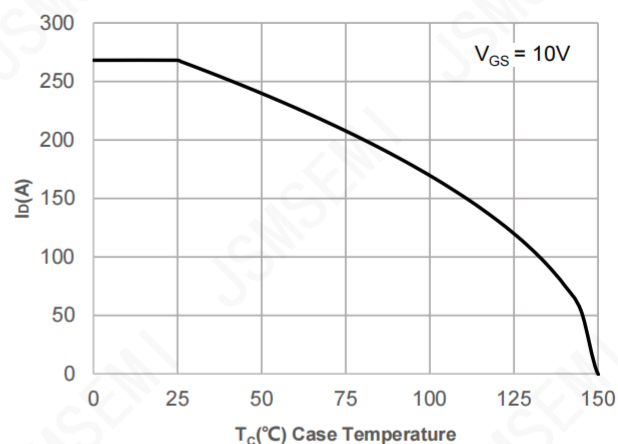


Figure 3: Normalized Maximum Transient Thermal Impedance

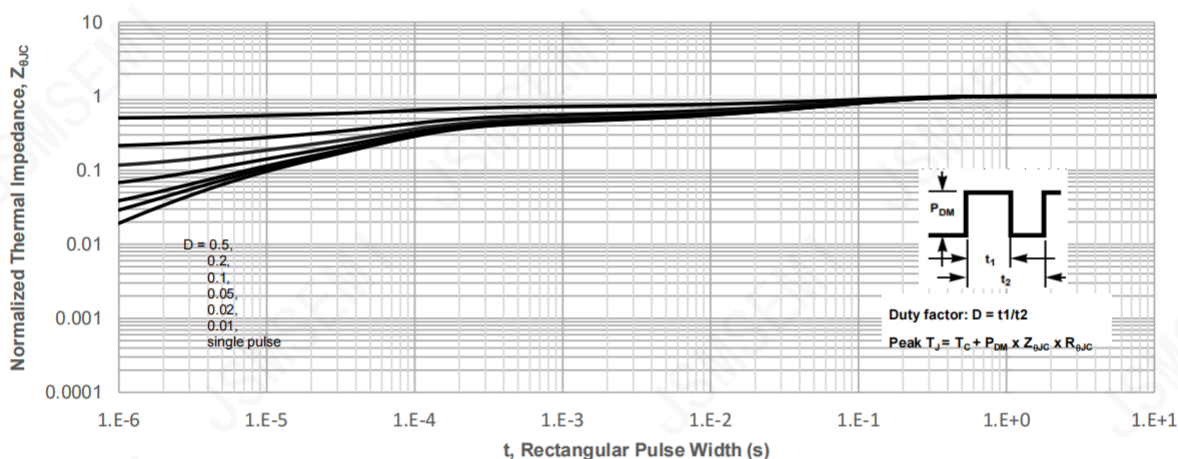


Figure 4: Peak Current Capacity

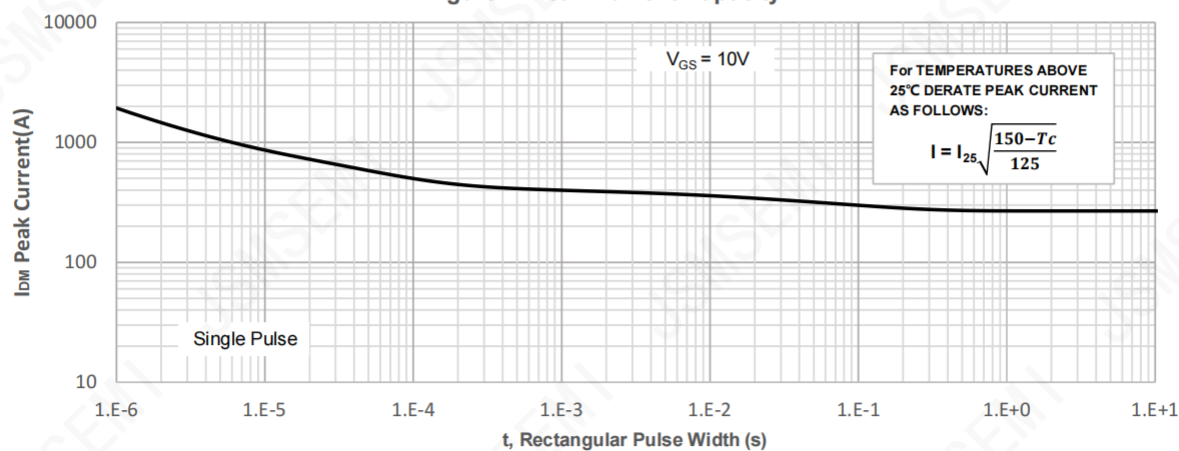


Figure 5: Output Characteristics

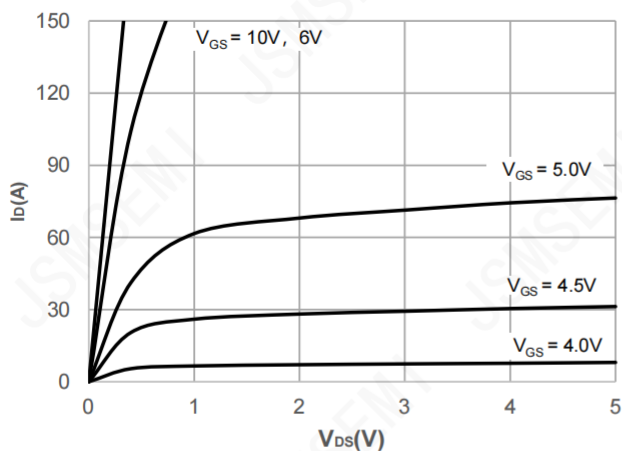


Figure 6: Typical Transfer Characteristics

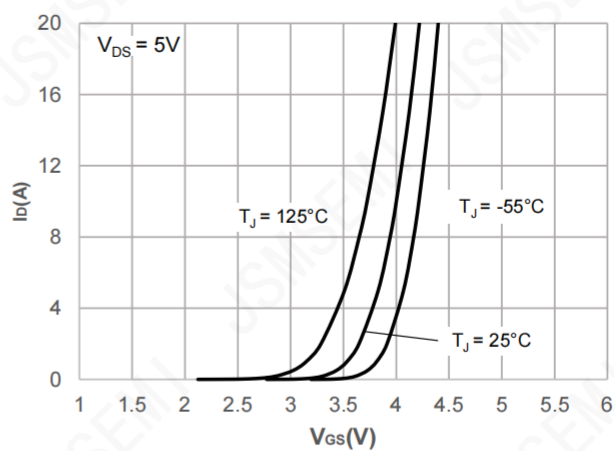


Figure 7: On-resistance vs. Drain Current

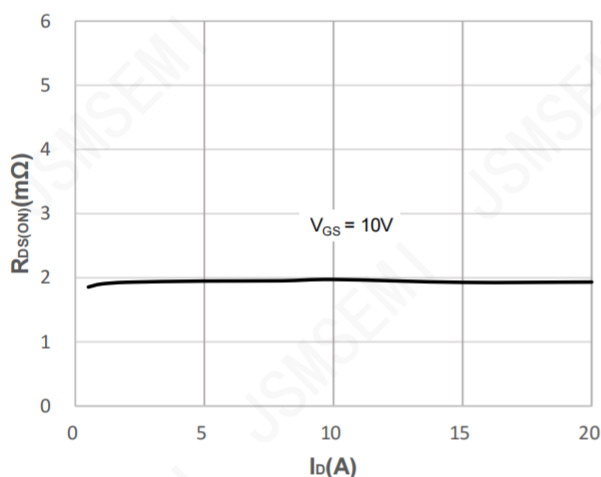


Figure 8: Body Diode Characteristics

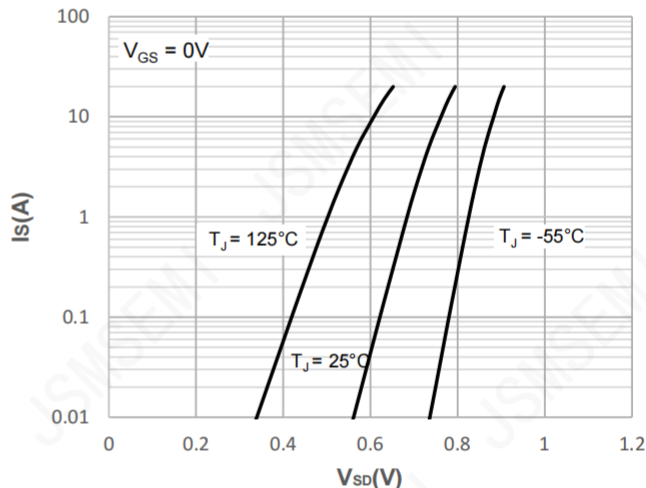


Figure 9: Gate Charge Characteristics

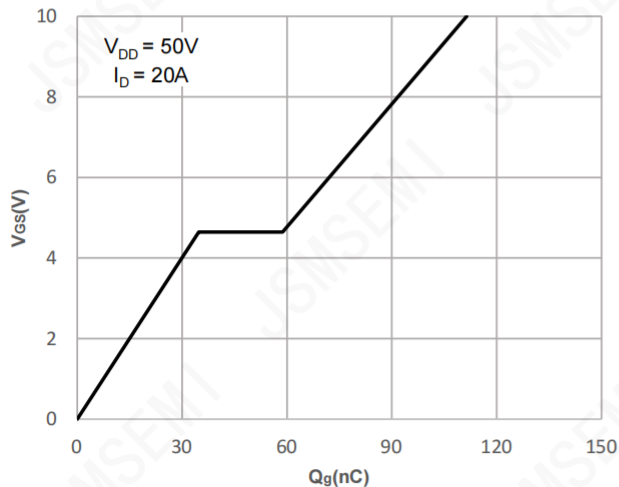


Figure 10: Capacitance Characteristics

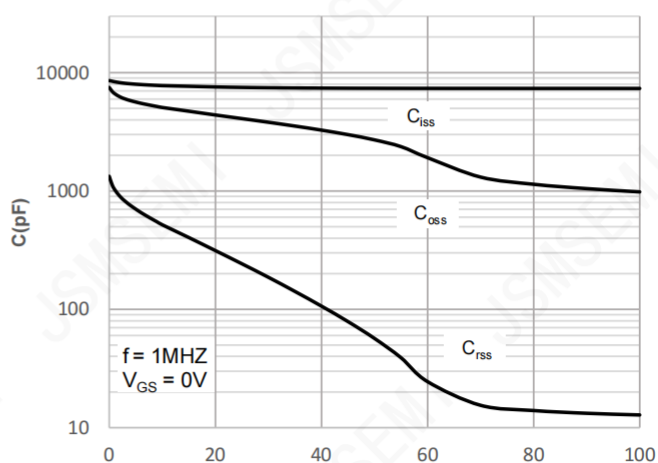


Figure 11: Normalized Breakdown voltage vs. Junction Temperature

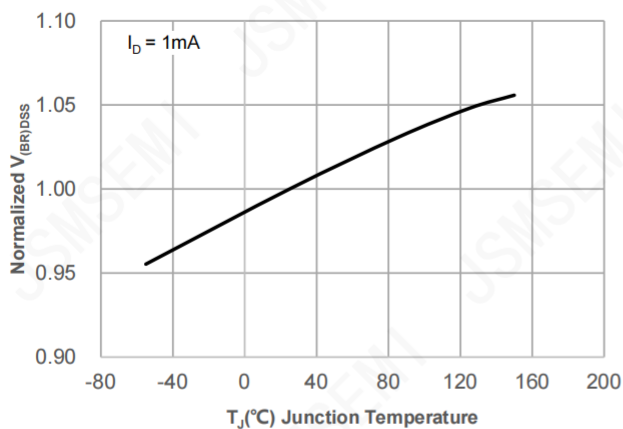


Figure 12: Normalized on Resistance vs. Junction Temperature

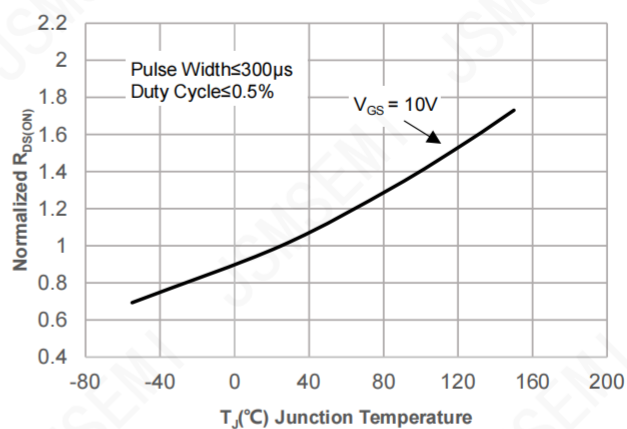


Figure 13: Normalized Threshold Voltage vs. Junction Temperature

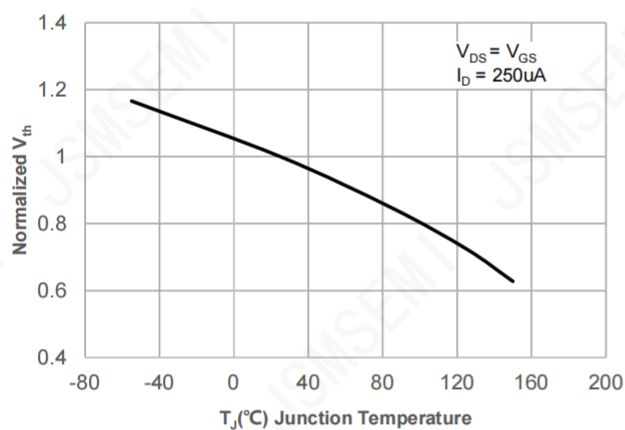


Figure 14: $R_{DS(ON)}$ vs. V_{GS}

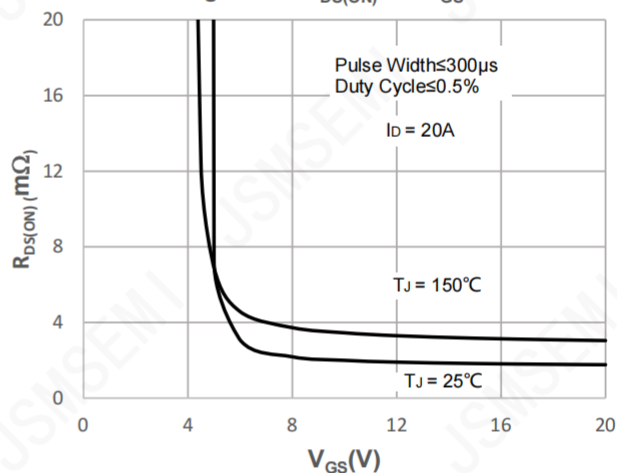
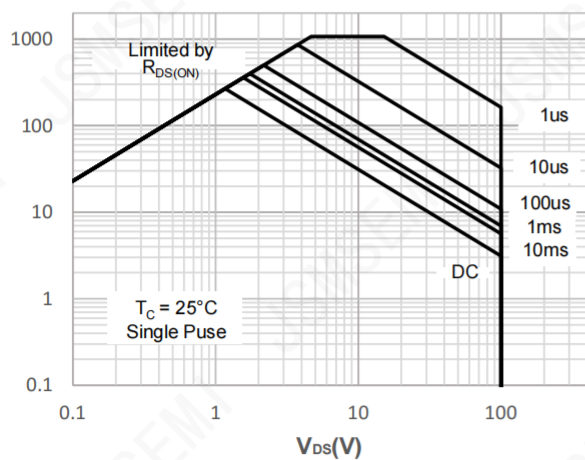
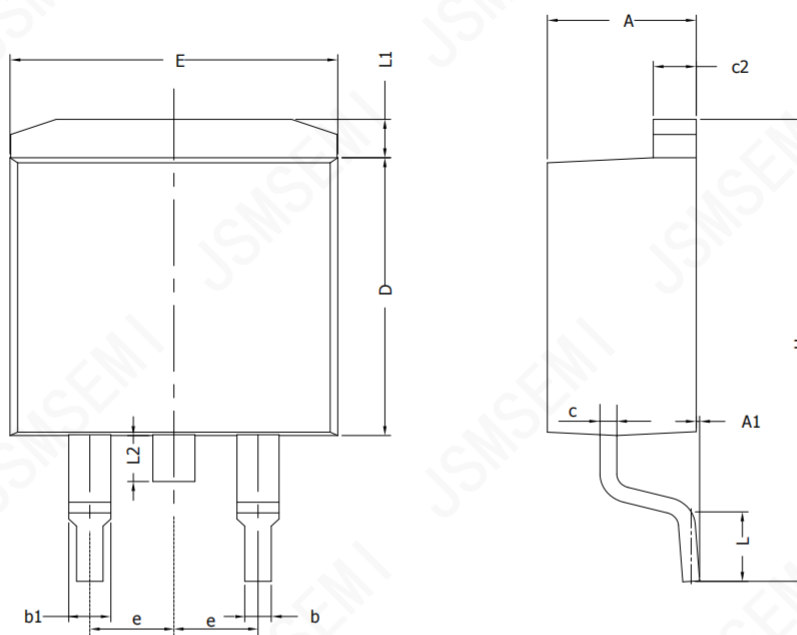


Figure 15: Maximum Safe Operating Area



Package Information

TO-263



SYMBOL	MIN	NOM	MAX
A	4.30	4.57	4.72
A1	0	0.10	0.25
b	0.71	0.81	0.91
c	0.30	---	0.60
c2	1.17	1.27	1.37
D	8.50	---	9.35
E	9.80	---	10.45
e	2.54BSC		
H	14.70	---	15.75
L	2.00	2.30	2.74
L1	1.12	1.27	1.42
L2	---	---	1.75

Revision History

Rev.	Change	Date
V1.0	Initial version	6/27/2021

Important Notice

JSMSEMI Semiconductor (JSMSEMI) PRODUCTS ARE NEITHER DESIGNED NOR INTENDED FOR USE IN MILITARY AND/OR AEROSPACE, AUTOMOTIVE OR MEDICAL DEVICES OR SYSTEMS UNLESS THE SPECIFIC JSMSEMI PRODUCTS ARE SPECIFICALLY DESIGNATED BY JSMSEMI FOR SUCH USE. BUYERS ACKNOWLEDGE AND AGREE THAT ANY SUCH USE OF JSMSEMI PRODUCTS WHICH JSMSEMI HAS NOT DESIGNATED FOR USE IN MILITARY AND/OR AEROSPACE, AUTOMOTIVE OR MEDICAL DEVICES OR SYSTEMS IS SOLELY AT THE BUYER' S RISK.

JSMSEMI assumes no liability for application assistance or customer product design. Customers are responsible for their products and applications using JSMSEMI products.

Resale of JSMSEMI products or services with statements diferent from or beyond the parameters stated by JSMSEMI for that product or service voids all express and any implied warranties for the associated JSMSEMI product or s ervice. JSMSEMI is not responsible or liable for any such statements.

JSMSEMI All Rights Reserved. Information and data in this document are owned by JSMSEMI wholly and may not be edited, reproduced, or redistributed in any way without the express written consent from JSMSEMI.

Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the JSMSEMI product that you intend to use.

For additional information please contact Kevin@jsmsemi.com or visit www.jsmsemi.com