

Product Summary

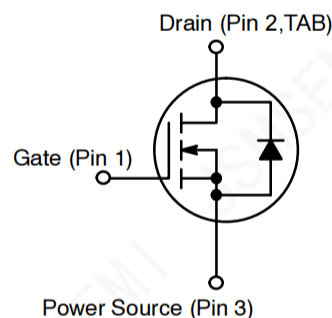
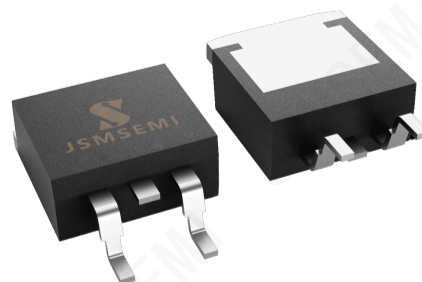
- V_{DS} 100V
- I_D 65A
- $R_{DS(ON)}$ (at $V_{GS}=10V$) $<30m\Omega$
- 100% EAS Tested
- 100% ∇V_{DS} Tested

General Description

- Vertical Double-diffused MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Power switching application
- Uninterruptible power supply
- DC-DC convertor
- Motor drivers



Absolute Maximum Ratings $T_C = 25^\circ C$, unless otherwise noted

Parameter	Symbol	Value	Unit
		TO-263	
Drain-Source Voltage ($V_{GS} = 0V$)	V_{DSS}	100	V
Continuous Drain Current	I_D	65	A
Pulsed Drain Current (note1)	I_{DM}	260	A
Gate-Source Voltage	V_{GSS}	± 20	V
Single Pulse Avalanche Energy (note2)	E_{AS}	243	mJ
Avalanche Current (note1)	I_{AR}	40	A
Repetitive Avalanche Energy (note1)	E_{AR}	46	mJ
Power Dissipation ($T_C = 25^\circ C$)	P_D	250	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 175	$^\circ C$

Thermal Resistance

Parameter	Symbol	Value	Unit
		TO-263	
Thermal Resistance, Junction-to-Case	R_{thJC}	0.8	$^\circ C/W$
Thermal Resistance, Junction-to-Ambient	R_{thJA}	80	

Specifications $T_J = 25^{\circ}\text{C}$, unless otherwise noted

Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	100	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 100V, V_{GS} = 0V, T_J = 25^{\circ}C$	--	--	1	μA
		$V_{DS} = 80V, V_{GS} = 0V, T_J = 125^{\circ}C$	--	--	100	
Gate-Source Leakage	I_{GSS}	$V_{GS} = +20V, V_{DS}=0V$	--	--	100	nA
		$V_{GS}=-20V, V_{DS}=0V$	--	--	-100	
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	2.0	--	4.0	V
Drain-Source On-Resistance (Note3)	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 40A$	--	25	30	m Ω
Forward Transconductance	gfs	$V_{DS} = 10V, I_D = 40A$		35		S
Dynamic						
Input Capacitance	C_{iss}	$V_{GS} = 0V,$ $V_{DS} = 25V,$ $f = 1.0MHz$	--	6100	--	pF
Output Capacitance	C_{oss}		--	410	--	
Reverse Transfer Capacitance	C_{rss}		--	260	--	
Total Gate Charge	Q_g	$V_{DD}=50V, I_D = 45A,$ $V_{GS} = 0 \text{ to } 10V$	--	150	--	nC
Gate-Source Charge	Q_{gs}		--	25	--	
Gate-Drain Charge	Q_{gd}		--	75	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD} = 50V,$ $I_D = 45A,$ $V_{GS}= 10V$ $R_G = 2.5 \Omega$	--	28	--	ns
Turn-on Rise Time	t_r		--	88	--	
Turn-off Delay Time	$t_{d(off)}$		--	75	--	
Turn-off Fall Time	t_f		--	25	--	
Drain-Source Body Diode Characteristics						
Continuous Body Diode Current	I_S	$T_C = 25^{\circ}C$	--	--	65	A
Pulsed Diode Forward Current	I_{SM}		--	--	260	
Body Diode Voltage	V_{SD}	$T_J = 25^{\circ}C, I_{SD} = 45A, V_{GS} = 0V$	--	--	1.3	V
Reverse Recovery Time	t_{rr}	$V_{GS} = 0V, I_S = 45A,$ $di_F/dt = 100A/\mu s$	--	195	--	ns
Reverse Recovery Charge	Q_{rr}		--	107	--	μC

- Notes**
1. Repetitive Rating: Pulse width limited by maximum junction temperature
 2. $I_{AS} = 30A, V_{DD} = 50V, R_G = 25 \Omega$, Starting $T_J = 25^{\circ}\text{C}$
 3. Pulse Test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 1\%$

Ordering Information

Order number	Package	Marking	Operation Temperature Range	MSL Grade	Ship, Quantity	Green
IXTA64N10L2-JSM	TO-263	IXTA64N10L2	-55 to 175°C	1	T&R,800	Rohs

Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

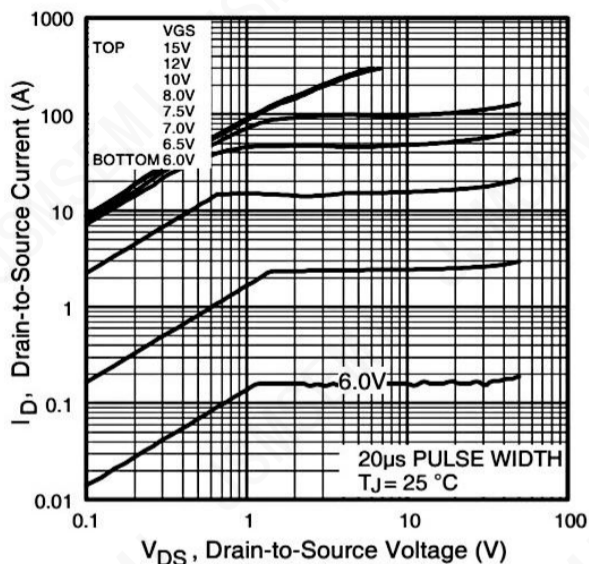


Fig 1. Typical Output Characteristics

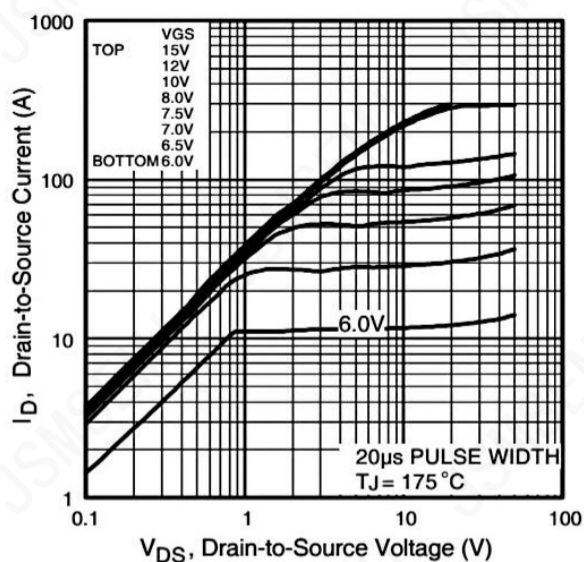


Fig 2. Typical Output Characteristics

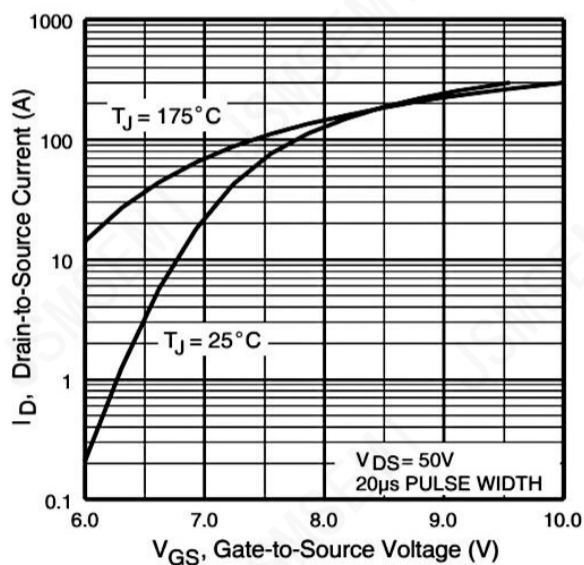


Fig 3. Typical Transfer Characteristics

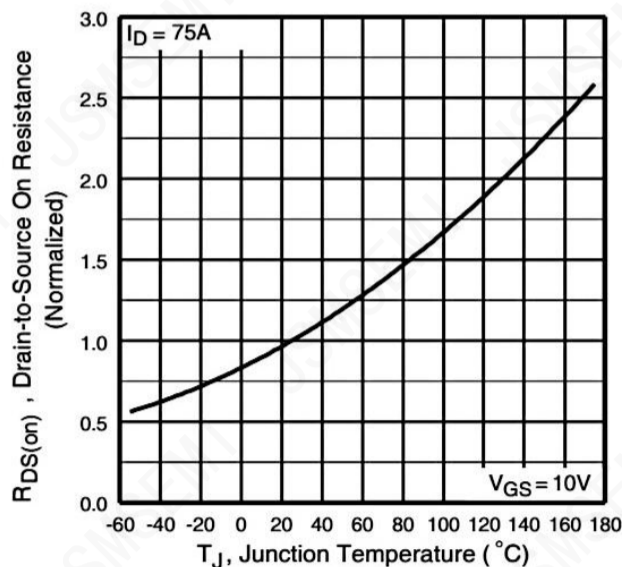
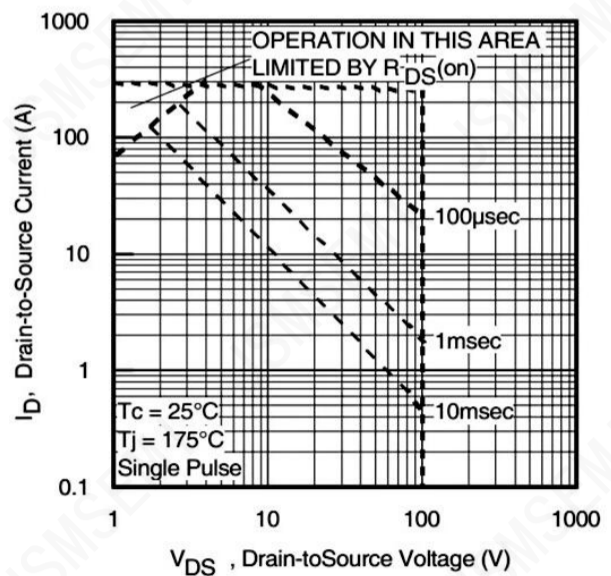
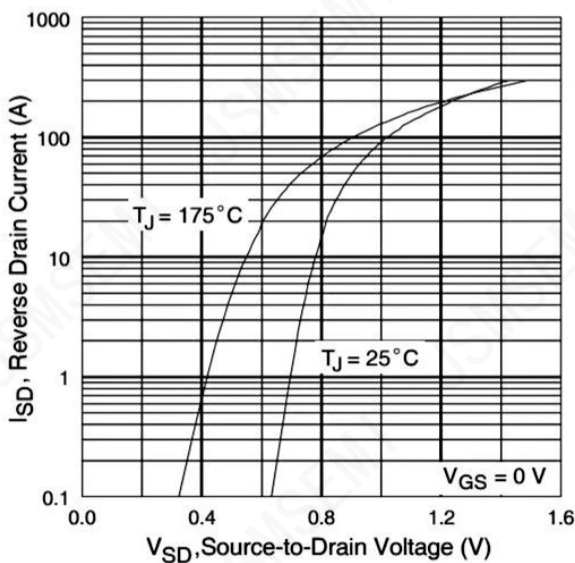
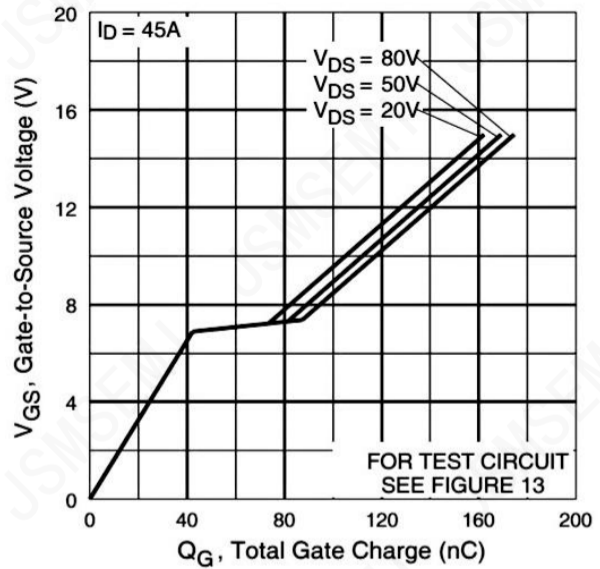
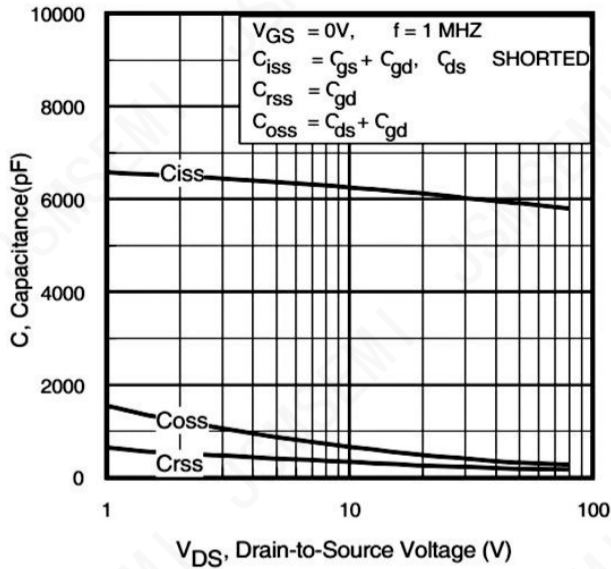


Fig 4. Normalized On-Resistance Vs. Temperature

Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted



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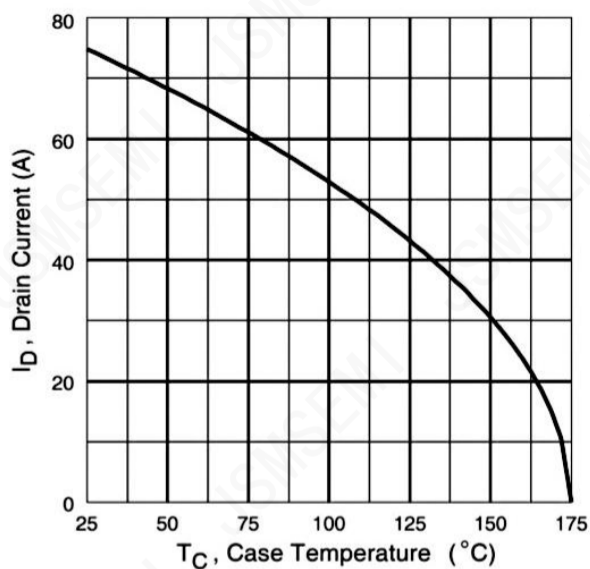


Fig 9. Maximum Drain Current Vs. Case Temperature

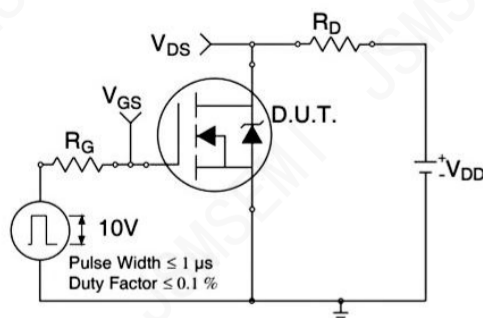


Fig 10a. Switching Time Test Circuit

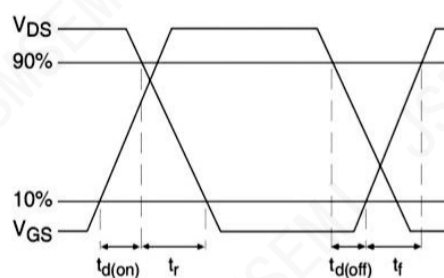
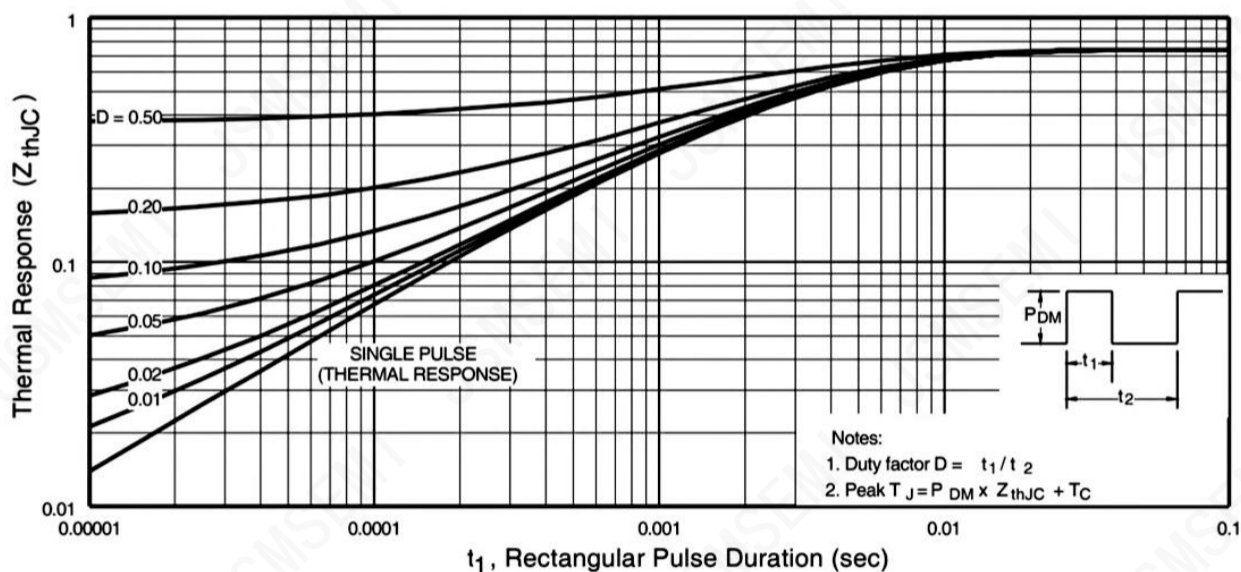
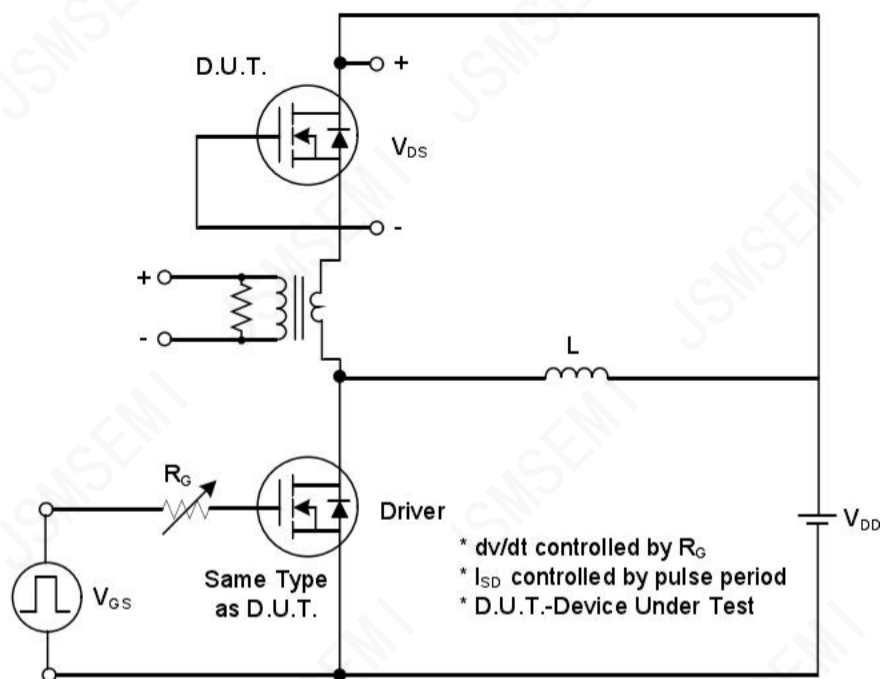


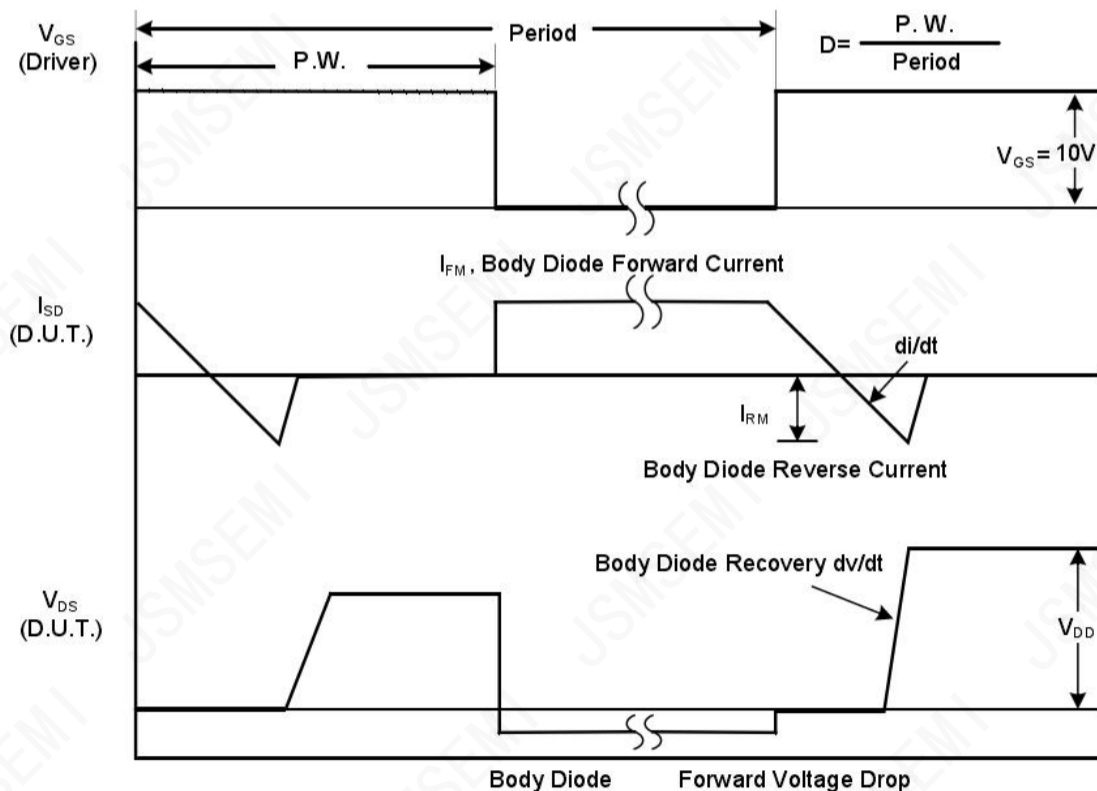
Fig 10b. Switching Time Waveforms



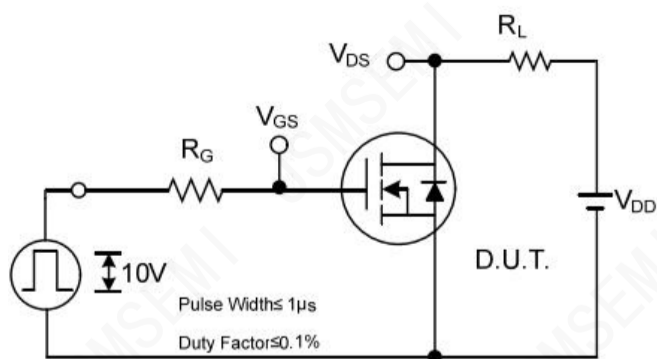
RATING AND CHARACTERISTIC CURVES



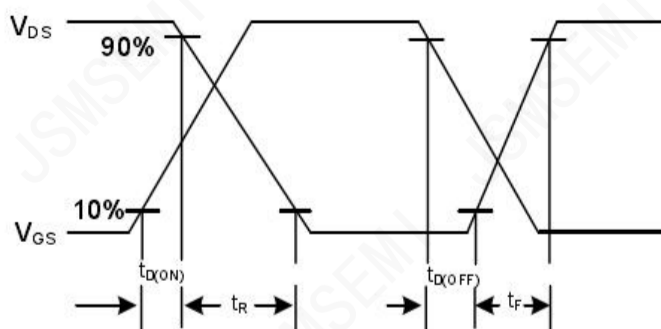
Peak Diode Recovery dv/dt Test Circuit



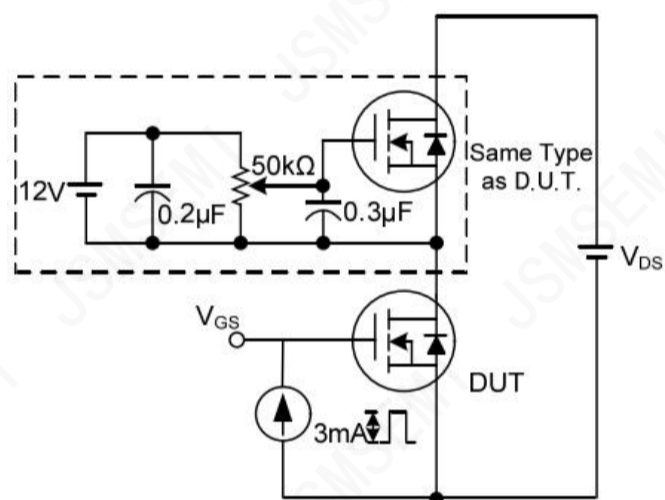
Peak Diode Recovery dv/dt Waveforms



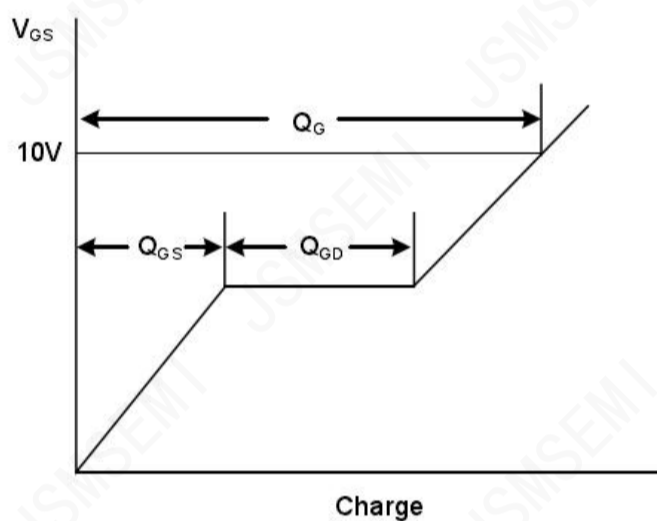
Switching Test Circuit



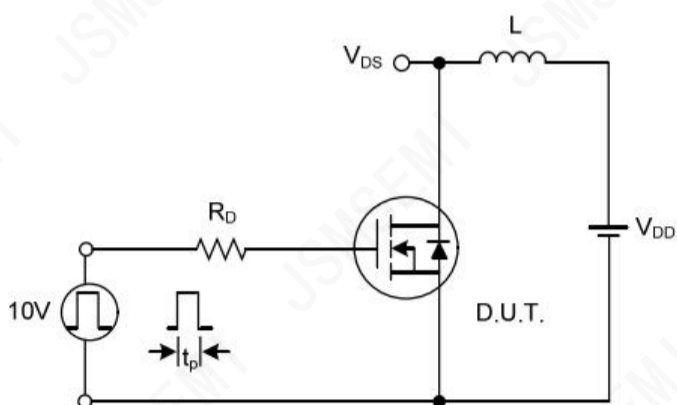
Switching Waveforms



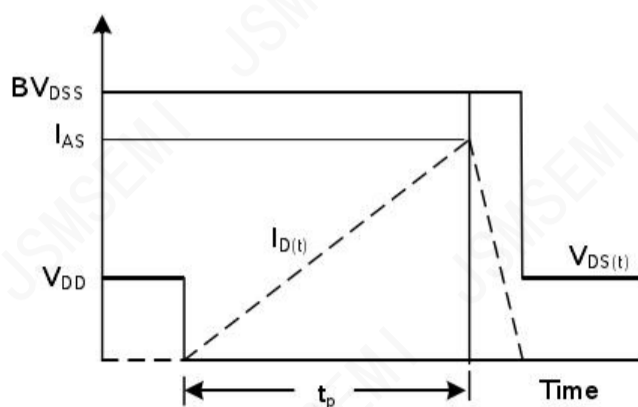
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

Figure A: Gate Charge Test Circuit and Waveform

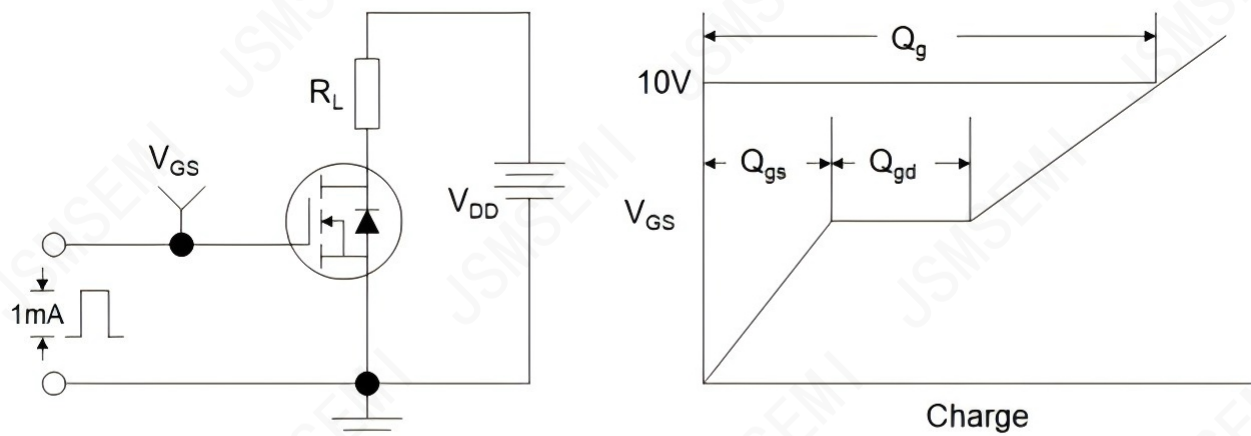


Figure B: Resistive Switching Test Circuit and Waveform

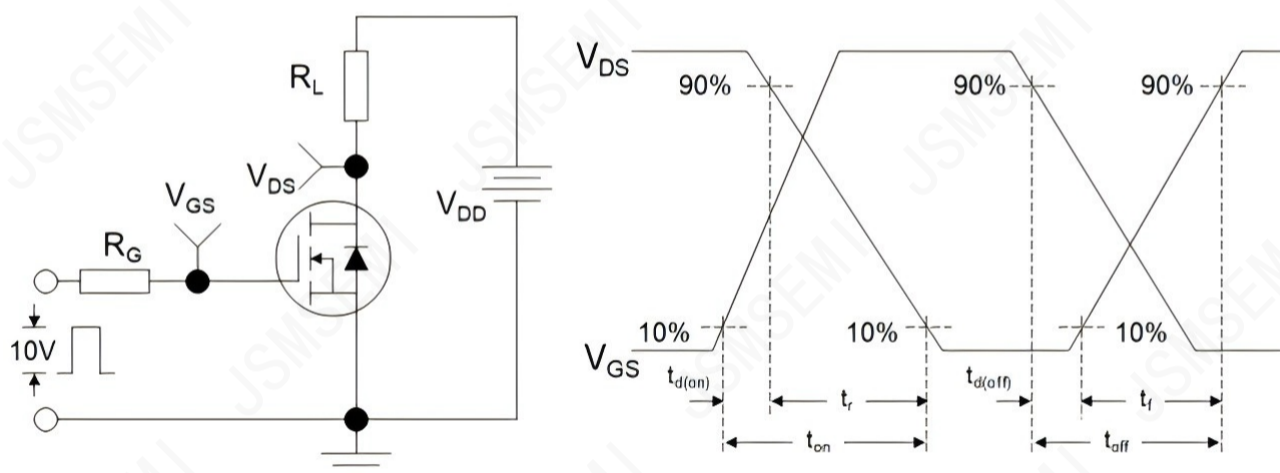
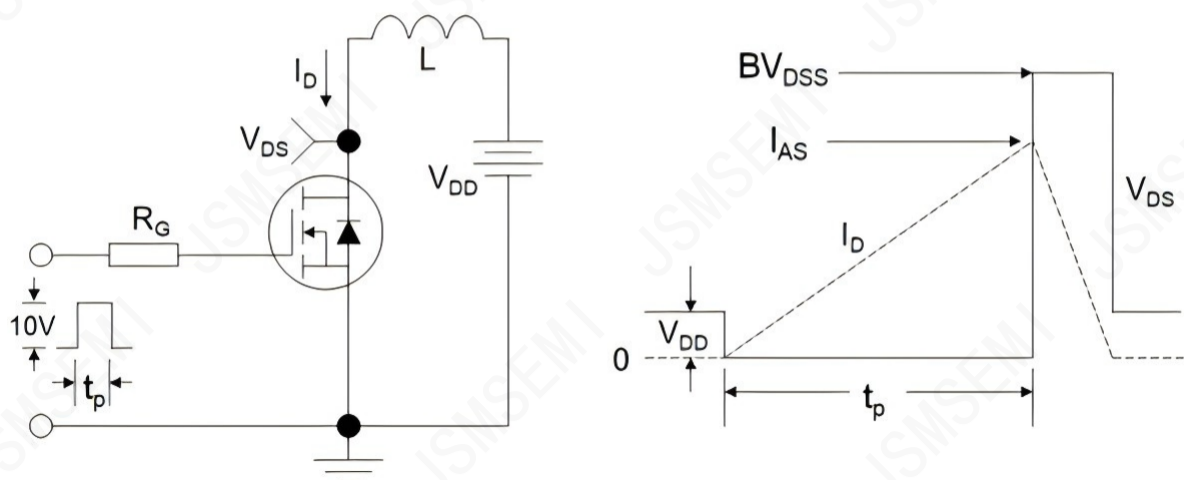
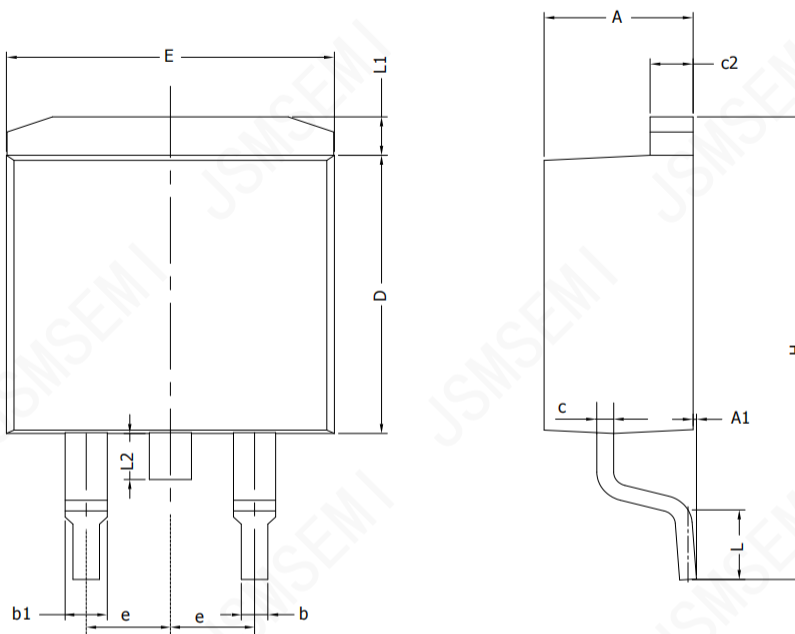


Figure C: Unclamped Inductive Switching Test Circuit and Waveform



Package Information



SYMBOL	MIN	NOM	MAX
A	4.30	4.57	4.72
A1	0	0.10	0.25
b	0.71	0.81	0.91
c	0.30	---	0.60
c2	1.17	1.27	1.37
D	8.50	---	9.35
E	9.80	---	10.45
e	2.54BSC		
H	14.70	---	15.75
L	2.00	2.30	2.74
L1	1.12	1.27	1.42
L2	---	---	1.75

Revision History

Rev.	Change	Date
V1.0	Initial version	3/11/2019

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