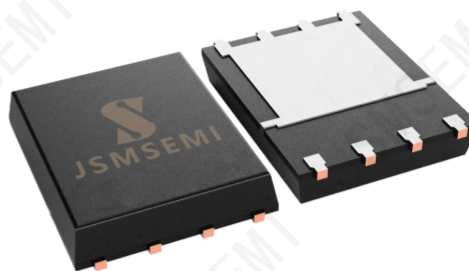


Product Summary

- V_{DS} 60V
- I_D 180A
- $R_{DS(ON)}$ (at $V_{GS}=10V$) $<2.0m\Omega$
- 100% EAS Tested
- 100% ∇V_{DS} Tested

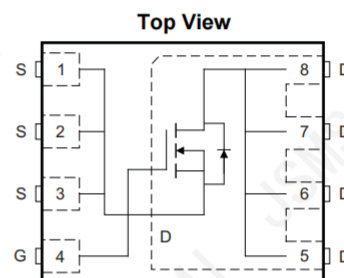


General Description

- Split gate trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Power switching application
- Uninterruptible power supply
- DC-DC convertor
- Motor drivers



■ Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	60	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current	$T_C=25^\circ\text{C}$	I_D	180	A
	$T_C=100^\circ\text{C}$		113	
Pulsed Drain Current ^A		I_{DM}	718	A
Avalanche energy ^B		EAS	740	mJ
Total Power Dissipation ^C	$T_C=25^\circ\text{C}$	P_D	150	W
	$T_C=100^\circ\text{C}$		60	
Junction and Storage Temperature Range		T_J, T_{STG}	$-55 \sim +150$	$^\circ\text{C}$

■ Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient ^D	Steady-State	$R_{\theta JA}$	30		$^\circ\text{C/W}$
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	0.8		

Ordering Information

Order number	Package	Marking	Operation Temperature Range	MSL Grade	Ship, Quantity	Green
JSM020N06QG5H	DFN5060-8L	020N06QG5H	-55 to 150°C	1	T&R, 5000	RoHS

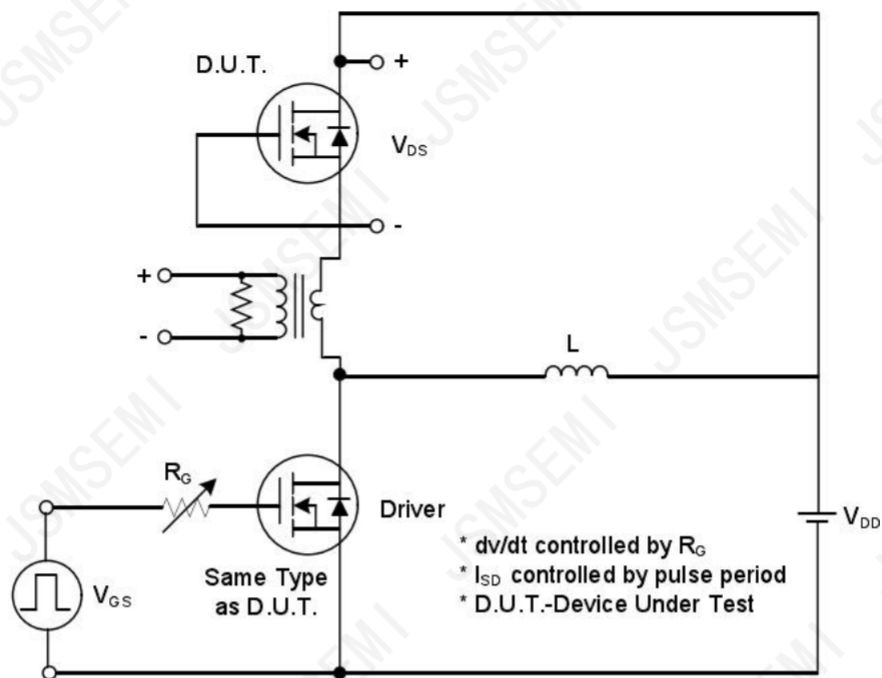
■ Electrical Characteristics ($T_J=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Off Characteristics ⁽⁶⁾						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	60	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 60V, V _{GS} = 0V	-	-	1.0	μA
		T _J = 125°C	-	-	100	μA
Gate-Source Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} = 0V	-	-	±100	nA
On Characteristics ⁽⁶⁾						
Gate Threshold Voltage	V _{GS(th)}	V _{GS} = V _{DS} , I _D = 250μA	2.0	3.0	4.0	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} = 10V, I _D = 20A	-	1.7	2.0	mΩ
Forward Transconductance	g _{fs}	V _{DS} = 5.0V, I _D = 20A	-	42	-	S
Diodes Forward Voltage	V _{SD}	I _S = 2.0A, V _{GS} = 0V	-	0.7	1.2	V
Dynamic Characteristics ⁽⁷⁾						
Input Capacitance	C _{iss}	V _{DS} = 30V, V _{GS} = 0V, f = 1MHz	-	5483	-	pF
Output Capacitance	C _{oss}		-	2514	-	pF
Reverse Transfer Capacitance	C _{rss}		-	98	-	pF
Gate Resistance	R _g	V _{GS} = 0V, V _{DS} = 0V, f = 1MHz	-	1.8	-	Ω
Switching Characteristics ⁽⁷⁾						
Turn-On DelayTime	t _{d(on)}	V _{GS} = 10V, V _{DS} = 30V I _D = 20A, R _{GEN} = 3.0Ω	-	8.5	-	ns
Rise Time	t _r		-	18	-	ns
Turn-Off DelayTime	t _{d(off)}		-	65	-	ns
Fall Time	t _f		-	28	-	ns
Gate Charge Characteristics ⁽⁷⁾						
Total Gate Charge (V _{GS} = 10V)	Q _g	V _{DS} = 30V, I _D = 20A V _{GS} = 10V	-	94	-	nC
Total Gate Charge (V _{GS} = 6.0V)	Q _g		-	60	-	nC
Gate-Source Charge	Q _{gs}		-	25	-	nC
Gate-Drain Charge	Q _{gd}		-	23	-	nC
Gate Plateau Voltage	V _{plateau}		-	4.4	-	V
Drain-Source Diode Characteristics ⁽⁷⁾						
Body Diode Reverse Recovery Time	t _{rr}	I _F = 20A, dI/dt = 100A/μs,	-	66	-	ns
Body Diode Reverse Recovery Charge	Q _{rr}	T _J = 25°C	-	131	-	nC
Diode Forward Current	I _S	T _C = 25°C	-	-	179	A

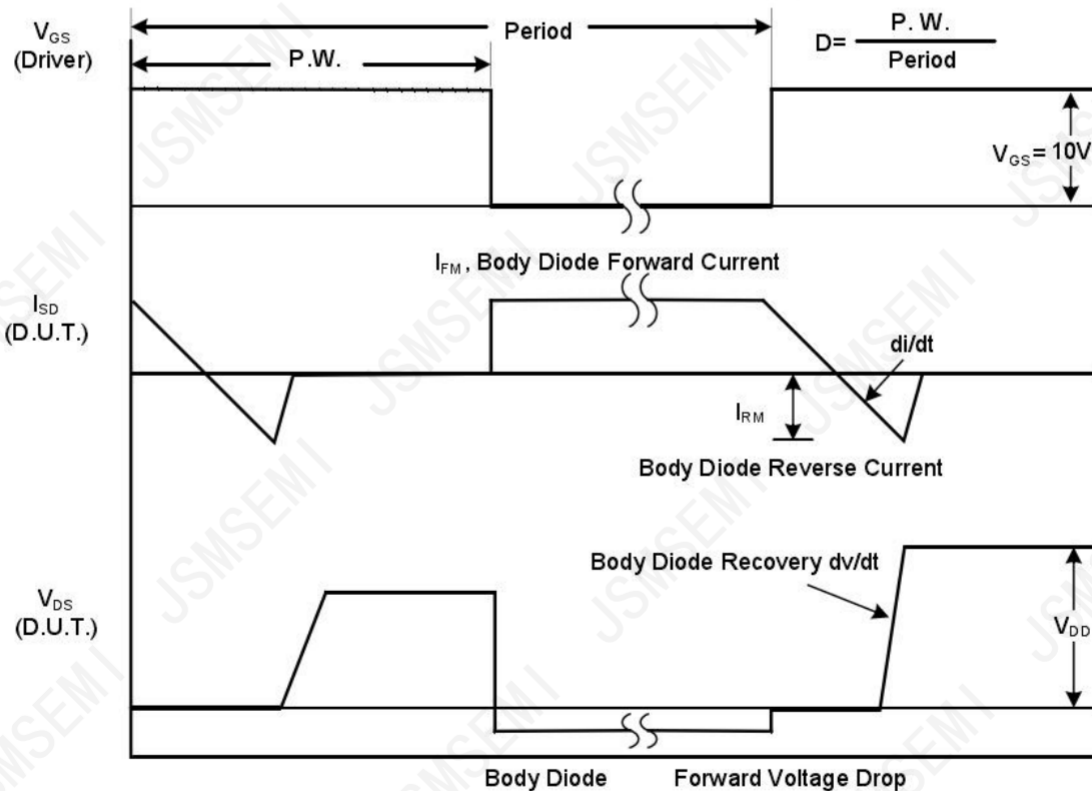
Notes:

1. This current is chip limited, which is calculated based on R_{thjc} .
2. This current is calculated on single pulse with $10\mu s$ Single Pulse.
3. Defined by design, not subject to production test, E_{AS} condition: $T_J=25^{\circ}\text{C}, V_{DD}=30V, V_{GS}=10V, L=1.0mH$.
4. Device mounted on FR-4 substrate PC board with 2oz copper in 1inch square cooling area.
5. Thermal resistance from junction to the exposed drain pad.
6. Short duration pulse test used to minimize self-heating effect.
7. Defined by design, not subject to production.

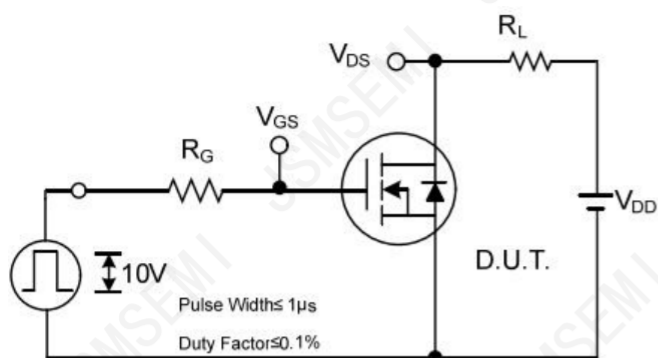
■ RATING AND CHARACTERISTIC CURVES



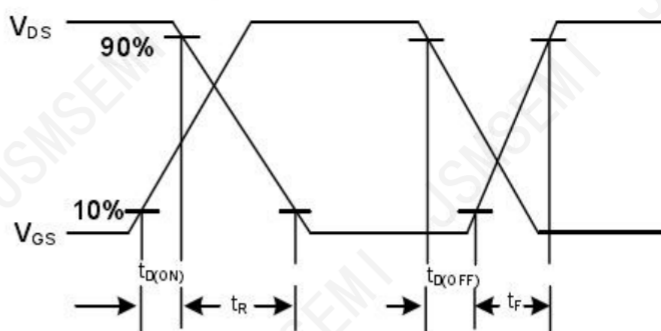
Peak Diode Recovery dv/dt Test Circuit



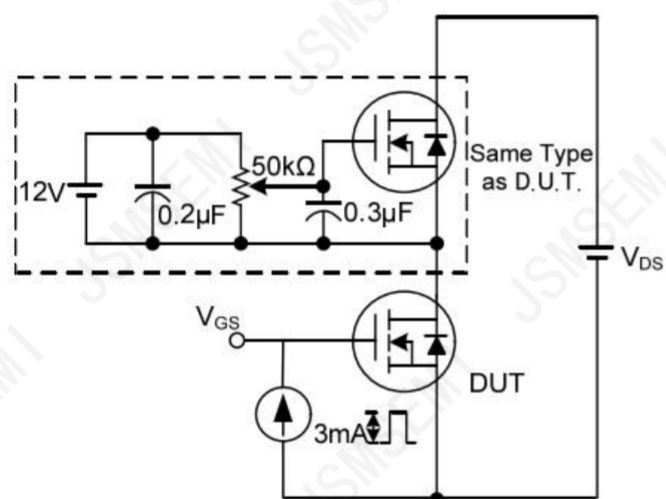
Peak Diode Recovery dv/dt Waveforms



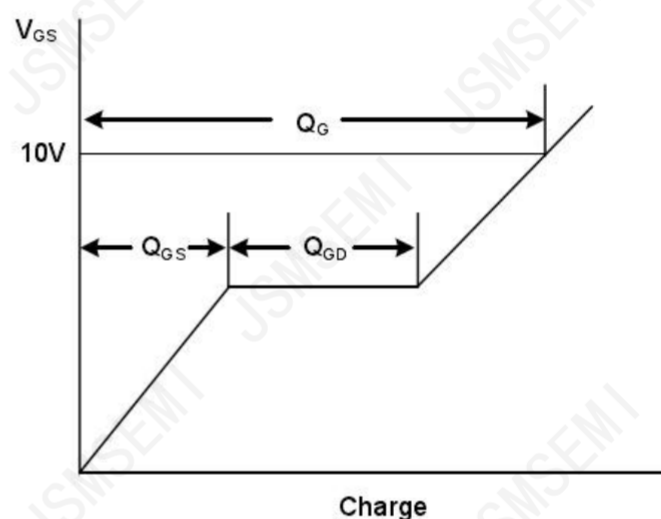
Switching Test Circuit



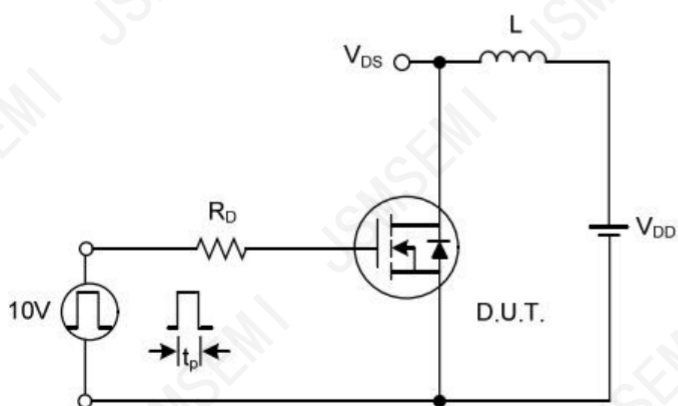
Switching Waveforms



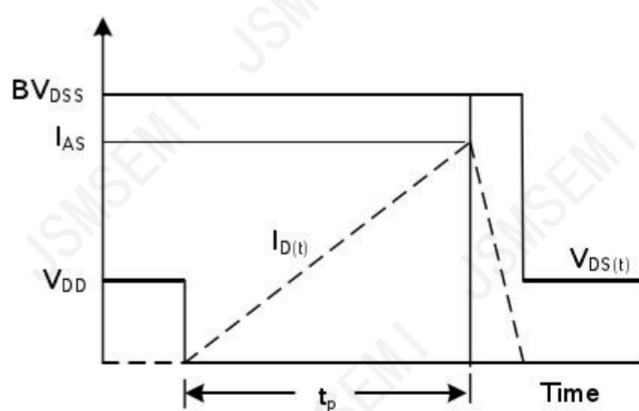
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

■ Typical Electrical and Thermal Characteristics Diagrams

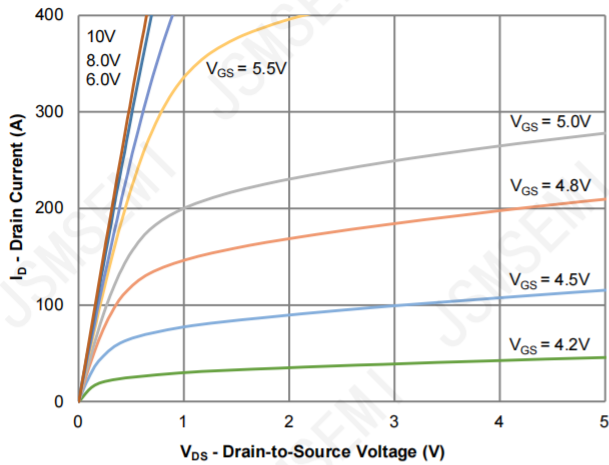


Figure 1: Output Characteristics

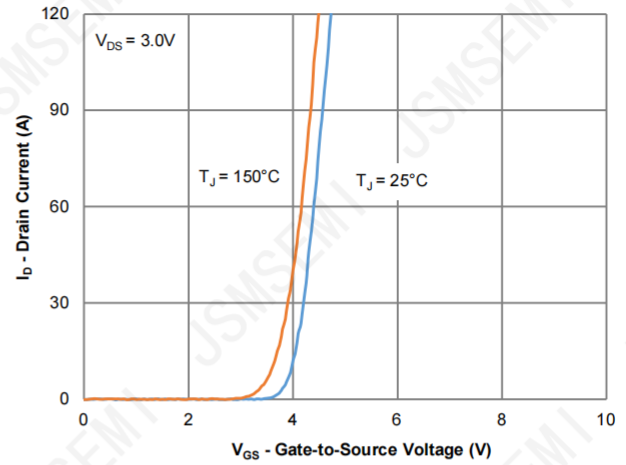


Figure 2: Transfer Characteristics

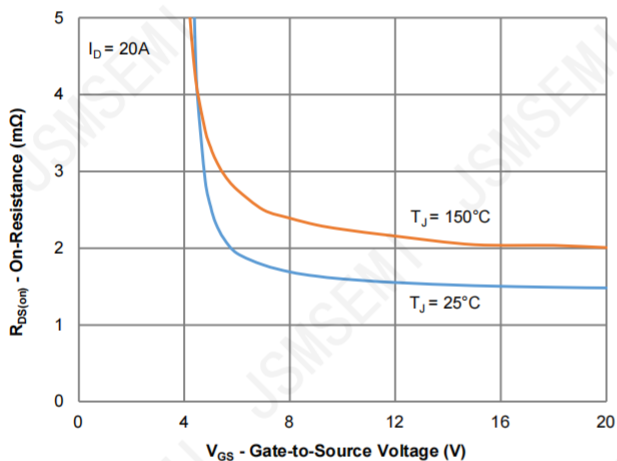


Figure 3: On-Resistance vs. Gate-Source Voltage

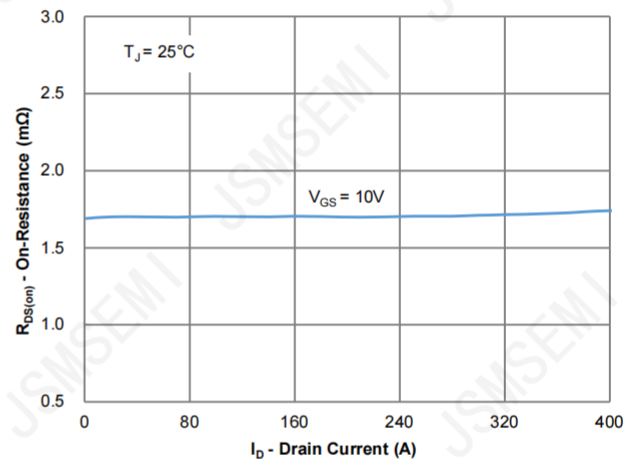


Figure 4: On-Resistance vs. Drain Current and Gate Voltage

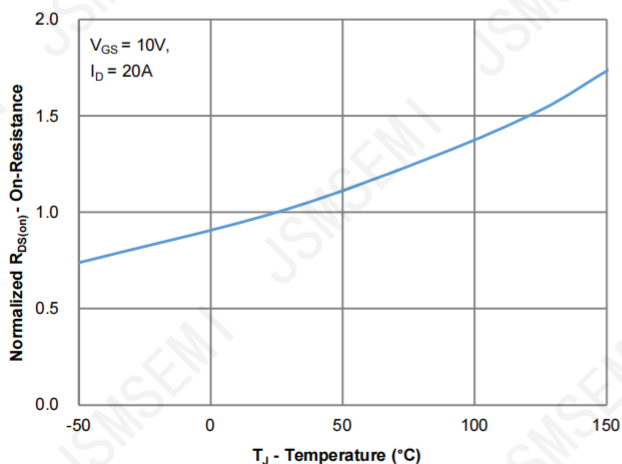


Figure 5: On-Resistance vs. Junction Temperature

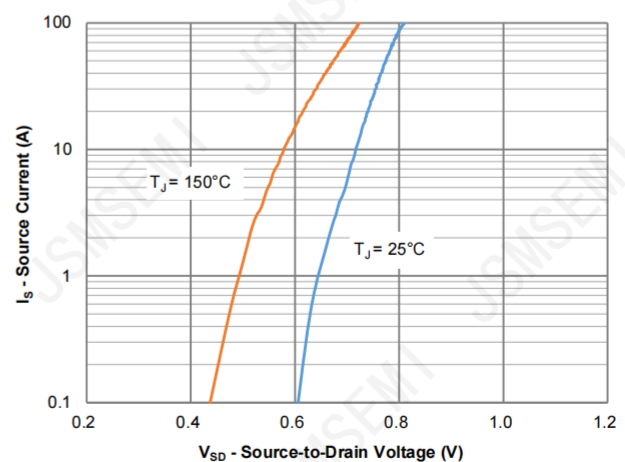


Figure 6: Source-Drain Diode Forward Voltage

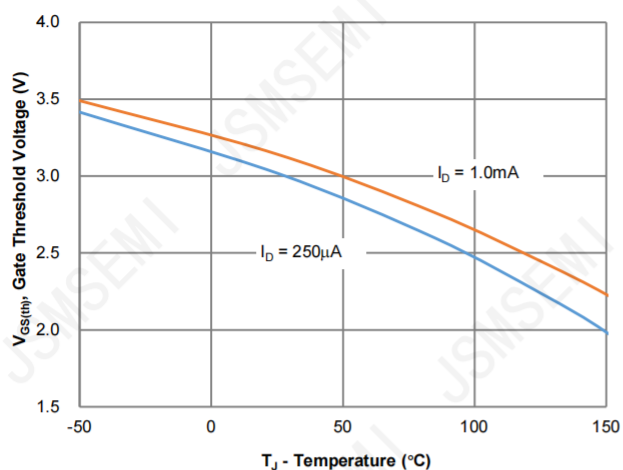


Figure 7: Gate Threshold Variation vs. Junction Temperature

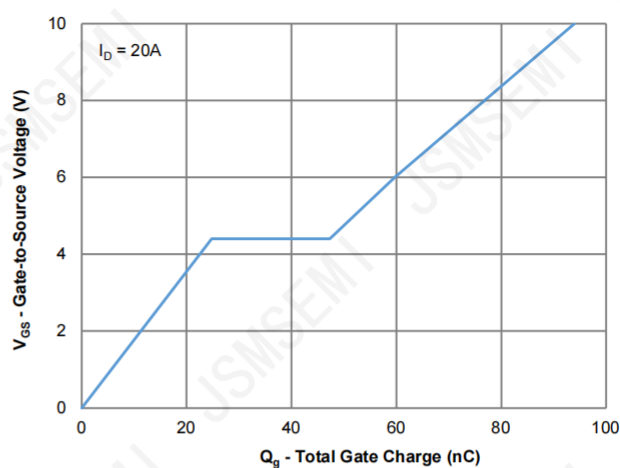


Figure 8: Gate Charge Characteristics

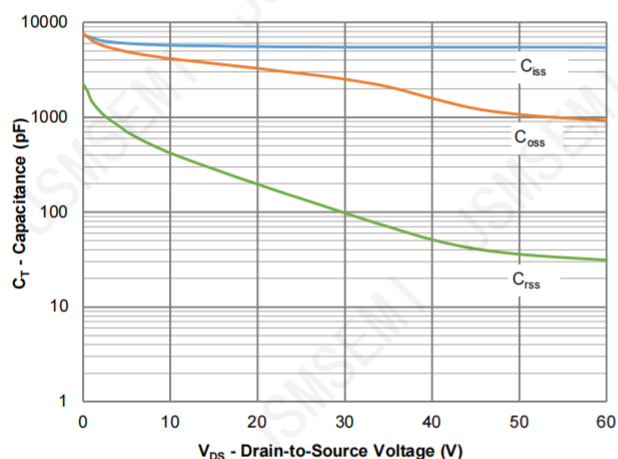


Figure 9: Capacitance Characteristics

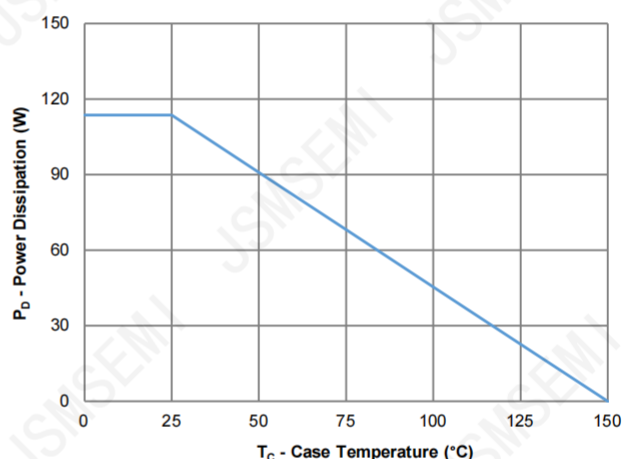


Figure 10: Power Derating

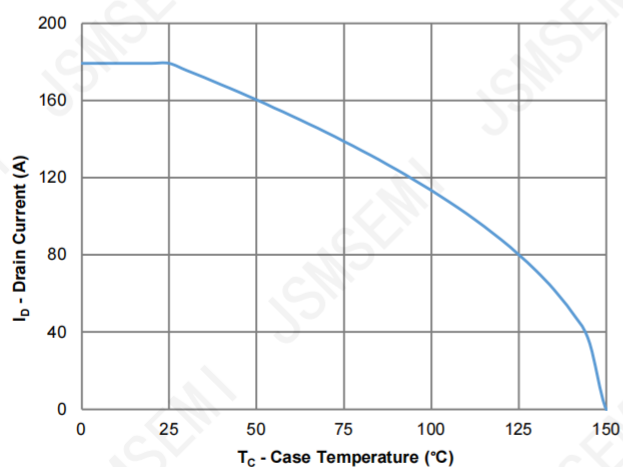


Figure 11: Current Derating

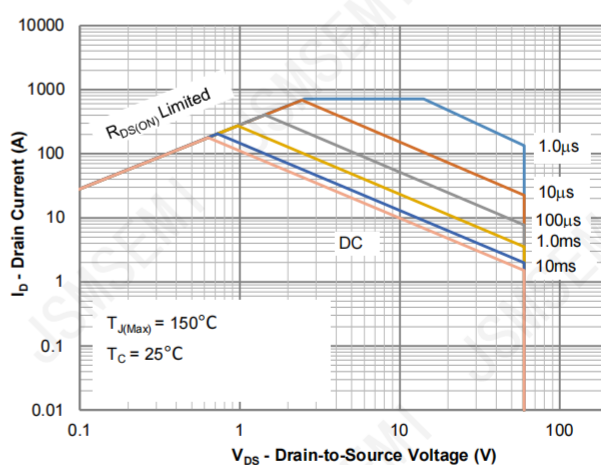


Figure 12: Safe Operating Area

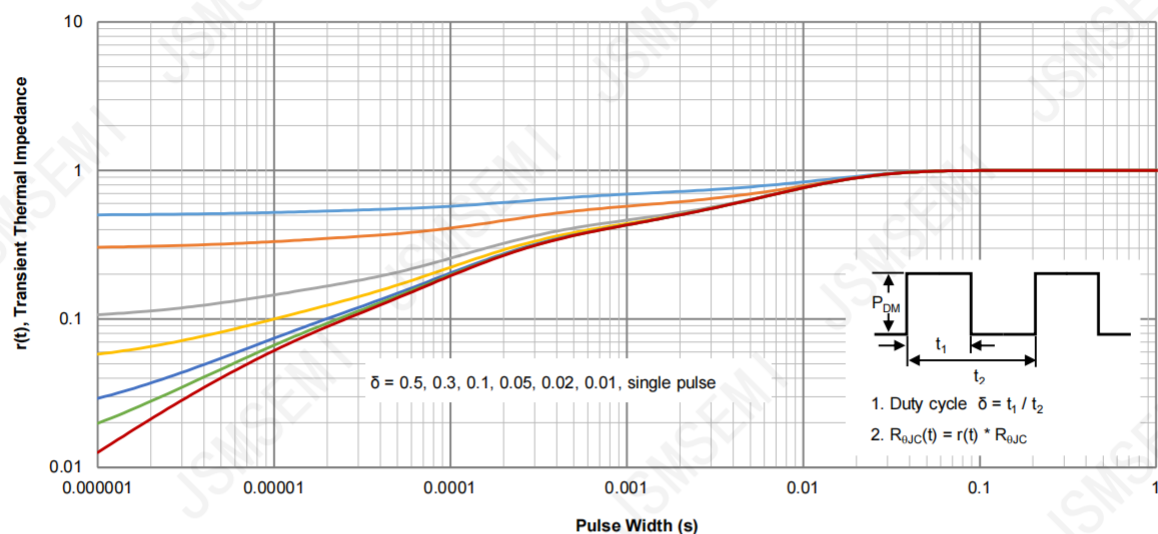
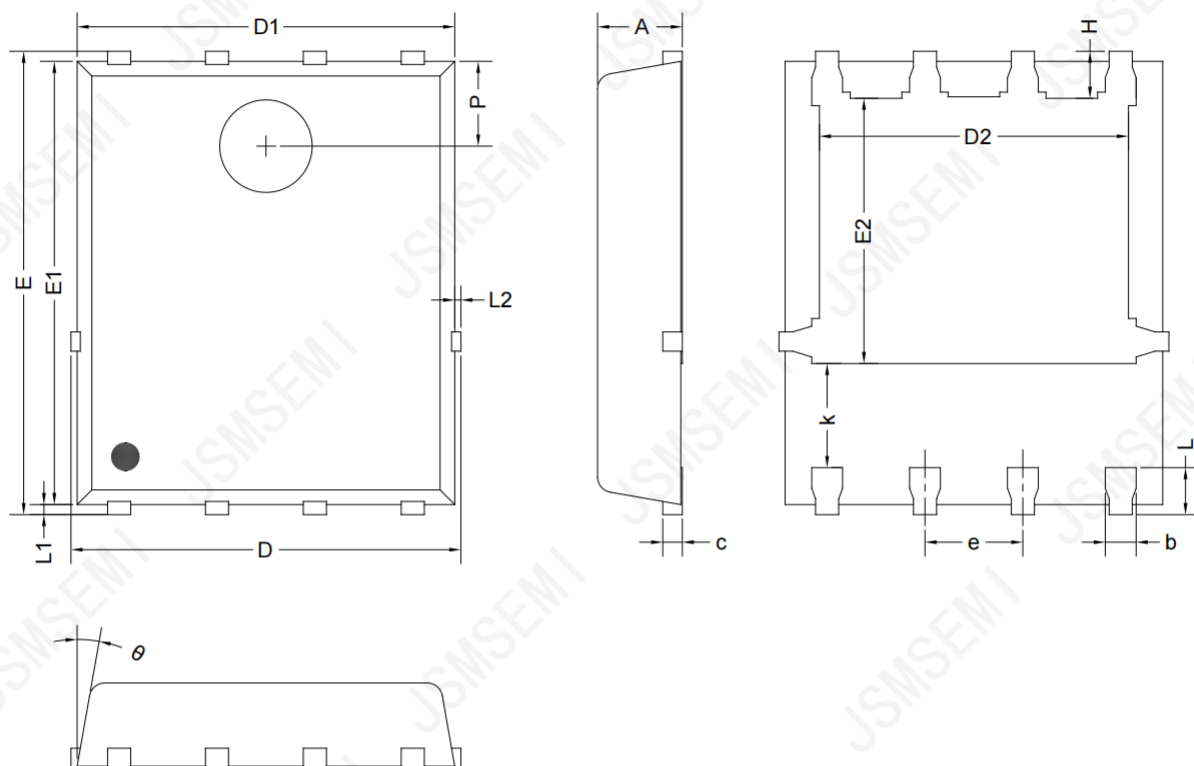


Figure 13: Normalized Maximum Transient Thermal Impedance

Package Information

PDFN5060-8L



Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	1.000	1.100	1.200
b	0.350	0.400	0.450
c	0.210	0.250	0.340
D	4.800	-	5.100
D1	4.800	4.900	5.000
D2	3.910	4.010	4.110
E	5.900	6.000	6.100
E1	5.700	5.750	5.800
E2	3.340	3.440	3.540
e	1.270 BSC		
H	0.510	0.610	0.710
k	1.100	-	-
L	0.510	0.610	0.710
L1	0.060	0.130	0.200
L2	-	-	0.100
P	1.000	1.100	1.200
θ	8°	10°	12°

NOTE: This drawing is subject to change without notice.

Revision History

Rev.	Change	Date
V1.0	Initial version	6/27/2021

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