

Product Summary

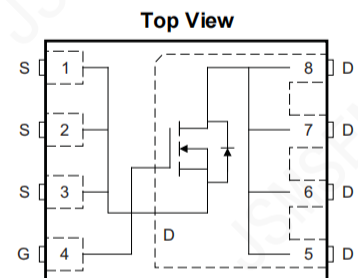
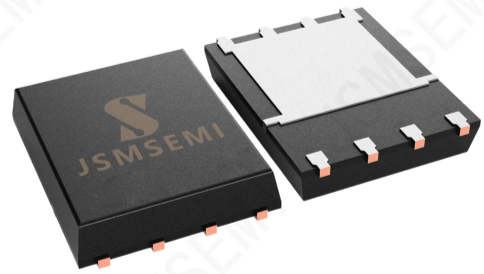
- V_{DS} 40V
- I_D 120A
- $R_{DS(ON)}$ (at $V_{GS}=10V$) <3.0m Ω
- 100% EAS Tested
- 100% ∇V_{DS} Tested

General Description

- Split gate trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Power switching application
- Uninterruptible power supply
- DC-DC convertor



Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Rating	Unit
Common Ratings			
V_{DSS}	Drain-Source Voltage	40	V
V_{GSS}	Gate-Source Voltage	± 20	
I_D^G	Continuous Drain Current	$T_C=25^\circ\text{C}$ 120 ^G	A
		$T_C=25^\circ\text{C}$ 205 ^I	
		$T_C=100^\circ\text{C}$ 85 ^G	
I_{DM}^C	Pulsed Drain Current	480	
I_{DSM}	Continuous Drain Current	$T_A=25^\circ\text{C}$ 40	A
		$T_A=70^\circ\text{C}$ 32	
P_D^B	Power Dissipation	$T_C=25^\circ\text{C}$ 157	W
		$T_C=100^\circ\text{C}$ 62	
I_S^G	Diode Continuous Forward Current	120	A
T_{STG}, T_J	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
P_{DSM}	Power Dissipation	$T_A=25^\circ\text{C}$ 6.2	W
		$T_A=70^\circ\text{C}$ 4	
I_{AS}^C	Single pulsed avalanche Current	47	A
E_{AS}^C	Single pulsed avalanche energy	$L=0.3\text{mH}$ 331	mJ
$R_{\theta JC}$	Thermal Resistance-Junction to Case	0.8	$^\circ\text{C/W}$
$R_{\theta JA}^{AD}$	Thermal Resistance-Junction to Ambient	$t \leq 10\text{S}$ 20	
		Steady State 50	

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	40			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =40V, V _{GS} =0V T _J =55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±20V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1	1.8	2.5	V
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =20A T _J =125°C		2.0 3.2	3.0 4	mΩ
		V _{GS} =4.5V, I _D =20A		3.1	3.9	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =20A		100		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.7	1	V
I _S	Maximum Body-Diode Continuous Current ^G				120	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =20V, f=1MHz		1825		pF
C _{oss}	Output Capacitance			895		pF
C _{rss}	Reverse Transfer Capacitance			55		pF
R _g	Gate resistance	f=1MHz	1	2	3.1	Ω
SWITCHING PARAMETERS						
Q _g (10V)	Total Gate Charge	V _{GS} =10V, V _{DS} =20V, I _D =20A		68	95	nC
Q _g (4.5V)	Total Gate Charge			28	40	nC
Q _{gs}	Gate Source Charge			16.5		nC
Q _{gd}	Gate Drain Charge			4.5		nC
Q _{oss}	Output Charge	V _{GS} =0V, V _{DS} =20V		37		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =20V, R _L =1Ω, R _{GEN} =3Ω		12.5		ns
t _r	Turn-On Rise Time			9.5		ns
t _{D(off)}	Turn-Off DelayTime			57.5		ns
t _f	Turn-Off Fall Time			10.5		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =20A, di/dt=500A/μs		20		ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =20A, di/dt=500A/μs		60		nC

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The Power dissipation P_{DSM} is based on R_{θJA} ≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on T_{J(MAX)}=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Single pulse width limited by junction temperature T_{J(MAX)}=150° C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=150° C. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.

I. The maximum current rating is silicon limited

Ordering Information

Order number	Package	Marking	Operation Temperature Range	MSL Grade	Ship, Quantity	Green
JSM030N04QG5L	DFN5060-8L	030N04QGL	-55 to 150°C	1	T&R,5000	Rohs

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

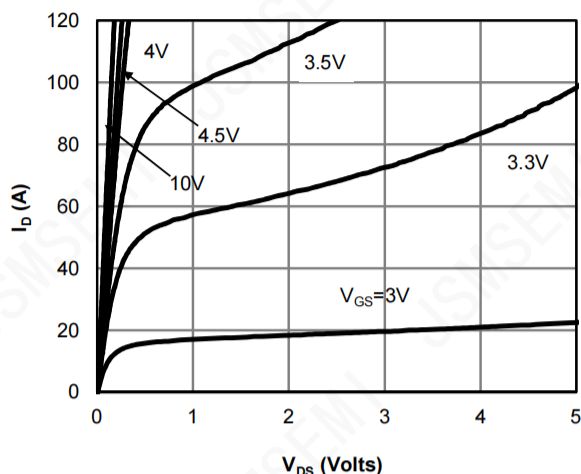


Figure 1: On-Region Characteristics (Note E)

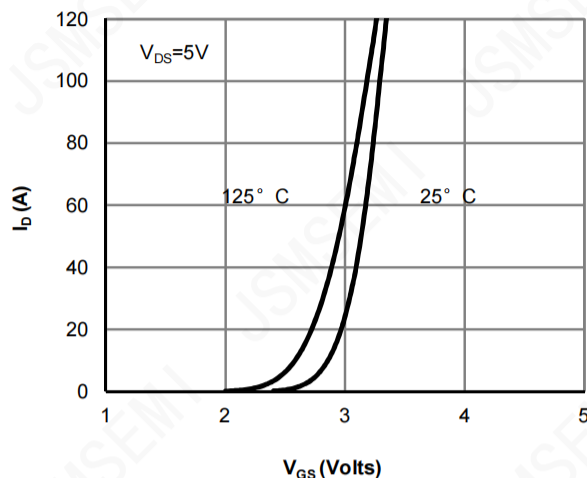


Figure 2: Transfer Characteristics (Note E)

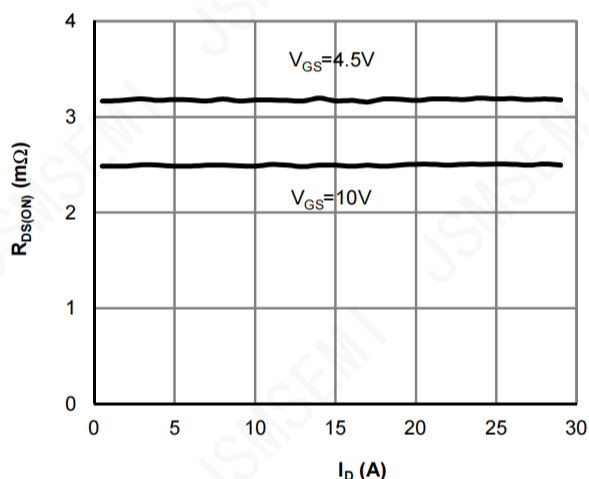


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

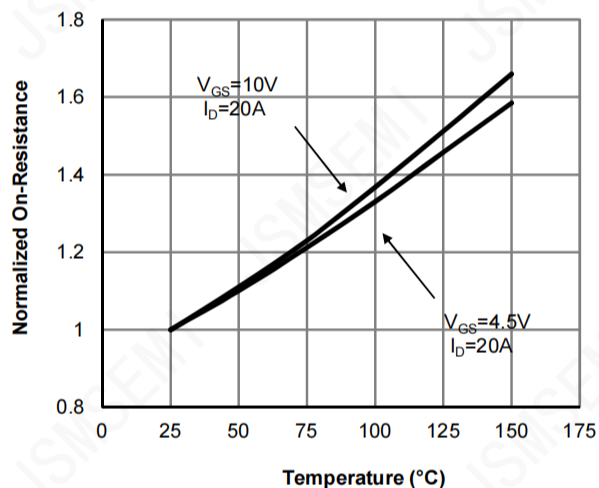


Figure 4: On-Resistance vs. Junction Temperature (Note E)

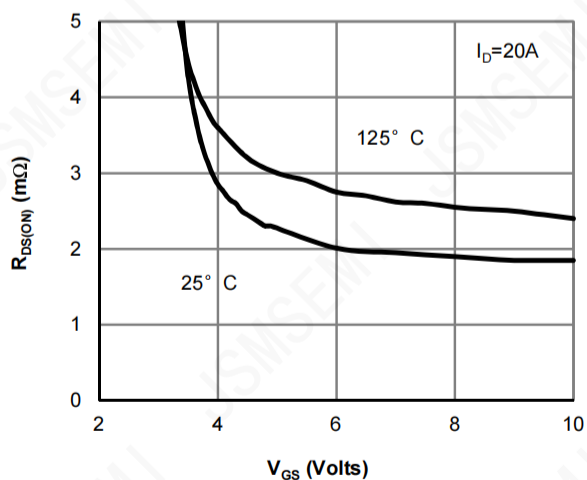


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

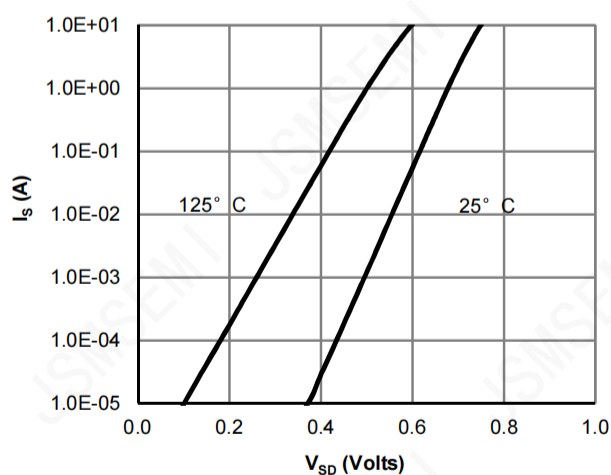
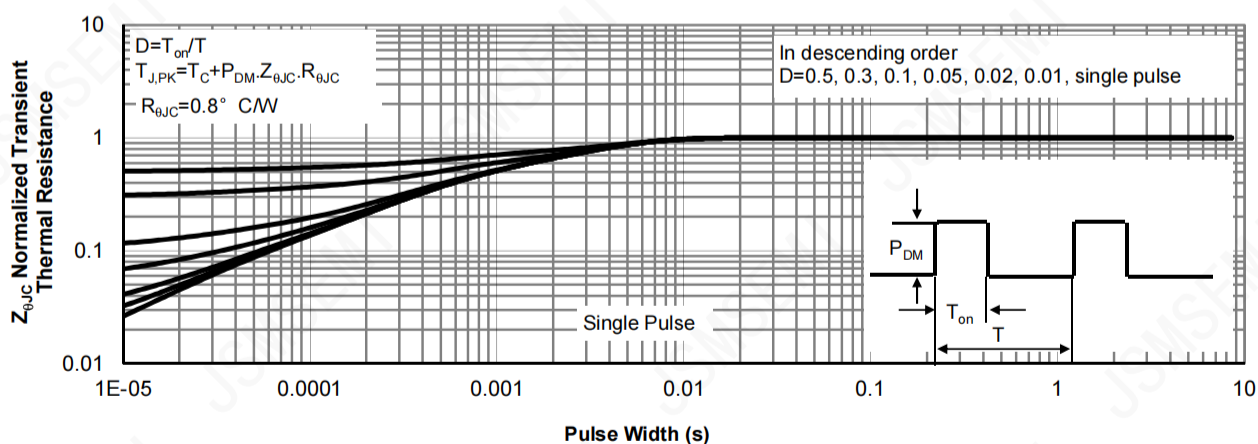
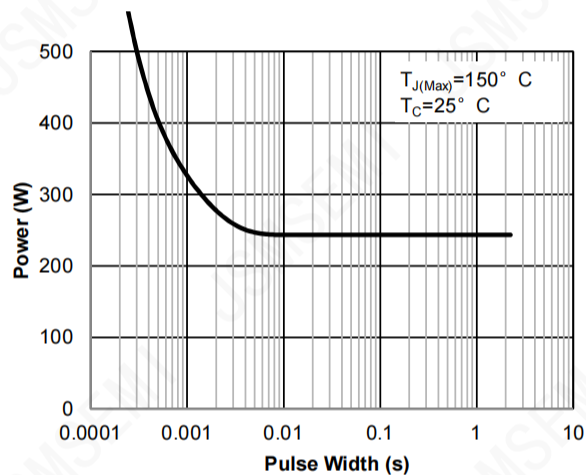
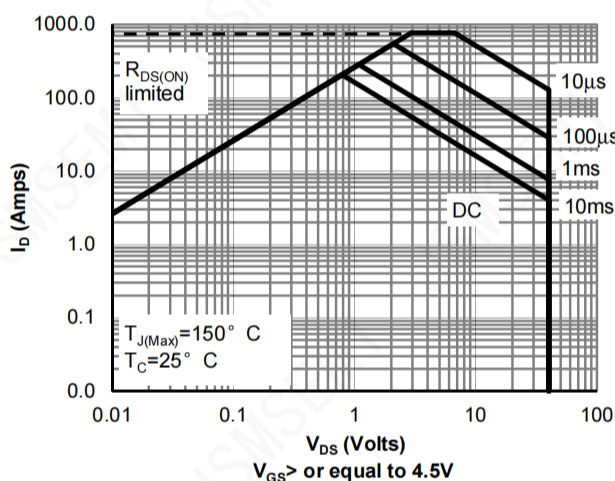
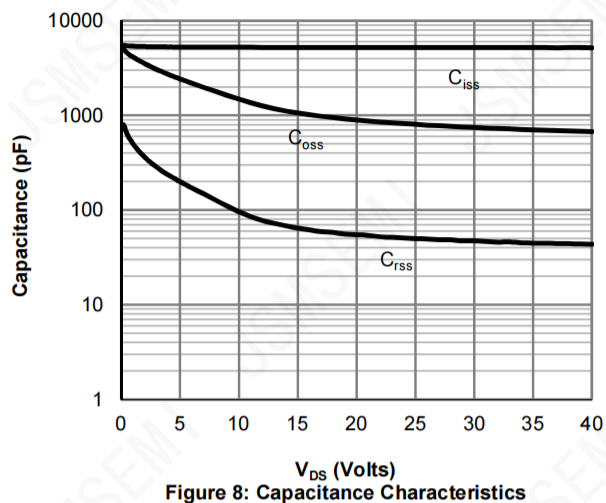
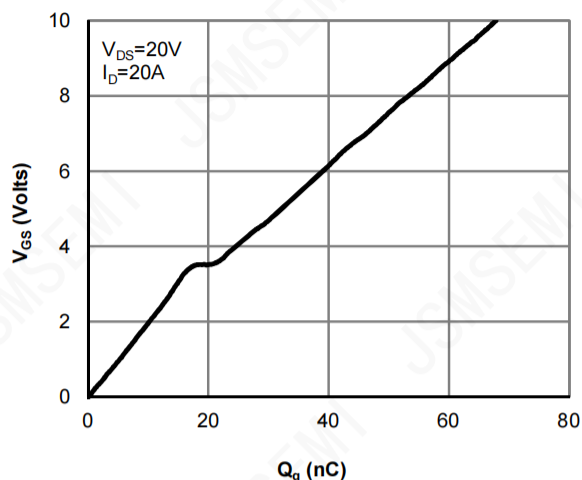


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS


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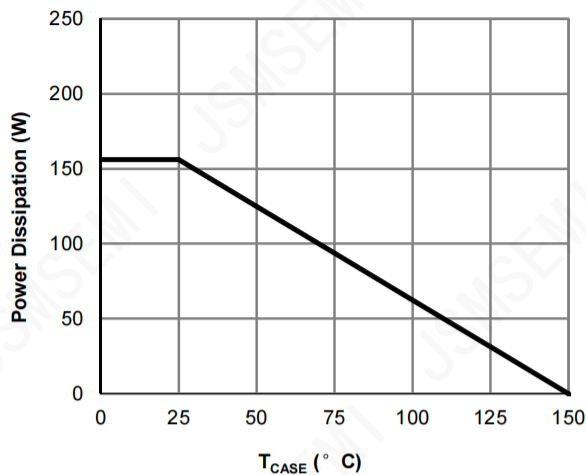


Figure 12: Power De-rating (Note F)

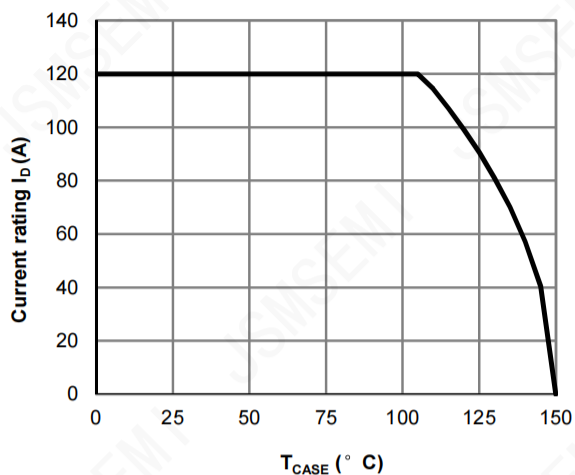


Figure 13: Current De-rating (Note F)

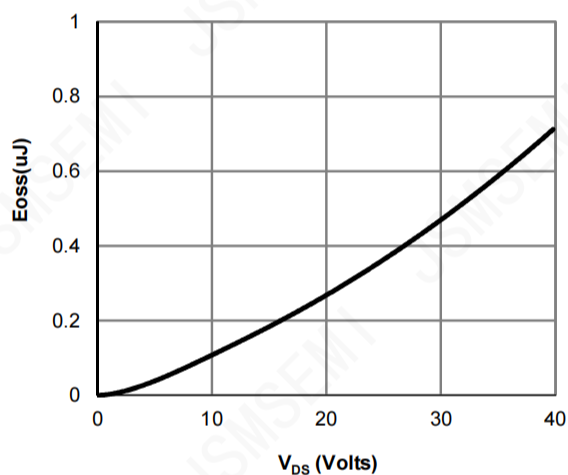


Figure 14: Coss stored Energy

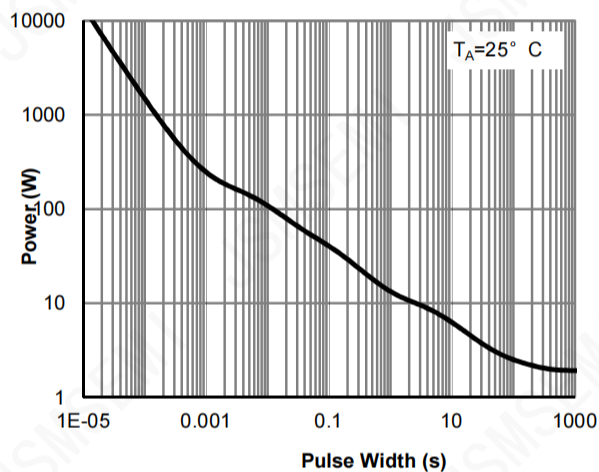


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

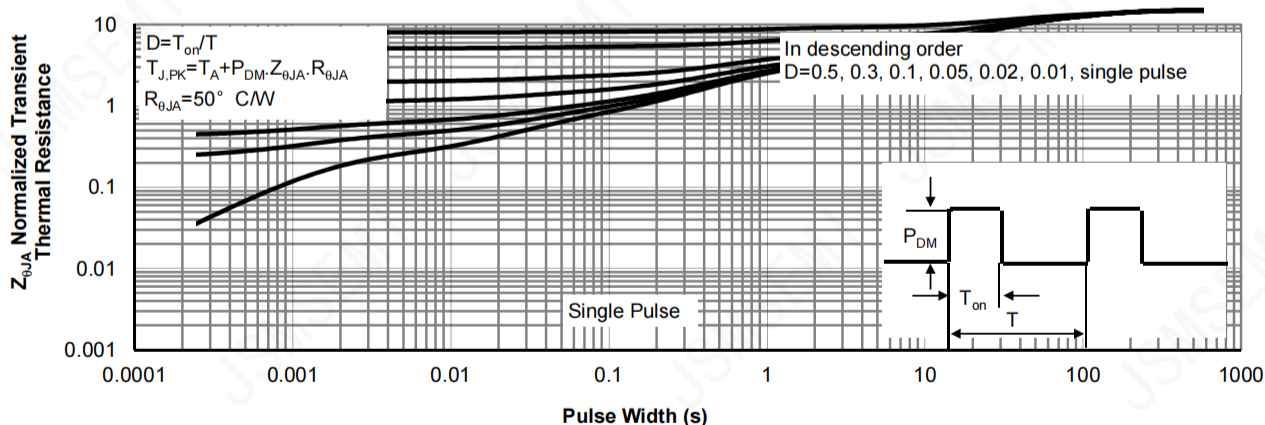


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

Figure A: Gate Charge Test Circuit & Waveforms

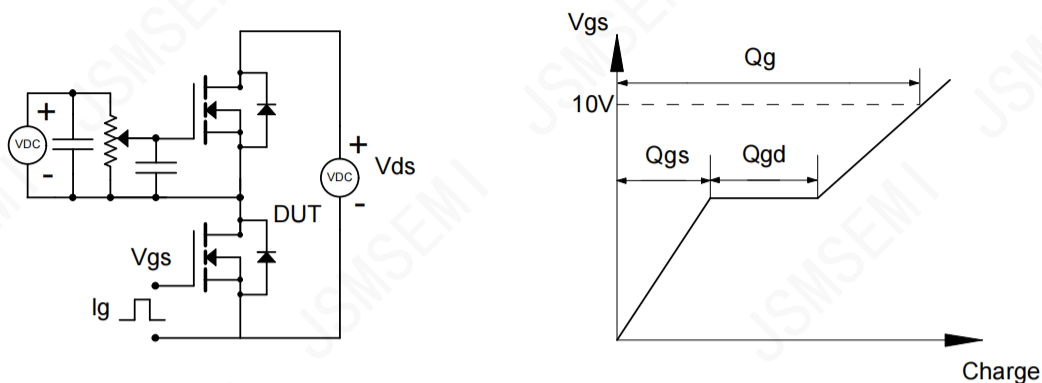


Figure B: Resistive Switching Test Circuit & Waveforms

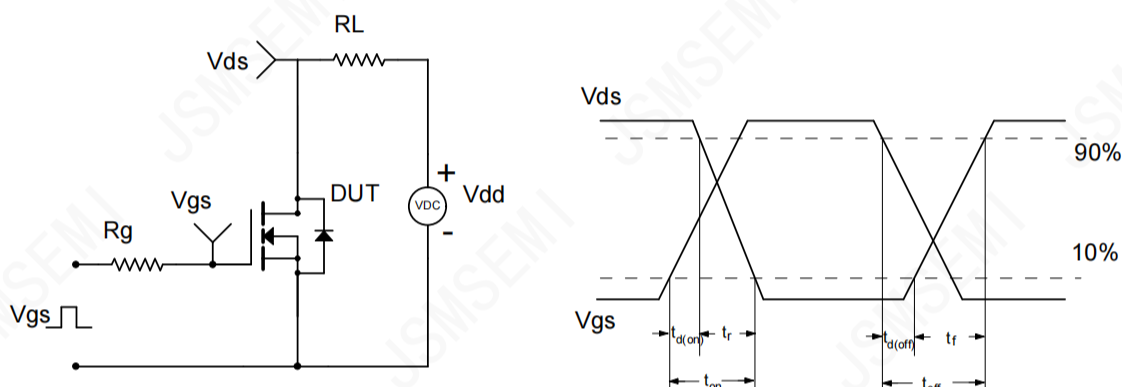


Figure C: Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

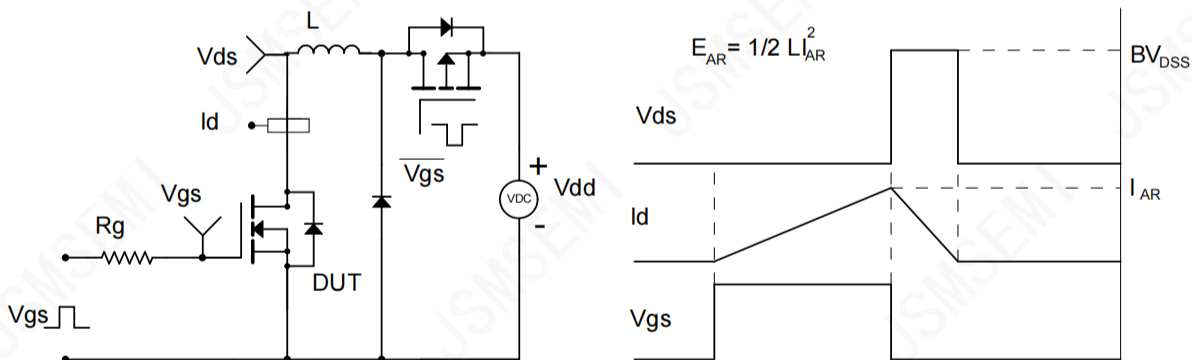
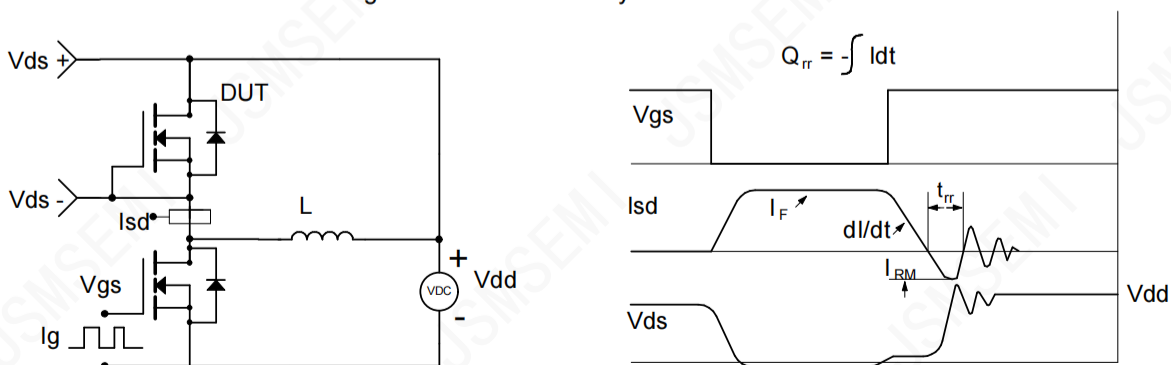
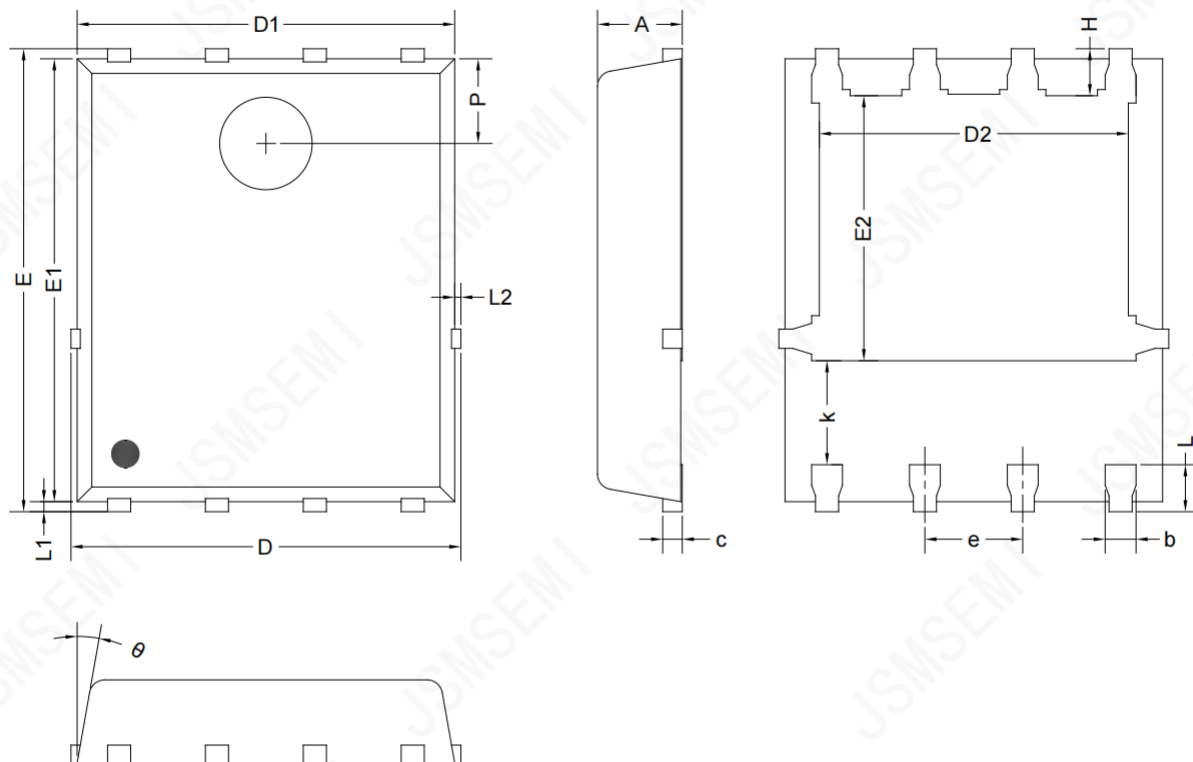


Figure D: Diode Recovery Test Circuit & Waveforms



Package Information

PDFN5060-8L



Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	1.000	1.100	1.200
b	0.350	0.400	0.450
c	0.210	0.250	0.340
D	4.800	-	5.100
D1	4.800	4.900	5.000
D2	3.910	4.010	4.110
E	5.900	6.000	6.100
E1	5.700	5.750	5.800
E2	3.340	3.440	3.540
e	1.270 BSC		
H	0.510	0.610	0.710
k	1.100	-	-
L	0.510	0.610	0.710
L1	0.060	0.130	0.200
L2	-	-	0.100
P	1.000	1.100	1.200
θ	8°	10°	12°

NOTE: This drawing is subject to change without notice.

Revision History

Rev.	Change	Date
V1.0	Initial version	6/27/2021

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