1 Description

The JSM27712 is a 650-V high-side and low-side gate driver with 4.5-A source, 5.0-A sink current, targeted to drive power MOSFETs or IGBTs.

The recommended VDD operating voltage is 10-V to 20-V for IGBT's and 10-V to 17-V for power MOSFETs.

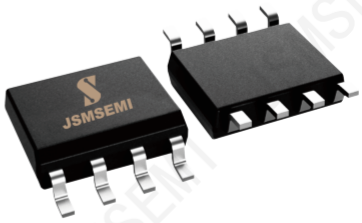
The JSM27712 includes protection features where the outputs are held low when the inputs are left open or when the minimum input pulse width specification is not met. Interlock and deadtime functions prevent both outputs from being turned on simultaneously. In addition, the device accepts a wide range bias supply range and offers UVLO protection for both the VDD and HB bias supply.

Developed with TI's state of the art high-voltage device technology, the device features robust drive with excellent noise and transient immunity including large negative voltage tolerance on its inputs, high dV/dt tolerance, wide negative transient safe operating area (NTSOA) on the switch node (HS), and interlock.

The device consists of one ground-referenced channel (LO) and one floating channel (HO) which is designed for operating with bootstrap or isolated power supplies. The device features fast propagation delays and excellent delay matching between both channels. On the JSM27712, each channel is controlled by its respective input pins, HI and LI.

2 Features

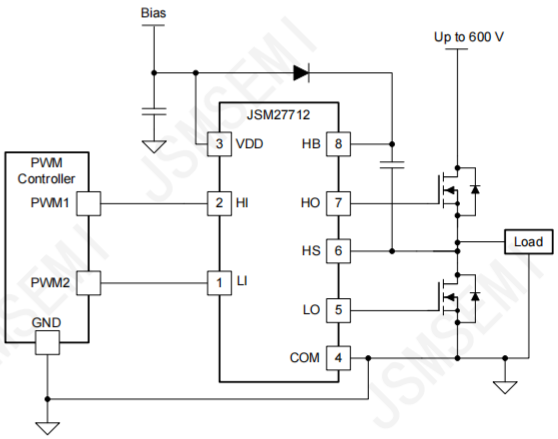
- High-Side and Low-Side Configuration
- Dual Inputs With Output Interlock and 300-ns Deadtime
- Fully Operational up to 650-V, 700-V Absolute Maximum on HB Pin
- 10-V to 20-V VDD Recommended Range
- Peak Output Current 5.0-A Sink, 4.5-A Source
- dv/dt Immunity of 50 V/ns
- Logic Operational up to –11 V on HS Pin
- Negative Voltage Tolerance On Inputs of –10V
- Large Negative Transient Safe Operating Area
- UVLO Protection for Both Channels
- Small Propagation Delay (160-ns Typical)
- Delay Matching (20-ns Typical)
- Floating Channel Designed for Bootstrap Operation
- Low Quiescent Current
- TTL and CMOS Compatible Inputs
- Industry Standard SOIC-8 Package
- All Parameters Specified Over Temperature Range, –40 °C to +125 °C



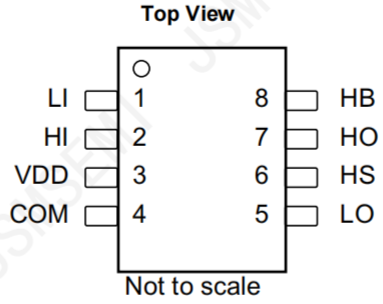
3 Applications

- Motor Drive (Stepper Motors, HVAC, Fans, Power Tools, Robotics, Drones)
- Bridge Converters in Offline AC/DC Power Supplies
- High-Density Switch Mode Power Supplies for Server, Telecom, IT and Industrial Infrastructures
- DC-to-AC Inverters

Simplified Schematic



4 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
COM	4	–	Ground
HB	8	I	High-side floating supply. Bypass this pin to HS with a suitable capacitor to sustain boot-strap circuit operation, typically 10 times bigger than the MOSFETs/IGBTs gate capacitance.
HI	2	I	Logic input for high-side driver. If HI is unbiased or floating, HO is held low
HO	7	O	High-side driver output.
HS	6	–	Return for high-side floating supply.
LI	1	I	Logic input for low-side driver. If LI is unbiased or floating, LO is held low
LO	5	O	Low-side driver output.
VDD	3	I	Bias supply input. Power supply for the input logic side of the device and also low-side driver output. Bypass this pin to COM with a 0.1-μF or larger value ceramic capacitor.

Ordering Information

Ordernumber	Package	Marking information	Operation Temperature Range	MSL Grade	Ship,Quantity	Green
UCC27712DR-JSM	SOP-8	JSM27712S	-40 to 125°C	3	T&R,4000	Rohs

5 Specifications

Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted). All voltages are with respect to COM (unless otherwise noted), currents are positive into and negative out of the specified terminal. (T_A) ≥ 25°C.

PARAMETER			MIN	MAX	UNIT
Input voltage	HI, LI		–5	25	V
	VDD supply voltage		–0.3	25	
	HB		–0.3	700	
	HB–HS		–0.3	25	
Output voltage	HO	DC	HS–0.3	HB+0.3	V
		Transient, less than 100 ns	HS–2	HB+0.3	
	LO	DC	–0.3	VDD+0.3	V
		Transient, less than 100 ns	–2	VDD+0.3	
Output current	HO, LO	I_{OUT_PULSED} (100 ns)		5.0/4.5	A
		I_{OUT_DC}		0.5	
dV_{HS}/dt	Allowable offset supply voltage transient			50	V/ns
T_J	Junction temperature		–40	150	°C
T_{stg}	Storage temperature		–55	150	

NOTE:
Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device.These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM)	±2000	V
		Charged device model (CDM)	±1000	

Recommended Operating Conditions

All voltages are with respect to COM, over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
VDD	Supply voltage	IGBT applications	10		20	V
		MOSFET applications	10		17	
HB–HS	Driver bootstrap voltage	IGBT applications	10		20	
		MOSFET applications	10		17	
HS	Source terminal voltage (1)		–11		600	
HI, LI	Input voltage with respect to COM		–4		20	
T_A	Ambient temperature		–40		125	°C

(1) Logic operational for HS of –11 V to +600 V at HB–HS = 15 V

Thermal Information

THERMAL METRIC		JSM27712 (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	150	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	65.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	60.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	19.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	65.2	°C/W

Electrical Characteristics

At VDD = VHB = 15 V, COM = VHS = 0, all voltages are with respect to COM, no load on LO and HO, –40°C < T_J < +125°C (unless otherwise noted). Currents are positive into and negative out of the specified terminal.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY BLOCK						
$V_{VDD\ ON}$	Turn-on threshold voltage of VDD		8.0	8.5	9.5	V
$V_{VDD\ OFF}$	Turn-off threshold voltage of VDD		7.2	8.0	8.6	
$V_{VDD\ HYS}$	Hysteresis of VDD			0.9		
$V_{VHB\ ON}$	Turn-on threshold voltage of VHB–VHS		7.5	8.5	9.5	
$V_{VHB\ OFF}$	Turn-off threshold voltage of VHB–VHS		6.9	7.7	8.5	
$V_{VHB\ HYS}$	Hysteresis of VHB–VHS			0.8		
I_Q	Total quiescent supply current	HI = LI = 0 V or 5 V, DC on/off state		240	360	µA
I_{QVDD}	Quiescent VDD-COM supply current	HI = LI = 0 V or 5 V, DC on/off state		200	350	
I_{QBS}	Quiescent HB-HS supply current	HI = 0 V or 5 V, HO in DC on/off state		50	100	
I_{BL}	Bootstrap supply leakage current	HB = HS = 600 V			20	
I_{OP}	Dynamic operating current	HI = LI = 0 V or 5 V, f = 100 kHz, duty = 50%, C_L= 1 nF		3800	4500	
INPUT BLOCK						
V_{INH}	Input Pin (HI, LI) high threshold			2.2	2.6	V
V_{INL}	Input Pin (HI, LI) low threshold		0.8	1.5		
V_{INHYS}	Input Pin (HI, LI) threshold hysteresis			0.8		
I_{INL}	HI, LI input low bias current	HI, LI = 0 V			2	µA
I_{INH}	HI, LI input high bias current	HI, LI = 5 V			60	
OUTPUT BLOCK						
V_{DD}-V_{LOH}	LO output high voltage	LI = 5 V, I_{LO} = –20 mA		60		mV
V_{HB}-V_{HOH}	HO output high voltage	HI = 5 V, I_{HO} = –20 mA		60		
V_{LOL}	LO output low voltage	LI = 0 V, I_{LO} = 20 mA		30		
V_{HOL}	HO output low voltage	HI = 0 V, I_{HO} = 20 mA		30		
I_{GPK-} (1)	HO, LO output low short circuit pulsed current	HI = LI = 0 V, HO = LO = 15 V, PW < 10 µs		5.0		A
I_{GPK+} (1)	HO, LO output high short circuit pulsed current	HI = LI = 5 V, HO = LO = 0 V, PW < 10 µs		4.5		

Dynamic Electrical Characteristics

At VDD = VHB = 15 V, COM = VHS = 0, all voltages are with respect to COM, no load on LO and HO, –40°C < T_J < +125°C (unless otherwise noted). Currents are positive into and negative out of the specified terminal.

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
DYNAMIC CHARACTERISTICS						
t_{PDLH}	Turn-on propagation delay (without deadtime)	LI to LO, HI to HO, HS = COM = 0 V		160	280	ns
t_{PDHL}	Turn-off propagation delay	LI to LO, HI to HO, HS = COM = 0 V		160	280	
t_{RISE}	Turn-on rise time	10% to 90%, HO/LO with 1000-pF load		15	50	
t_{FALL}	Turn-off fall time	10% to 90%, HO/LO with 1000-pF load		10	30	
t_{ON}	Minimum HI/LI ON pulse that changes output state	0-V to 5-V input signal on HI and LI pins		20	50	
t_{OFF}	Minimum HI/LI OFF pulse that changes output state	5-V to 0-V input signal on HI and LI pins		20	50	
DT	Deadtime	Internal deadtime for Interlock	200	300	400	

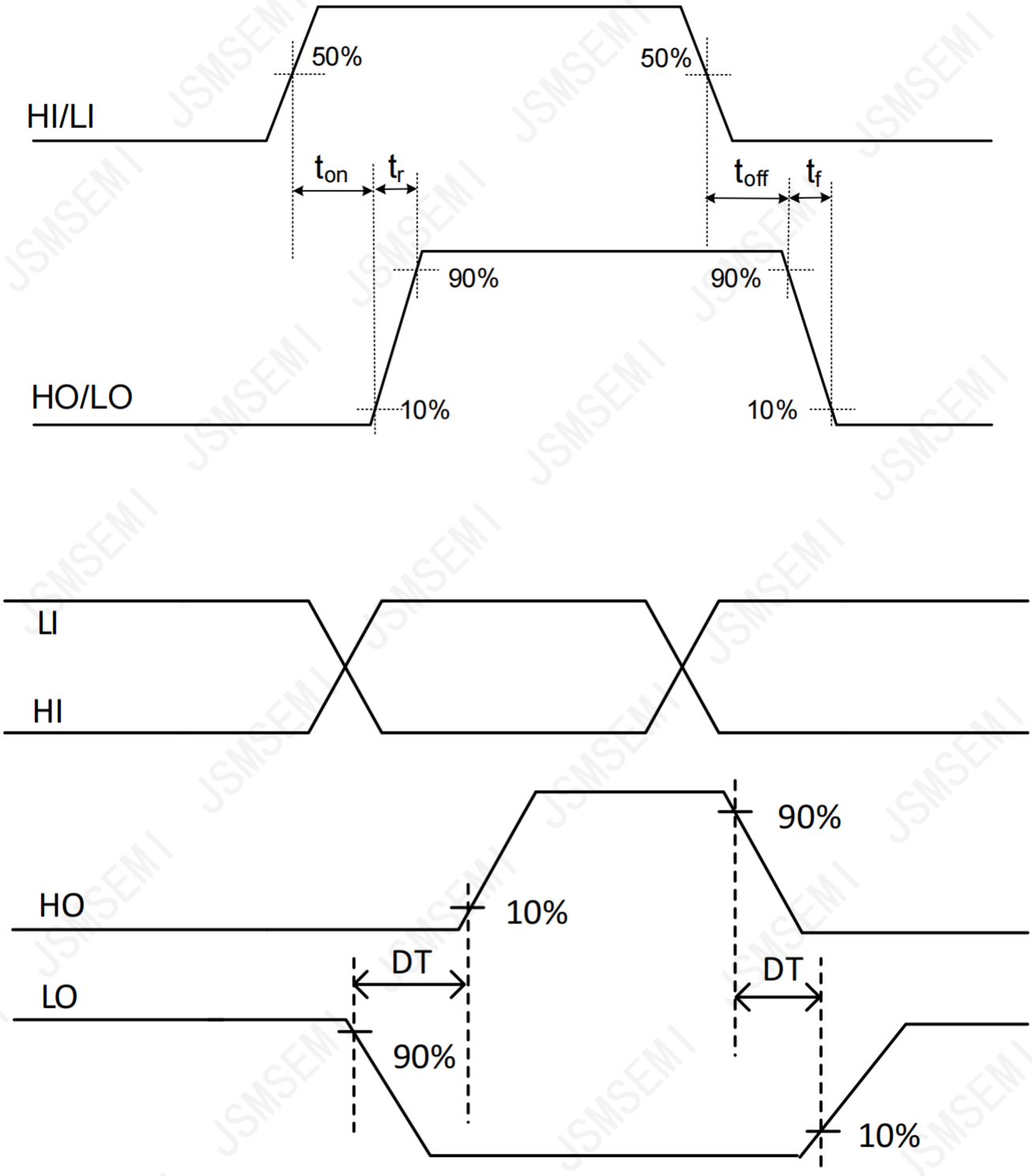


Figure 1. Typical Test Timing Diagram

6 Detailed Description

Overview

The JSM27712 consists of one ground-referenced channel (LO) and one floating channel (HO) which is designed for operating with bootstrap or isolated power supplies. The device features fast propagation delays and excellent delay matching between both channels. On the JSM27712, each channel is controlled by its respective input pins,

Developed with TI's state of the art high-voltage technology, the device features robust drive with excellent noise and transient immunity including large negative voltage tolerance on its inputs, high dv/dt tolerance, and wide negative transient safe operating area (NTSOA) on the switch node (HS).

The JSM27712 includes protection features where the outputs are held low when the inputs are floating or when the minimum input pulse width specification is not met. Interlock and deadtime functions prevent both outputs from being turned on simultaneously. In addition, the device accepts a wide range bias supply range from 10 V ~ 20 V, and offers UVLO protection for both the VDD and HB bias supply.

High-current, gate-driver devices are required in switching power applications for a variety of reasons. In order to implement fast switching of power devices and reduce associated switching power losses, a powerful gate-driver device is employed between the PWM output of control devices and the gates of the power semiconductor devices. Further, gate-driver devices are indispensable when having the PWM controller device directly drive the gates of the switching devices is sometimes not feasible. In the case of digital power supply controllers, this situation is often encountered because the PWM signal from the digital controller is often a 3.3-V logic signal which is not capable of effectively turning on a power switch.

In bridge topologies, like hard-switch half bridge, hard-switch full bridge, half-bridge and full-bridge LLC, and phase-shift full bridge, the source and emitter pin of the top-side power MOSFET and IGBT switch is referenced to a node whose voltage changes dynamically; that is, not referenced to a fixed potential, so floating-driver devices are necessary in these topologies.

The JSM27712 is a high-side and low-side driver dedicated for offline AC-to-DC power supplies and inverters. The high side is a floating driver that can be biased effectively using a bootstrap circuit, and can handle up to 600-V. The driver can be used with 100% duty cycle as long as HB-HS can be above UVLO of the high side.

The device features industry best-in-class propagation delay and delay matching between both channels aimed at minimizing pulse width distortion in high-frequency switching applications. Each channel is controlled by its respective input pins (HI and LI), allowing independent flexibility to control on and off state of the output but does not allow the HO and LO outputs to be on at the same time. The JSM27712 includes an interlock feature which guarantees a 150ns dead time between the HO and LO outputs if the HI and LI inputs are complimentary. The JSM27712 includes protection features wherein the outputs are held low when inputs are floating or when the minimum input pulse width specification is not met. The driver inputs are CMOS and TTL compatible for easy interface to digital power controllers and analog controllers alike.

Functional Block Diagram

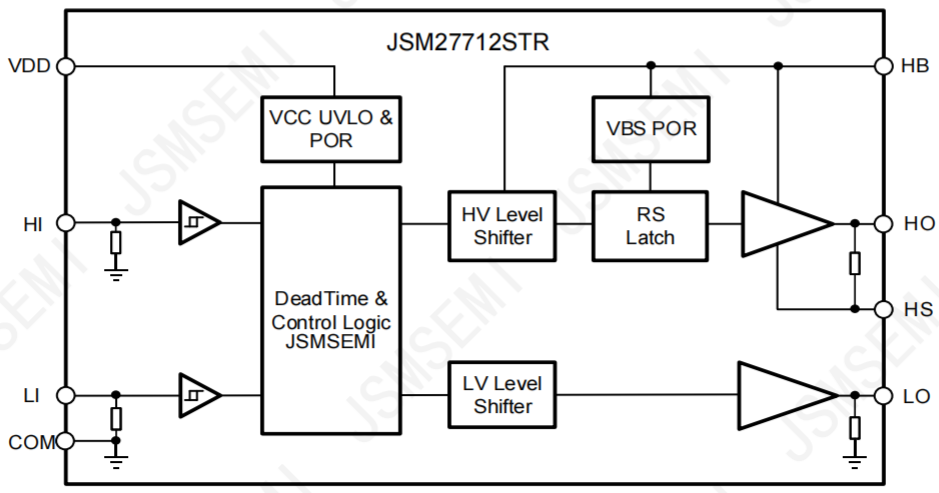


Figure 2. JSM27712 Block Diagram

Feature Description

VDD and Under Voltage Lockout

The JSM27712 has an internal under voltage-lockout (UVLO) protection feature on the supply circuit blocks between VDD and VSS pins, as well as between HB and HS pins. When VDD bias voltage is lower than the $V_{VDD(on)}$ threshold at device start-up or lower than $V_{VDD(off)}$ after start-up, the VDD UVLO feature holds both the LO and HO outputs low, regardless of the status of the HI and LI inputs. On the other hand, if HB-HS bias supply voltage is lower than the $V_{VHB(on)}$ threshold at start-up or $V_{VHB(off)}$ after start-up, the HB-HS UVLO feature only holds HO to low, regardless of the status of the HI. The LO output status is not affected by the HB-HS UVLO feature (see Table 1 and Table 2). This allows the LO output to turn-on and re-charge the HB-HS capacitor using the boot-strap circuit and thus allows HB-HS bias voltage to surpass the $V_{VHB(on)}$ threshold.

Both the VDD and VHB UVLO protection functions are provided with a hysteresis feature. This hysteresis prevents chatter when there is ground noise from the power supply. Also this allows the device to accept a small drop in the bias voltage which is bound to happen when the device starts switching and quiescent current consumption increases instantaneously, as well as when the boot-strap circuit charges the HB-HS capacitor during the first instance of LO turn-on causing a drop in VDD voltage.

The UVLO circuit of VDD-VSS and HB-HS in JSM27712 generate internal signals to enable/disable the outputs after UVLO_ON/UVLO_OFF thresholds are crossed respectively (please refer to Figure 3). Design considerations indicate that the UVLO propagation delay before the outputs are enabled and disabled can vary from 20 μs to 50 μs.

Table 1. VDD UVLO Feature Logic Operation

CONDITION (VHB-VHS>$V_{VHB,\ ON}$ FOR ALL CASES BELOW)	HI	LI	HO	LO
VDD-VSS < $V_{VDD(on)}$ during device start up	H	L	L	L
VDD-VSS < $V_{VDD(on)}$ during device start up	L	H	L	L
VDD-VSS < $V_{VDD(on)}$ during device start up	H	H	L	L
VDD-VSS < $V_{VDD(on)}$ during device start up	L	L	L	L
VDD-VSS < $V_{VDD(off)}$ after device start up	H	L	L	L
VDD-VSS < $V_{VDD(off)}$ after device start up	L	H	L	L
VDD-VSS < $V_{VDD(off)}$ after device start up	H	H	L	L
VDD-VSS < $V_{VDD(off)}$ after device start up	L	L	L	L

Table 2. VHB UVLO Feature Logic Operation

CONDITION (VDD-VSS > $V_{VDD,ON}$ FOR ALL CASES BELOW)	HI	LI	HO	LO
VHB-VHS < $V_{VHB(on)}$ during device start up	H	L	L	L
VHB-VHS < $V_{VHB(on)}$ during device start up	L	H	L	H
VHB-VHS < $V_{VHB(on)}$ during device start up	H	H	L	L
VHB-VHS < $V_{VHB(on)}$ during device start up	L	L	L	L
VHB-VHS < $V_{VHB(off)}$ after device start up	H	L	L	L
VHB-VHS < $V_{VHB(off)}$ after device start up	L	H	L	H
VHB-VHS < $V_{VHB(off)}$ after device start up	H	H	L	L
VHB-VHS < $V_{VHB(off)}$ after device start up	L	L	L	L

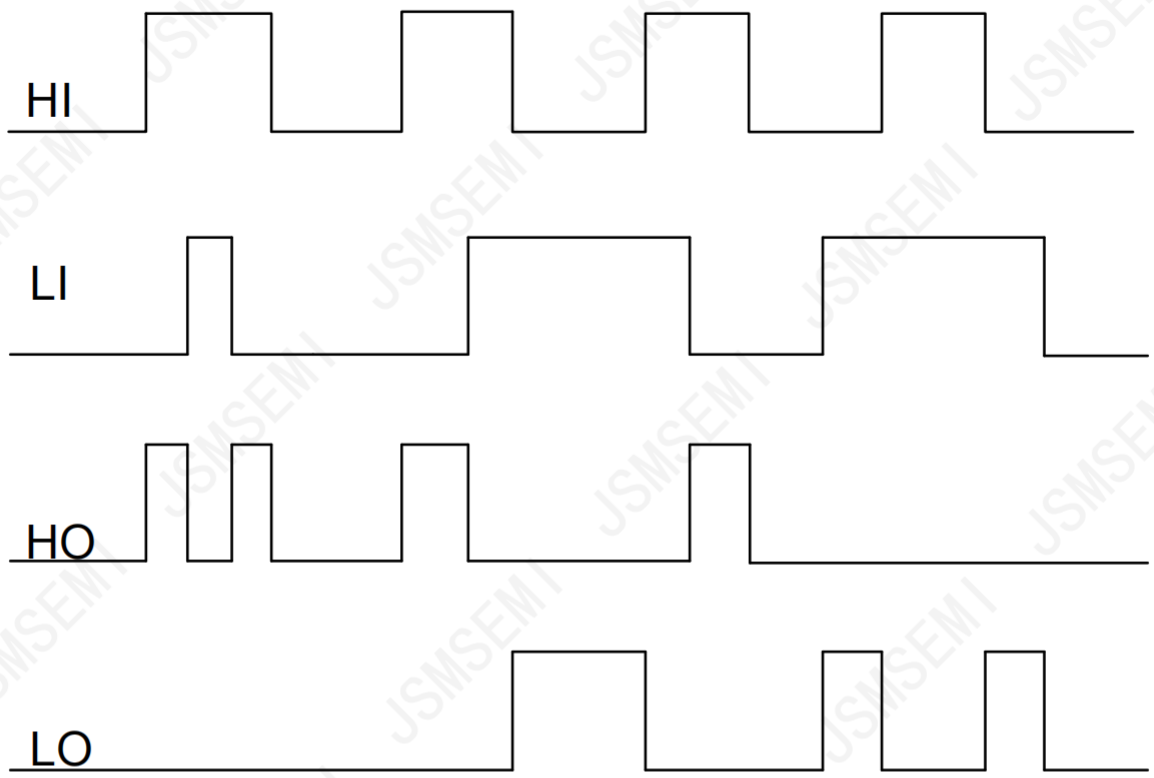


Figure 3. Power-Up Driver

Input and Output Logic Table

JSM27712 features separate inputs, HI and LI, for controlling the state of the outputs, HO and LO, respectively. The device does include internal cross-conduction prevention logic and does not allow both HO and LO outputs to be turned on simultaneously (refer to Table 3). This feature prevents cross conduction in bridge topologies in the case of incorrect timing from the controller.

Table 3. Input/Output Logic Table
(Assuming no UVLO fault condition exists for VDD and VHB)

HI	LI	HO	LO	Note
L	L	L	L	
L	H	L	H	Output transitions occur after the dead time expires
H	L	H	L	
H	H	L	L	
Left Open	Left Open	L	L	

7 Application and Implementation

Application Information

To effect fast switching of power devices and reduce associated switching power losses, a powerful gate driver is employed between the PWM output of controllers and the gates of the power semiconductor devices. Also, gate drivers are indispensable when it is impossible for the PWM controller to directly drive the gates of the switching devices. With the advent of digital power, this situation will be often encountered because the PWM signal from the digital controller is often a 3.3-V logic signal which cannot effectively turn on a power switch. Level shifting circuitry is needed to boost the 3.3-V signal to the gate-drive voltage (such as 12 V) in order to fully turn on the power device and minimize conduction losses. Traditional buffer drive circuits based on NPN/PNP bipolar transistors in totem-pole arrangement, being emitter follower configurations, prove inadequate with digital power because they lack level-shifting capability.

Gate drivers effectively combine both the level-shifting and buffer-drive functions. Gate drivers also find other needs such as minimizing the effect of high-frequency switching noise by locating the high-current driver physically close to the power switch, driving gate-drive transformers and controlling floating power-device gates, reducing power dissipation and thermal stress in controllers by moving gate charge power losses from the controller into the driver.

Typical Application

The circuit in Figure 4 shows a reference design example with JSM27712 driving a typical half-bridge configuration which could be used in several common power converter topologies such as synchronous buck, synchronous boost, half-bridge/full bridge isolated topologies, and motor drive applications.

For more information, please refer to Figure 4.

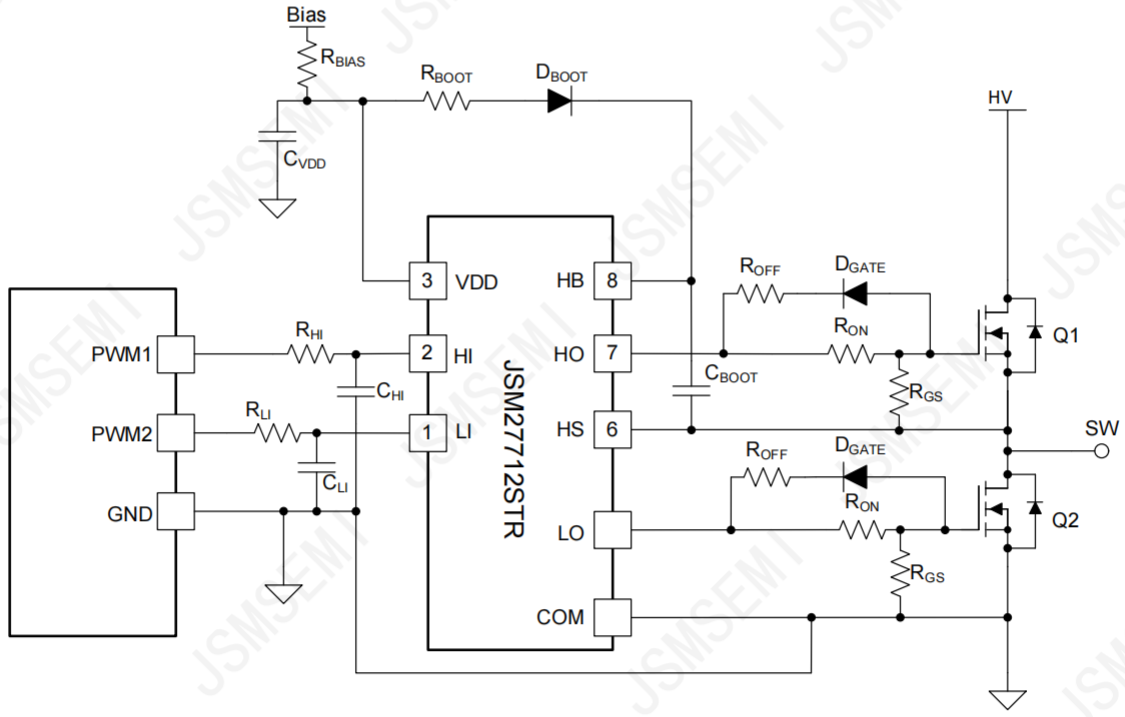


Figure 4. Typical Application Schematic

Bootstrap Circuit Design Guide

The structure of a general half-bridge circuit is shown in Figure 5, including bootstrap resistance, bootstrap diode and bootstrap capacitor. This scheme is the most commonly used and cost-effective scheme in the current motor drive.

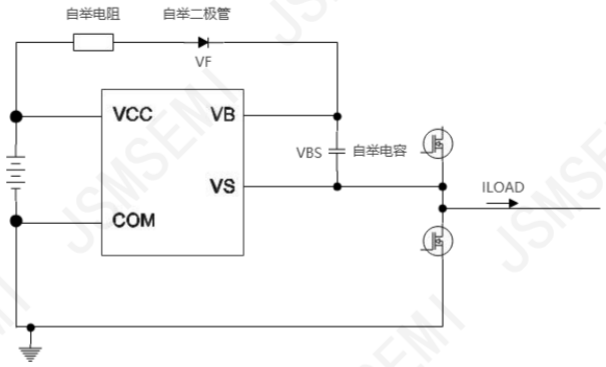


Figure 5 Basic structure of the bootstrap circuit

Bootstrap circuit capacitance selection

In order to determine the size of the bootstrap capacitance, we first need to evaluate the following points:

-The gate charge required for MOS to turn on: Q_g;

-GS leakage of MOS: I_{LK_GS};

-Static operating current of the drive: I_{QBS};

-Leakage of bootstrap diode: I_{LK_DIODE};

-Bootstrap capacitor leakage: I_{LK_CAP};

-Upper bridge height time: T_{HON}.

I_{LK_CAP} is included in the calculation only when the bootstrappable capacitor uses an electrolytic capacitor. Other types of capacitors do not need to be considered. It is recommended to use at least one low ESR ceramic capacitor. Parallel electrolytic capacitor and low ESR ceramic capacitor can achieve better circuit performance.

By calculation, we can find the loss of capacitance for a single turn on:

$$Q_{TOT} = Q_G + (I_{LK\_GS} + I_{QBS} + I_{LK\_DIODE} + I_{LK\_CAP}) \times T_{HON}$$

Specifies the range that VBS can drop during bootstrapping: $\triangle V_{BS}$

$$\Delta V_{BS} \leq V_{CC} - V_F - V_{GSmin} - V_{DSon}$$

In the process, you need assurance:

$$V_{GSmin} > V_{BSUV-}$$

V_F MOS reverse diode voltage drop

V_{GEmin} Maintain the minimum gate voltage for MOS tube conduction

V_{DSon} On-off pressure drop of the lower bridge MOS

And with that, you can calculate it:

$$C_{BOOTmin} = \frac{Q_{TOT}}{\triangle V_{BS}}$$

Note: In the process of calculating bootstrap capacitance here, only the charge required for a pulse process is calculated, without considering the duty ratio and frequency of PWM. If the signal is controlled by PWM wave, please get the actual required bootstrap capacitance size based on the above calculation method through a certain equivalent conversion.

Note on bootstrap circuit

A. Bootstrap resistance

Bootstrap resistors are used in some bootstrap circuits and are not required. HO and LO may have abnormal jump during startup. At this time, the increase of bootstrap resistance will limit the current passing through the bootstrap diode when the bootstrap circuit is started, which can effectively suppress some bad signals and protect the circuit.

B. Bootstrap capacitor

ESR must be considered in the design of the circuit with the upper bridge arm open for a long time when the electrolytic capacitor is used as the bootstrap capacitor. When the upper bridge arm is opened for a long time, a bootstrap capacitor with a large capacity is required, and electrolytic capacitors are generally used. But the electrolytic capacitor has a certain internal resistance, which will reduce the partial voltage of bootstrap resistance and can not realize its function. This situation can be effectively avoided by connecting a ceramic capacitor with a low ESR.

C. Bootstrap diode

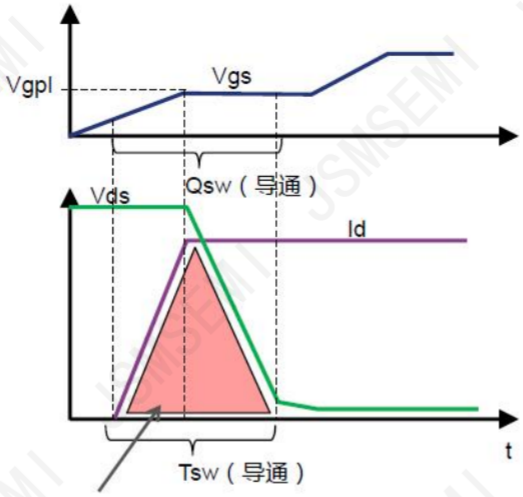
The bootstrap diode is used to maintain the voltage stability of the bootstrap circuit. It is necessary to ensure that the reverse voltage resistance of the diode is greater than the voltage of the driving power supply. On this basis, fast recovery diodes such as Schottky diodes are selected as much as possible.

Bootstrap Circuit Design Guide

Gate resistance is used to control the switching speed of the driven MOS and the slope of the rising and falling edge, which will affect a number of application performance, such as loss, reliability and so on. This section describes how to select the driving resistance and discusses the impact of the driving resistance. The selection of grid resistance is closely related to the driver chip, MOSFET and even circuit design, and it needs to be re-selected according to the actual situation in different environments.

Common industrial brushless motors operate at a frequency of about 2kHz-10kHz. Based on this, grid resistors of 20-120 Ω are usually selected. This is determined by the following two factors：

（1） **Switching loss of MOS.** Part of the MOS loss is switching loss, and the other part is on-off loss, while the grid resistance mainly affects the loss of the switching process. The larger the resistance value, the slower the switching process, and the larger the overlap area of voltage and current, the greater the loss. The most direct impact of excessive loss is that the chip temperature will rise rapidly, and the device will face the risk of failure under the condition of higher than 150℃.



$$Psw(on) = \frac{1}{2} \times Id \times Vds \times Tsw(on)$$

Figure 6 MOS switch loss under resistive load

（2） **Reliability.** As opposed to loss, the smaller the resistance value of the gate resistance, the faster the MOSFET will switch. In practical applications, the power end current is larger, more sensitive to parasitic parameters, too high switching speed will increase the signal instability, light will make the motor EMI is too large, heavy will make the circuit damage. Some of the most common are:

1) Grid signal rings, causing MOS damage (as shown in Figure 7);

2) The dv/dt is too fast, and the VS port will bear too high or too low voltage signal, resulting in drive damage.。

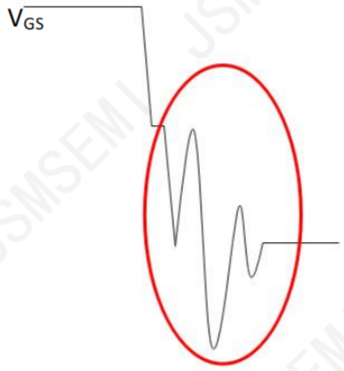


Figure 7 Grid ringing

PCB layout guide

To achieve the outstanding performance of half bridge grid driver chips, the following printed circuit board (PCB) layout routing guidelines should be followed.

• Low ESR/ESL capacitors should be placed near the driver chip between the VCC and COM pins, and between the VB and VS pins to provide peak current for the VCC and VB pins.

• To prevent large voltage transients from high-side MOSFET drains, a low ESR electrolytic capacitor and a ceramic capacitor must be connected between the high-side MOSFET drain and the ground (COM).

• To avoid excessive negative voltage transients on switch node (VS) pins, the parasitic inductance between the high-side MOSFET source and the low-side MOSFET (synchronous rectifier) source must be minimized.

• Overlap of the VS layer with the ground (COM) layer should be avoided as much as possible to minimize the coupling of switching noise from the VS layer to the ground layer.

• The heat dissipation pad of the driver chip should be connected to a large area of thick copper layer to improve the heat dissipation performance of the driver chip. The heat dissipation pad is usually connected to the ground that is equal to the COM of the chip. It is recommended to connect the heat dissipation pad to the COM pin only.

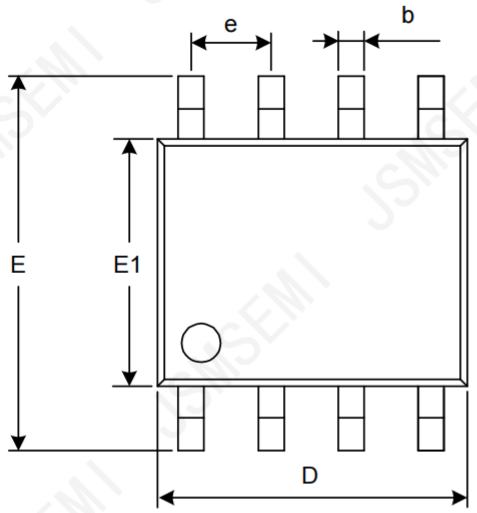
• Grounding precautions:

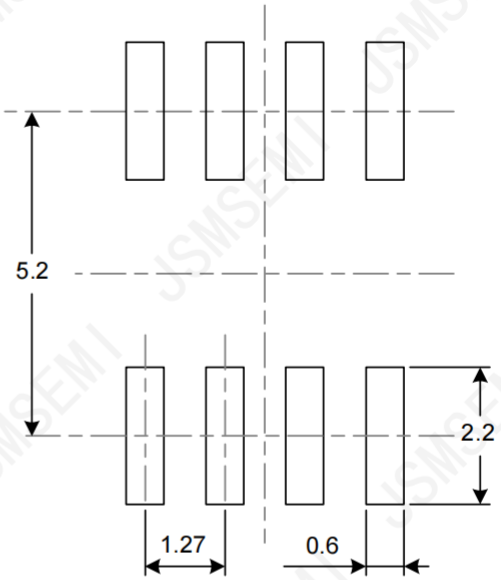
The primary goal of designing a ground connection is to limit the MOSFET gate charge and discharge loop to the smallest possible loop area. This method reduces the loop inductance and can effectively avoid the noise problem on the MOSFET gate. At the same time, the gate driver chip should be as close to the MOSFET as possible.

The second consideration is to ensure reasonable charging paths for bootstrap capacitors, including VCC bypass capacitors based on ground (COM), bootstrap diodes, bootstrap capacitors, and low-side MosFETs. Since the VCC bypass capacitor charges the bootstrap capacitor by cycle through the bootstrap diode, and each charge occurs in a very short period of time, this charge path passes through the peak current. Minimizing the loop length and area of the bootstrap circuit on PCB can make the bootstrap circuit work in a stable state, which is very important to ensure the reliable operation of the driver chip.

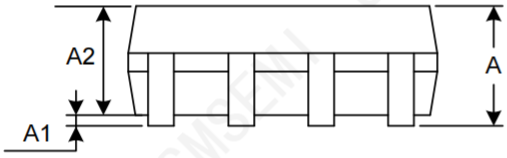
Package Information

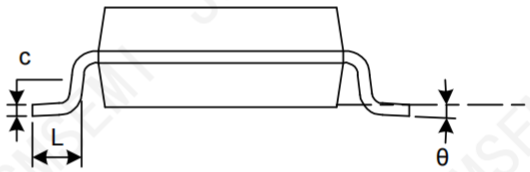
SOIC-8





RECOMMENDED LAND PATTERN (Unit: mm)





Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270 (BSC)		0.050 (BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Revision History

Rev.	Change	Date
V1.0	Initial version	6/27/2021

Important Notice

JSMSEMI Semiconductor (JSMSEMI) PRODUCTS ARE NEITHER DESIGNED NOR INTENDED FOR USE IN MILITARY AND/OR AEROSPACE, AUTOMOTIVE OR MEDICAL DEVICES OR SYSTEMS UNLESS THE SPECIFIC JSMSEMI PRODUCTS ARE SPECIFICALLY DESIGNATED BY JSMSEMI FOR SUCH USE. BUYERS ACKNOWLEDGE AND AGREE THAT ANY SUCH USE OF JSMSEMI PRODUCTS WHICH JSMSEMI HAS NOT DESIGNATED FOR USE IN MILITARY AND/OR AEROSPACE, AUTOMOTIVE OR MEDICAL DEVICES OR SYSTEMS IS SOLELY AT THE BUYER’S RISK.

JSMSEMI assumes no liability for application assistance or customer product design. Customers are responsible for their products and applications using JSMSEMI products.

Resale of JSMSEMI products or services with statements diferent from or beyond the parameters stated by JSMSEMI for that product or service voids all express and any implied warranties for the associated JSMSEMI product or s ervice. JSMSEMI is not responsible or liable for any such statements.

Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc.When designing equipment, refer to the "Delivery Specification" for the JSMSEMI product that you intend to use.

For additional information please contact Kevin@jsmsemi.com or visit www.jsmsemi.com