MP8870

18V, 15A, Synchronous Step-Down Converter with Configurable System Settings via I²C and MTP

DESCRIPTION

The MP8870 is a fully integrated, high-frequency, synchronous buck converter with an I²C control interface. It offers a very compact solution that achieves up to 15A of output current (I_{OUT}) with excellent load and line regulation across a wide input supply range. The MP8870 operates at high efficiency across a wide I_{OUT} load range.

The output voltage (V_{OUT}) can be controlled on-the-fly via the I²C serial interface. The reference voltage (V_{REF}) can be set between 0.3V and 1.536V, in 1.5mV steps. The voltage transition slew rate, frequency, current limit, hiccup mode and latch-off protection, enable, and power-saving mode can also be selected via the I²C interface.

The MP8870 adopts an internally compensated constant-on-time (COT) control mode that provides fast transient response and eases loop stabilization.

An open-drain power good (PG) signal indicates whether the output is within its nominal voltage range. PG is clamped at around 0.7V with an external pull-up voltage when the input supply fails to power the MP8870.

Full protection features include over-current protection (OCP), over-voltage protection (OVP), under-voltage protection (UVP), and over-temperature protection (OTP).

The MP8870 requires a minimal number of readily available, standard external components and is available in a QFN-21 (3mmx4mm) package.

FEATURES

- Wide 3V to 18V Input Voltage (V_{IN}) Range
- 15A Continuous/20A Peak Output Current (I_{OUT})
- 8mΩ/2.5mΩ Low-$R_{DS(ON)}$ Internal Power MOSFETs
- Two-Time Multiple-Time Programmable (MTP) Memory (1)
- PMBus Compliant
- Differential Output Voltage (V_{OUT}) Remote Sense
- 60μA Low Quiescent Current
- Adaptive Constant-On-Time (COT) Control for Ultra-Fast Transient Response
- Stable with Zero-ESR Output Capacitor (C_{OUT})
- I²C-Configurable Reference Voltage (V_{REF}) from 0.3V to 1.536V (in 1.5mV Steps) with Slew Rate Control
- Selectable Pulse-Frequency Modulation (PFM) or Pulse-Width Modulation (PWM) Mode, Adjustable Frequency, and Current Limit via the I²C Interface
- 7 Different Selectable I²C Addresses
- Configurable Soft Start
- V_{OUT} Tracking
- Open-Drain Power Good/PMBus Alert Selectable via the I²C
- PG Active Clamped at Low Level during Power Failure
- Pre-Biased Start-Up
- Over-Current Protection (OCP), Under-Voltage Protection (UVP), Under-Voltage Lockout (UVLO), Thermal Shutdown, and Over-Voltage Protection (OVP)
- Available in a QFN-21 (3mmx4mm) Package

MPL Optimized Performance with MPS Inductor MPL-AY Series

Note:

1) The two-time programmable multi-time programmable (MTP) memory is only for the standard version of the MP8870 (MP8870GL-0000).

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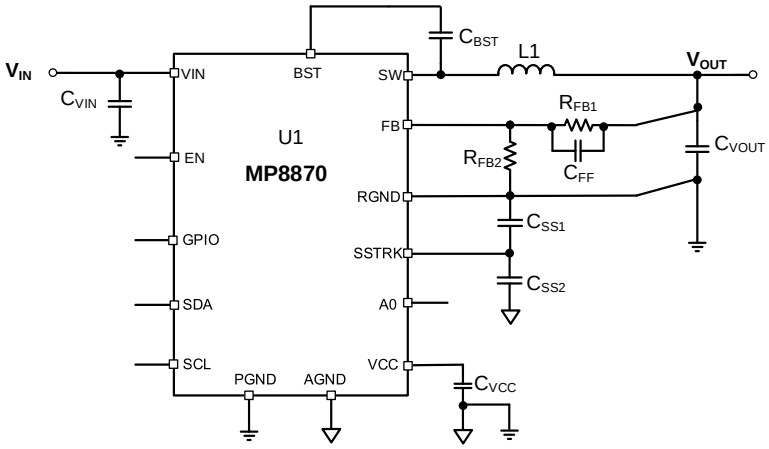
APPLICATIONS

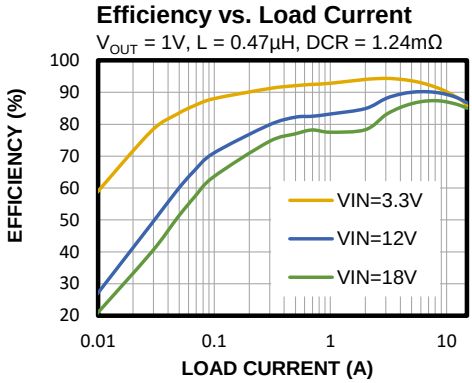
- Solid-State Drives (SSDs)
- System-On-Chip (SoC), FPGA, and DSP Cores
- Networking/Servers
- Flat-Panel Televisions and Monitors
- Industry Machines

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TYPICAL APPLICATION





MTP E-FUSE SELECTED TABLE BY DEFAULT (MP8870GL-0001)

One-Time Programmable Items	Configuration Value
Reference Voltage	0.40V
Output Voltage Set Mode	External voltage divider mode
Initial On/Off	On
MODE	Auto PFM/PWM mode
Valley Current Limit	16A
Soft-Start Time (0% to 100% V_{OUT})	1ms
Soft Stop when EN is Off	Disabled
Switching Frequency	650kHz
GPIO	PG
PG Delay Time	100µs
Protection Mode (OCP, OTP, and UVP)	Hiccup
V_{IN} OV Fault Response	Hiccup
Output OV Fault Response	Output discharge
MTP Configuration Code	0x01
MTP Revision Number	0x00

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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP8870GL-xxxx**	QFN-21(3mmx4mm)	*See Below*	1
MP8870GL-0001			
EVKT-MP8870	Evaluation kit	-	

* For Tape & Reel, add suffix -Z (e.g. MP8870GL-xxxx-Z).

** "-xxxx" is the configuration code identifier for the register setting stored in the MTP. Each "x" can be a hexadecimal value between 0 and F. For customized configurations, contact an MPS FAE to assign a 4-digit suffix code, even if ordering the "-0001" code. The MP8870GL-0001 is the default version, which can be programmed one time. The MP8870GL-0000 is the standard version, and it is only available for sampling. The MP8870GL-0000 can be programmed two times.

TOP MARKING

MPYW
8870
LLL

MP: MPS prefix
Y: Year code
W: Week code
8870: Part number
LLL: Lot number

EVALUATION KIT EVKT-MP8870

EVKT-MP8870 kit contents (items below can be ordered separately): (2)

#	Part Number	Item	Quantity
1	EVL8870-L-00A	MP8870GL evaluation board	1
2	EVKT-USBI2C-02	Includes one USB to I²C communication interface device, one USB cable, and one ribbon cable	1
3	MP8870GL-0001	The MP8870GL-0001 with its default configuration (can be used for the one-time programmable memory)	2
4	Online resources	Include GUI and supplemental resources	-

Order directly from MonolithicPower.com or our distributors.



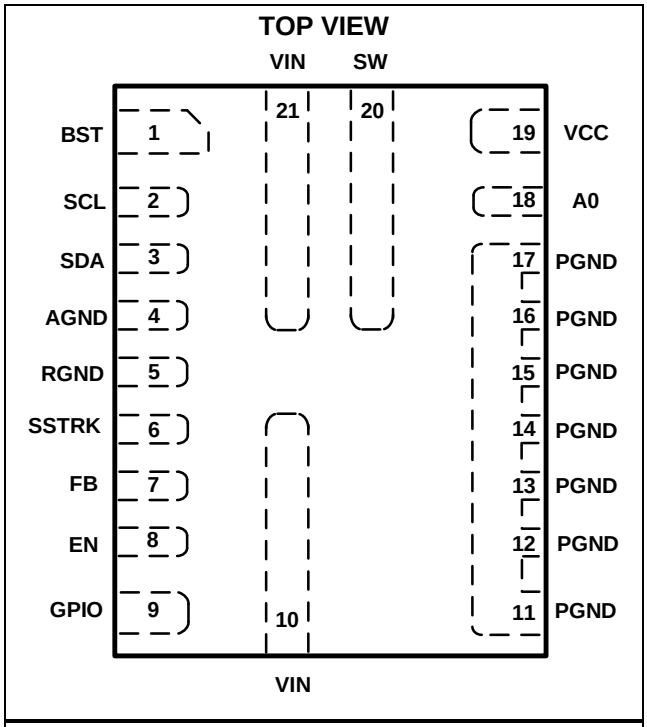
Figure 1: Evaluation Kit Set-Up

Note:

2) The two-time programmable multi-time programmable (MTP) memory is only for the standard version of the MP8870 (MP8870GL-0000).

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PACKAGE REFERENCE



QFN-21 (3mmx4mm)

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PIN FUNCTIONS

Pin #	Name		Description
1	BST		**Bootstrap.** Connect a capacitor between the SW and BST pins to form a floating supply across the high-side switch driver.
2	SCL		**I²C bus/PMBus clock.**
3	SDA		**I²C bus/PMBus data.**
4	AGND		**Analog ground.** Select the AGND pin as the control circuit reference point.
5	RGND		**Differential remote sense negative input.** Connect the RGND pin to the load's GND sense point. If the remote sense function is not used, short RGND to AGND.
6	SSTRK		**External tracking voltage input.** The output voltage (V_{OUT}) tracks this input signal. In addition, the soft-start (SS) time can be set by connecting an SS capacitor to the SSTRK pin. The total capacitance of the SS capacitors (C_{SS1}, connected from the SSTRK pin to RGND; and C_{SS2}, connected from the SSTRK pin to AGND) determines the soft-start time. See Equation (2) on page 21 for additional details. A minimum of 1nF is required for both SS capacitors (C_{SS1} and C_{SS2}). Place the SS capacitors as close to the SSTRK pin as possible. X7R or X5R grade dielectric ceramic capacitors are recommended for their stable temperature characteristics. See the Soft Start section on page 21 for more details.
7	FB		**Feedback (differential remote sense positive input).** An external resistor divider connected from the output to RGND, and tapped to the FB pin, sets V_{OUT}. It is recommended to place the resistor dividers as close to FB as possible. Avoid placing vias on the FB traces.
8	EN		**Enable.** The EN pin is an input signal that turns the regulator on or off. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. For automatic start-up, connect EN to VIN through a pull-up resistor or a resistive voltage divider.
9	GPIO	PG	**Power good.** When the MTP/I²C sets this pin to act as PG, this pin is the power good output. The output of PG is an open-drain signal. To indicate under-voltage (UV) and over-voltage (OV) conditions, connect PG to a DC voltage with a pull-up resistor. There is a PG delay time from low to high, which can be set via D7h, bits[4:2]. PG must be pulled high to ensure proper operation.
		PMBUS_ ALERT	**PMBus alert.** When the MTP/I²C configures this pin as PMBUS_ALERT, this pin reports an alert to the host if any alert items are detected. PMBUS_ALERT is an open-drain output. A high output indicates that there are no alert items, while a low output indicates that there is an alert item. PMBUS_ALERT must be pulled high to ensure proper operation.
10, 21	VIN		**Input voltage.** The VIN pin supplies power for the internal MOSFET and regulator. Input capacitors are required to decouple the input rail. Use wide PCB traces to make the VIN connection.
11, 12, 13, 1,4 15, 16, 17	PGND		**System ground.** The PGND pin is the reference ground of the regulated V_{OUT}, and it requires careful consideration during PCB layout. Use wide PCB traces to make the PGND connection.
18	A0		**I²C address set-up.** Connect a resistor from the A0 pin to AGND to set the device's address . When A0 is floating, the address is set to 46h.
19	VCC		**Internal 3.5V LDO output.** The driver and control circuits are powered from the VCC voltage. Decouple VCC with a minimum 1µF ceramic capacitor placed as close to this pin as possible. X7R or X5R grade dielectric ceramic capacitors are recommended due to their stable temperature characteristics. During MTP configurations, VCC may have a voltage of 5V for about 400ms.
20	SW		**Switch output.** Use a wide PCB trace for the SW pin connection.

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ABSOLUTE MAXIMUM RATINGS (3)

Supply voltage (V_{IN}), V_{EN} 20V
V_{IN} - V_{SW}.....-0.3V (-5V for <10ns) to +20.3V (+25V for <10ns)
V_{SW}.....-0.3V (-5V for <10ns) to V_{IN} + 0.3V (+25V for <10ns)
V_{BST}.....V_{SW} + 4V
V_{CC} 5V
V_{RGND}.....-0.3V to +0.3V
All other pins.....-0.3V to +4V
Junction temperature.....150°C
Lead temperature.....260°C
Storage temperature..... -65°C to +150°C

ESD Ratings

Human body model (HBM) ..... ±2000V
Charged device model (CDM) ..... ±750V

Recommended Operating Conditions (4)

Supply voltage (V_{IN})..... .....3V to 18V
Output voltage (V_{OUT}).....0.3V to 12V
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance (5) θ_{JA} θ_{JB} θ_{JC_TOP}

QFN-21(3mmx4mm)
EVL8870-L-00A (6).....26.....8.....4.....°C/W
JESD51-7 (7).....44....3.8....39....°C/W

Notes:

3) Exceeding these ratings may damage the device.
4) The device is not guaranteed to function outside of its operating conditions.
5) θ_{JB} is the thermal resistance from the junction to the board around the PGND soldering point.
θ_{JC_TOP} is the thermal resistance from the junction to the top of the package.
6) Measured on EVL8870-L-00A, 4-layer 85mmx85mm PCB.
7) The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C (8), typical values are tested at T_J = 25°C, unless otherwise noted. The over-temperature limit is derived by characterization, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
Supply current (shutdown)	I_{SD}	V_{EN} = 0V		0	5	μA
Supply current (quiescent)	I_Q	V_{EN} = 2V, V_{FB} = 0.42V		60	100	μA
MOSFET						
High-side (HS) switch on resistance	HS_{RDS-ON}	V_{BST-SW} = 3.5V		8		mΩ
Low-side (LS) switch on resistance	LS_{RDS-ON}	V_{CC} = 3.5V		2.5		mΩ
Switch leakage	SW_{LKG_HS}	V_{EN} = 0V, V_{SW} = 0V, T_J = 25°C			1	μA
	SW_{LKG_LS}	V_{EN} = 0V, V_{SW} = 12V, T_J = 25°C			10	
Current Limit and Zero-Current Detection (ZCD)						
Peak current limit	I_{LIMIT_PK}	Adjustable via the I²C or MTP	18	20	25	A
Valley current limit	I_{LIMIT_VALLEY}	Adjustable via the I²C or MTP	14	16	18	A
ZCD	I_{ZCD}	PFM mode		50		mA
LS negative current limit	I_{LIM_NEG}	Forced continuous conduction mode (FCCM), adjustable via the I²C or MTP		-8		A
Switching Frequency and Minimum On/Off Time						
Switching frequency	f_{SW}	V_{OUT} = 1V, I_{OUT} = 0A, FCCM, adjustable via the I²C or MTP	550	650	750	kHz
Minimum on time (9)	t_{ON_MIN}			30		ns
Minimum off time (9)	t_{OFF_MIN}			80		ns
Over-Voltage Protection (OVP) and Under-Voltage Protection (UVP)						
OVP threshold	V_{OVP}		112%	120%	128%	V_{REF}
UVP_1 threshold	V_{UVP1}		62%	70%	78%	V_{REF}
UVP_2 threshold	V_{UVP2}		42%	50%	58%	V_{REF}
Feedback Voltage						
Feedback voltage	V_{FB}	T_J = 25°C, adjustable via the I²C or MTP	396	400	404	mV
		T_J = -40 to +125°C, adjustable via the I²C or MTP	394	400	406	mV
SSTRK						
SSTRK sourcing current	I_{TRACK_SOURCE}	V_{SSTRK} = 0V	3	4	5	μA
SSTRK sinking current	I_{TRACK_SINK}	V_{SSTRK} = 1V	0.7	1	1.3	μA
Soft-start time	t_{SS}	T_J = 25°C, adjustable via the MTP and SS capacitor		1		ms
Error Amplifier (EA)						
Feedback current	I_{FB}	V_{FB} = V_{REF}		50	100	nA

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C [8], typical values are tested at T_J = 25°C, unless otherwise noted. The over-temperature limit is derived by characterization, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
I²C Address Threshold						
A0 voltage threshold 1	V_{ADD_1}	Set the I²C address to 40h	0		0.15	V
A0 voltage threshold 2	V_{ADD_2}	Set the I²C address to 41h	0.25		0.35	V
A0 voltage threshold 3	V_{ADD_3}	Set the I²C address to 42h	0.42		0.52	V
A0 voltage threshold 4	V_{ADD_4}	Set the I²C address to 43h	0.62		0.72	V
A0 voltage threshold 5	V_{ADD_5}	Set the I²C address to 44h	0.82		0.92	V
A0 voltage threshold 6	V_{ADD_6}	Set the I²C address to 45h	1.02		1.12	V
A0 voltage threshold 7	V_{ADD_7}	Set the I²C address to 46h	1.3		V_{CC}	V
A0 sourcing current	I_{A0}	V_{A0} = 0V		10		µA
Enable and UVLO						
Enable input rising threshold	$V_{EN-RISING}$		1.14	1.2	1.26	V
Enable hysteresis	V_{EN-HYS}			120		mV
EN pin pull-down resistor	R_{EN_PD}			1.5		MΩ
Input Voltage (V_{IN}) Under-Voltage Lockout (UVLO)						
V_{IN} range			3		18	V
V_{IN} UVLO rising threshold	VIN_{VTH_RISE}		2.6	2.7	2.97	V
V_{IN} UVLO hysteresis	VIN_{VTH_HYS}			300		mV
VCC Regulator						
VCC regulator	V_{CC}		3.4	3.5	3.6	V
VCC load regulation		I_{CC} = 25mA		1		%
Power Good						
Power good UV rising threshold	$PGUV_{VTH_HI}$		0.82	0.9	0.98	V_{REF}
Power good UV falling threshold	$PGUV_{VTH_LO}$		0.72	0.8	0.88	V_{REF}
Power good OV rising threshold	$PGOV_{VTH_HI}$		1.12	1.2	1.28	V_{REF}
Power good OV falling threshold	$PGOV_{VTH_LO}$		1.02	1.1	1.18	V_{REF}
Power good delay	PG_{TD}	Adjustable via the I²C or MTP		100		µs
Power good sink current capability	V_{PG}	Sink = 4mA			0.4	V
Power good leakage current	I_{PG_LKG}	V_{PG} = 4V			10	µA
Thermal shutdown [9]	T_{SD}			150		°C
Thermal shutdown hysteresis [9]	T_{SD_HYS}			20		°C

Notes:

8) Not tested in production. Derived by over-temperature correlation.
9) Derived by sample characterization. Not tested in production.

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I/O LEVEL CHARACTERISTICS

Parameter	Symbol	Condition	HS Mode		LS Mode		Units
			Min	Max	Min	Max	
Low-level input voltage	V_{IL}		-0.5	+0.3 x V_{CC}	-0.5	+0.3 x V_{CC}	V
High-level input voltage	V_{IH}		0.7 x V_{CC}	V_{CC} + 0.5	0.7 x V_{CC}	V_{CC} + 0.5	V
Hysteresis of Schmitt trigger inputs	V_{HYS}	V_{CC} > 2V	0.05 x V_{CC}		0.05 x V_{CC}		V
		V_{CC} < 2V	0.1 x V_{CC}		0.1 x V_{CC}		
Low-level output voltage (open drain) at 3mA sink current	V_{OL}	V_{CC} > 2V	0	0.4	0	0.4	V
		V_{CC} < 2V	0	0.2 x V_{CC}	0	0.2 x V_{CC}	
Low-level output current	I_{OL}			3		3	mA
Transfer gate on resistance for currents between SDA and SCAH, or SCL and SCLH	R_{ONL}	V_{OL} level, I_{OL} = 3mA		50		50	Ω
Transfer gate on resistance between SDA and SCAH, or SCL and SCLH	R_{ONH}	Both signals (SDA and SDAH, or SCL and SCLH) at V_{CC} level	50		50		kΩ
Pull-up current of the SCLH current source	I_{CS}	SCLH output levels between 30% and 70% of V_{CC}	2	6	2	6	mA
Rising time of the SCLH or SCL signal	t_{RCL}	Output rising time (current source enabled) with an external pull-up current source of 3mA					
		Capacitive load from 10pF to 100pF	10	40			ns
		Capacitive load of 400pF	20	80			ns
Falling time of the SCLH or SCL signal	t_{FCL}	Output falling time (current source enabled) with an external pull-up current source of 3mA					
		Capacitive load from 10pF to 100pF	10	40			ns
		Capacitive load of 400pF	20	80	20	250	ns
Rising time of SDAH signal	t_{RDA}	Capacitive load from 10pF to 100pF	10	80			ns
		Capacitive load of 400pF	20	160	20	250	ns
Falling time of SDAH signal	t_{FDA}	Capacitive load from 10pF to 100pF	10	80			ns
		Capacitive load of 400pF	20	160	20	250	ns

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I/O LEVEL CHARACTERISTICS *(continued)*

Parameter	Symbol	Condition	HS Mode		LS Mode		Units
			Min	Max	Min	Max	
Pulse width of spikes that must be suppressed by the input filter	t_{SP}		0	10	0	50	ns
Input current of each I/O pin	I_I	Input voltage between 10% and 90% of V_{CC}		+10	-10	+10	µA
Capacitance of each I/O pin	C_I			10		10	pF

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I²C PORT SIGNAL CHARACTERISTICS (10)

Parameter	Symbol	Condition	C_B = 100pF		C_B = 400pF		Units
			Min	Max	Min	Max	
SCLH and SCL clock frequency	f_{SCHL}		0	3.4	0	0.4	MHz
Set-up time for a repeated start command	t_{SU_STA}		160		600		ns
Hold time (repeated) start command	t_{HD_STA}		160		600		ns
Low period of the SCL clock	t_{LOW}		160		1300		ns
High period of the SCL clock	t_{HIGH}		60		600		ns
Data set-up time	t_{SU_DAT}		10		100		ns
Data hold time	t_{HD_DAT}		0	70	0		ns
Rising time of SCLH signal	t_{RCL}		10	40	20 x 0.1 x C_B	300	ns
Rising time of SCLH signal after a repeated start command and after an acknowledge bit	t_{FCL1}		10	80	20 x 0.1 x C_B	300	ns
Falling time of SCLH signal	t_{FCL}		10	40	20 x 0.1 x C_B	300	ns
Rising time of SDAH signal	t_{FDA}		10l	80	20 x 0.1 x C_B	300	ns
Falling time of SDAH signal	t_{FDA}		10	80	20 x 0.1 x C_B	300	ns
Set-up time for stop condition	t_{SU_STO}		160		600		ns
Bus free time between a stop and start command	t_{BUF}		160		1300		ns
Data valid time	t_{VD_DAT}			16		90	ns
Data valid acknowledge time	t_{VD_ACK}			160		900	ns
Capacitive load for each bus line	C_B	SDAH and SCLH line		100		400	pF
		SDAH and SDA line, and SCLH and SCL line		400		400	pF
Noise margin at the low level	C_I	For each connected device		0.1 x V_{CC}	0.1 x V_{CC}		V
Noise margin at the high level	V_{NH}	For each connected device		0.2 x V_{CC}	0.2 x V_{CC}		V

Note:

10) V_{CC} is the I²C bus voltage, with a range between 1.8V and 3.6V range. It is used for the 1.8V, 2.5V, and 3.3V bus voltages.

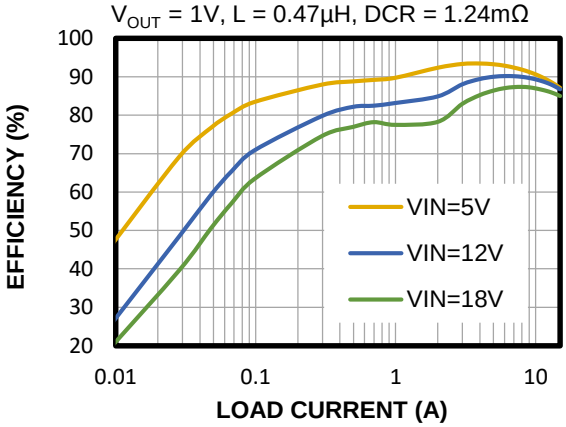
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TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 1V, L = 0.47µH, f_{SW} = 650kHz, T_A = 25°C, unless otherwise noted.

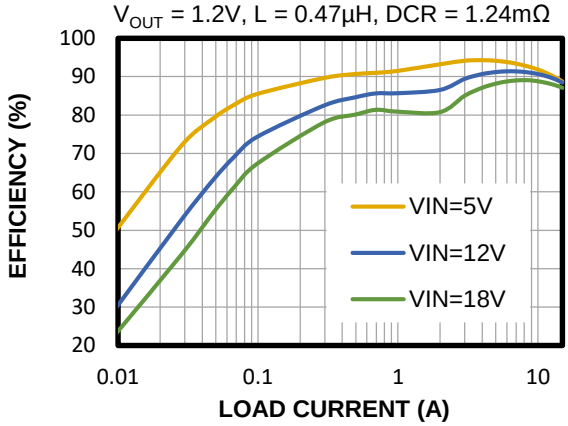
Efficiency vs. Load Current

V_{OUT} = 1V, L = 0.47µH, DCR = 1.24mΩ



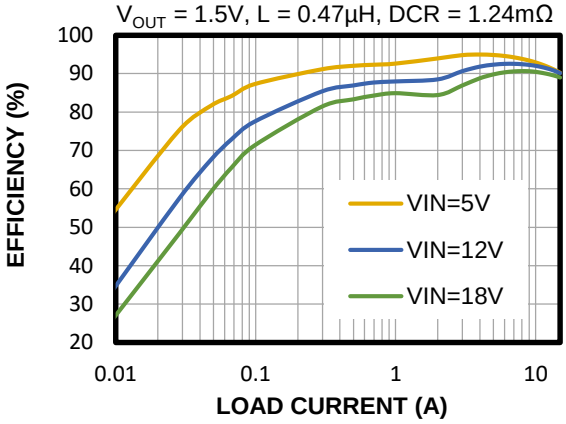
Efficiency vs. Load Current

V_{OUT} = 1.2V, L = 0.47µH, DCR = 1.24mΩ



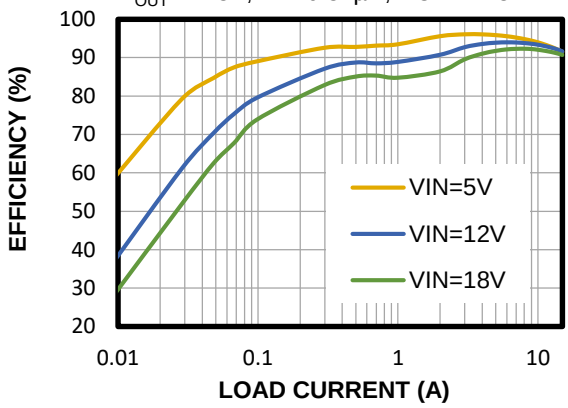
Efficiency vs. Load Current

V_{OUT} = 1.5V, L = 0.47µH, DCR = 1.24mΩ



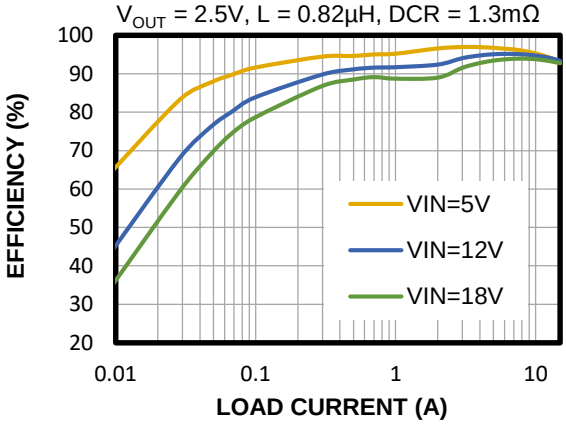
Efficiency vs. Load Current

V_{OUT} = 1.8V, L = 0.82µH, DCR = 1.3mΩ



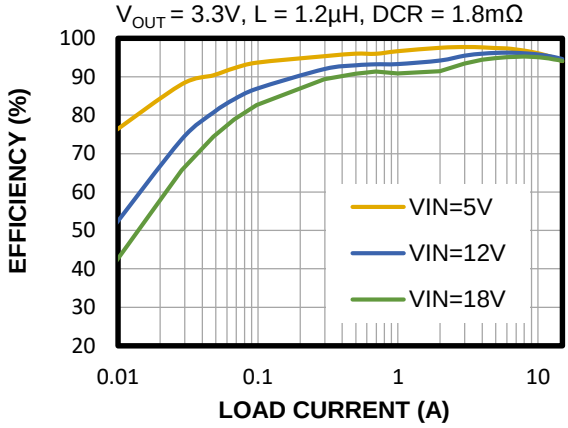
Efficiency vs. Load Current

V_{OUT} = 2.5V, L = 0.82µH, DCR = 1.3mΩ



Efficiency vs. Load Current

V_{OUT} = 3.3V, L = 1.2µH, DCR = 1.8mΩ



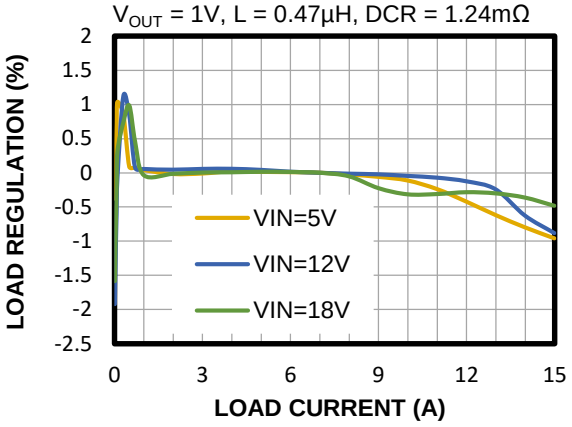
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1V, L = 0.47µH, f_{SW} = 650kHz, T_A = 25°C, unless otherwise noted.

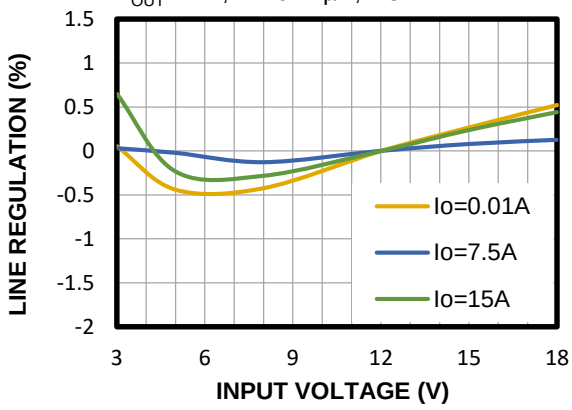
Load Regulation vs. Load Current

V_{OUT} = 1V, L = 0.47µH, DCR = 1.24mΩ



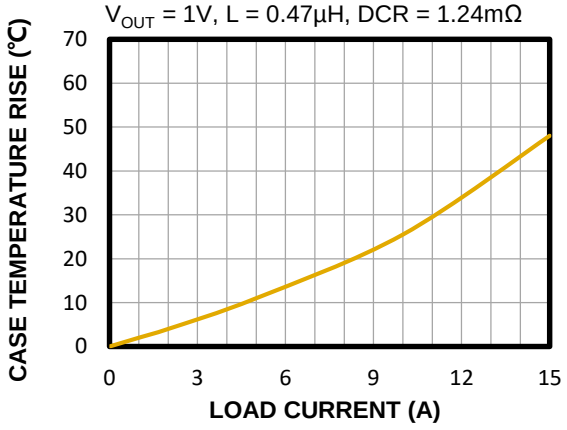
Line Regulation vs. V_{IN}

V_{OUT} = 1V, L = 0.47µH, DCR = 1.24mΩ

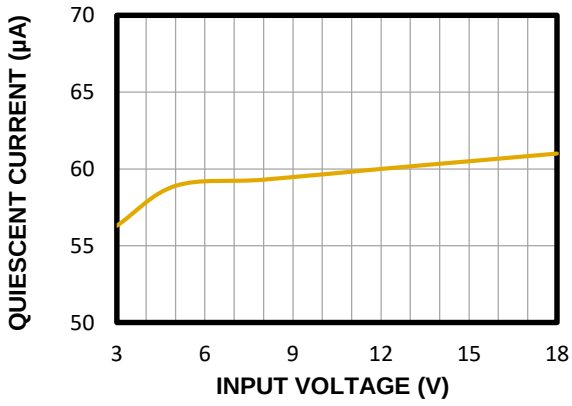


Case Temperature Rise vs. Load Current

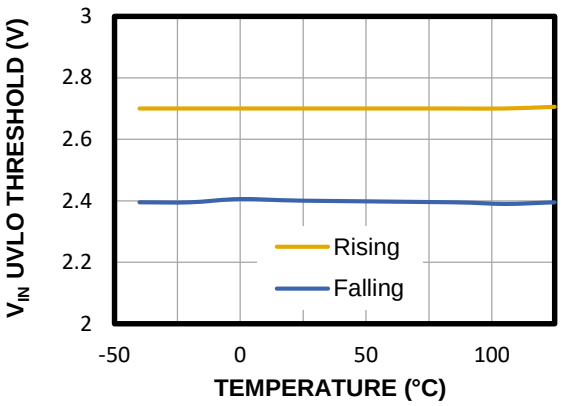
V_{OUT} = 1V, L = 0.47µH, DCR = 1.24mΩ



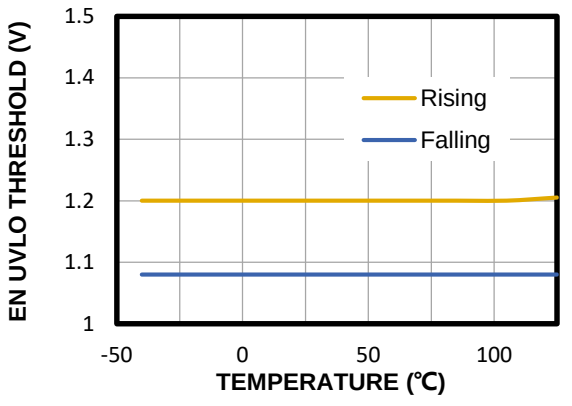
Quiescent Current vs. Input Voltage



V_{IN} UVLO Threshold vs. Temperature



EN UVLO Threshold vs. Temperature

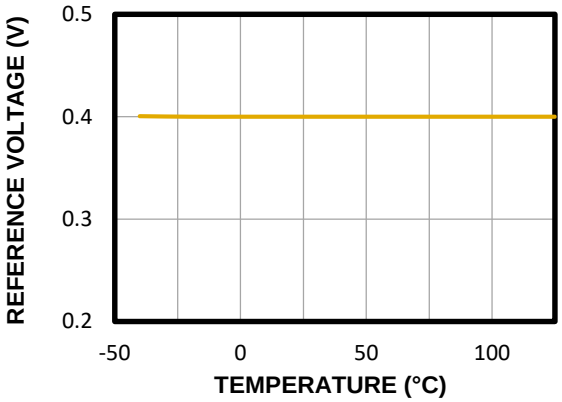


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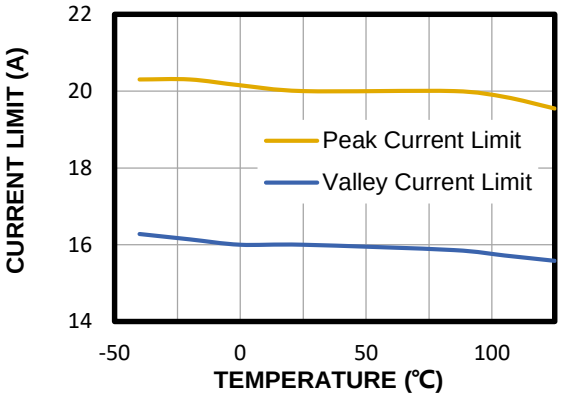
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1V, L = 0.47µH, f_{SW} = 650kHz, T_A = 25°C, unless otherwise noted.

Reference Voltage vs. Temperature



Current Limit vs. Temperature



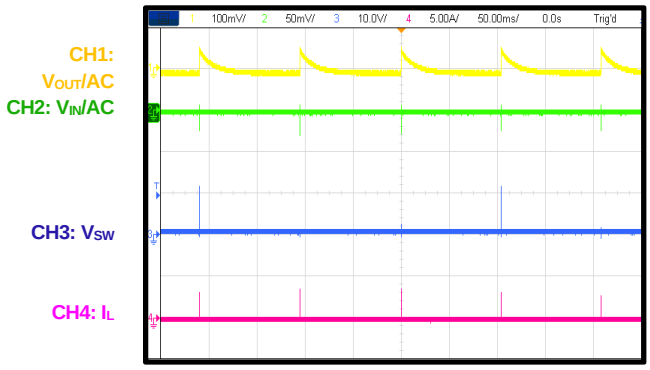
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TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 1V, L=0.47µH, f_{SW} = 650kHz, T_A = 25°C, unless otherwise noted.

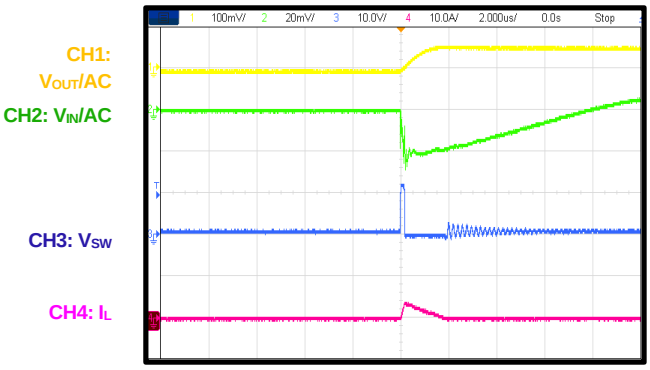
Input and Output Voltage Ripple

I_{OUT} = 0A



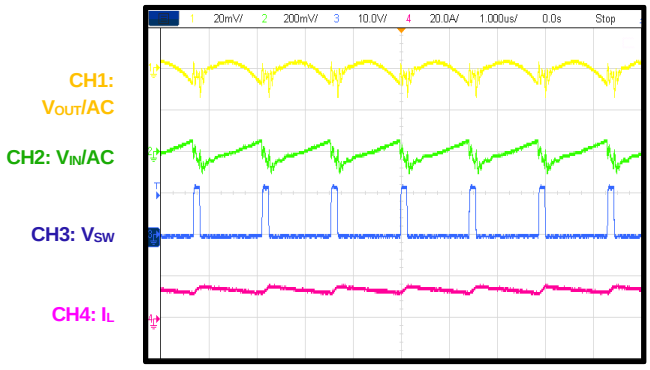
Input and Output Voltage Ripple

I_{OUT} = 0A



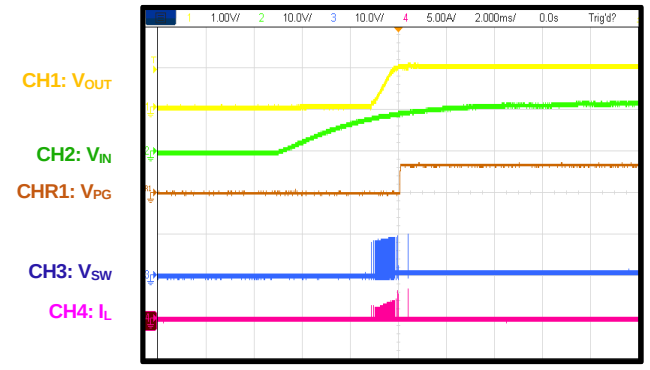
Input and Output Voltage Ripple

I_{OUT} = 15A



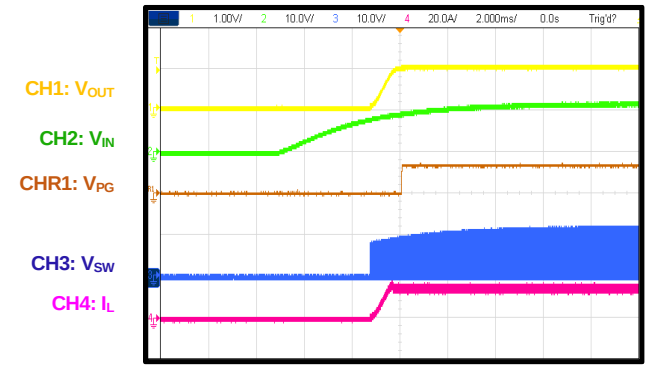
Start-Up through the Input Voltage

I_{OUT} = 0A



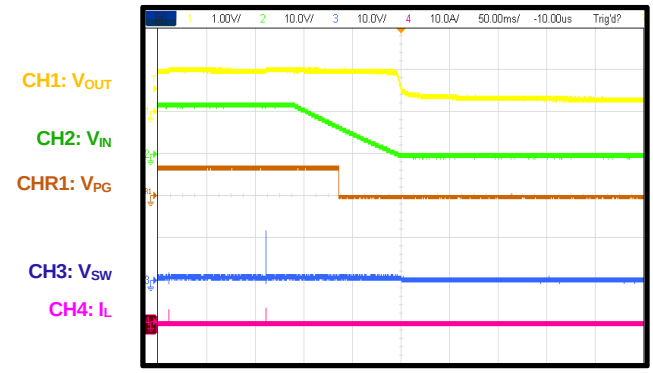
Start-Up through the Input Voltage

I_{OUT} = 15A



Shutdown through the Input Voltage

I_{OUT} = 0A



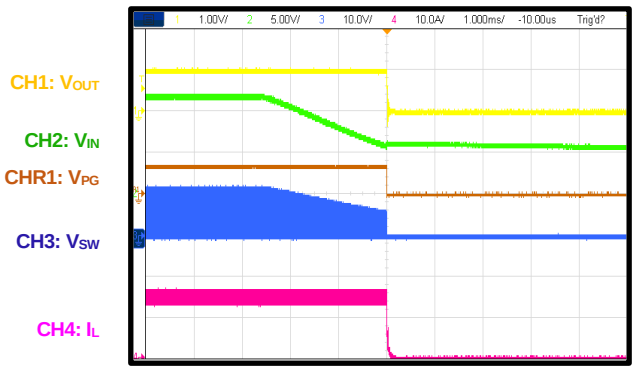
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1V, L = 0.47µH, f_{SW} = 650kHz, T_A = 25°C, unless otherwise noted.

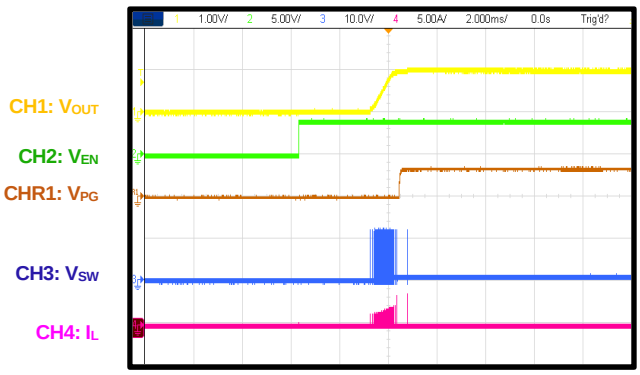
Shutdown through the Input Voltage

I_{OUT} = 15A



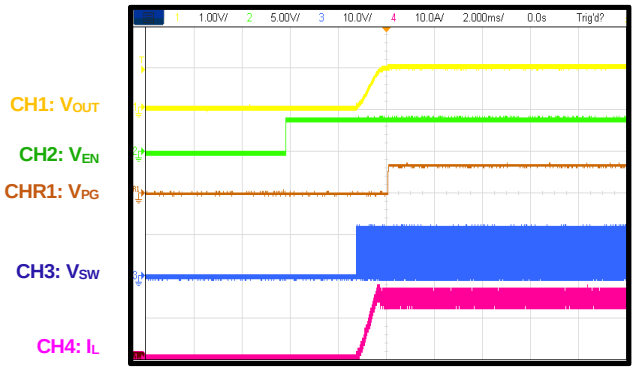
Start-up Through EN

I_{OUT} = 0A



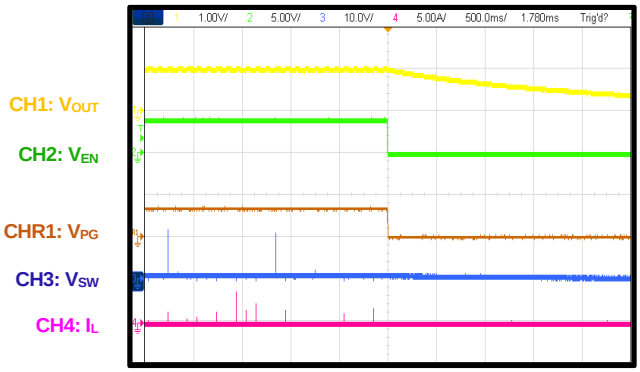
Start-Up through EN

I_{OUT} = 15A



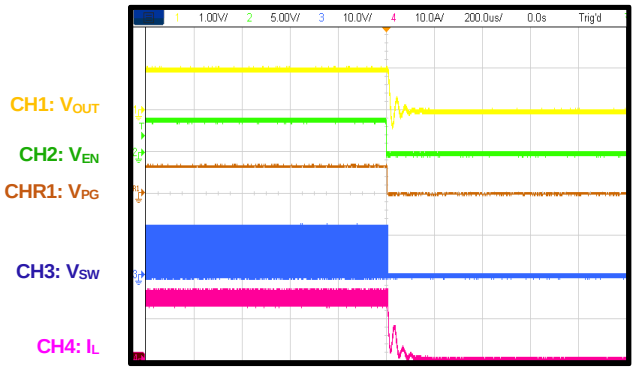
Shutdown through EN

I_{OUT} = 0A



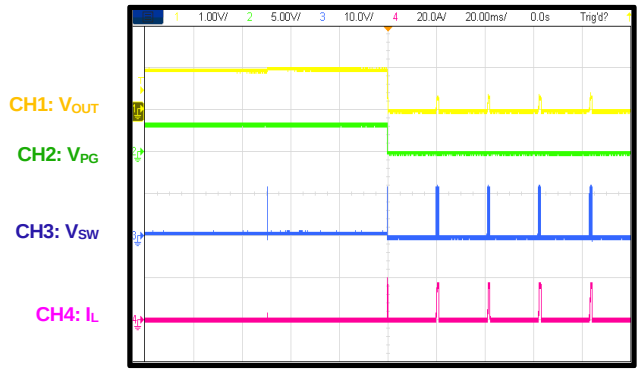
Shutdown through EN

I_{OUT} = 15A



Short-Circuit Protection Entry

I_{OUT} = 0A



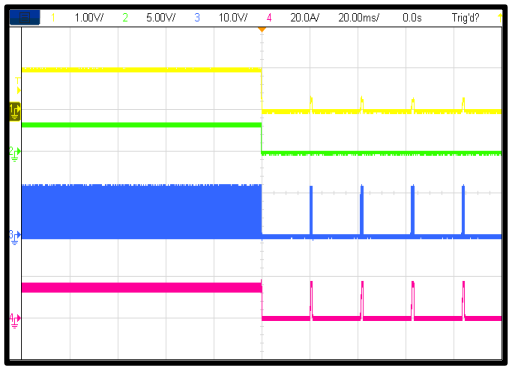
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

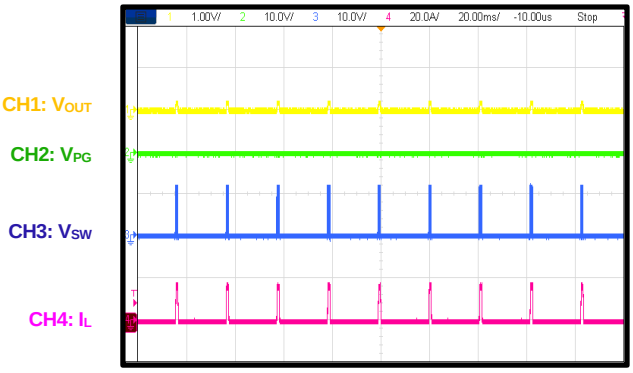
V_{IN} = 12V, V_{OUT} = 1V, L = 0.47µH, f_{SW} = 650kHz, T_A = 25°C, unless otherwise noted.

Short-Circuit Protection Entry

I_{OUT} = 15A

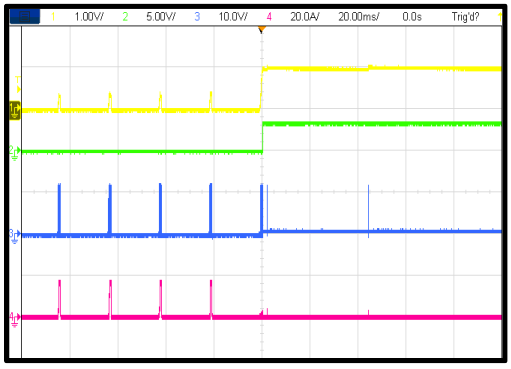


Short-Circuit Protection Steady State



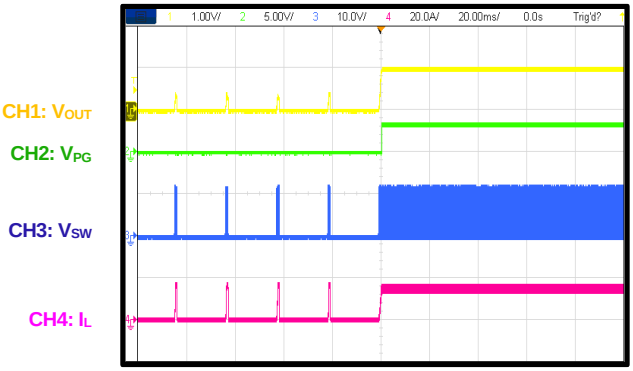
Short-Circuit Protection Recovery

I_{OUT} = 0A



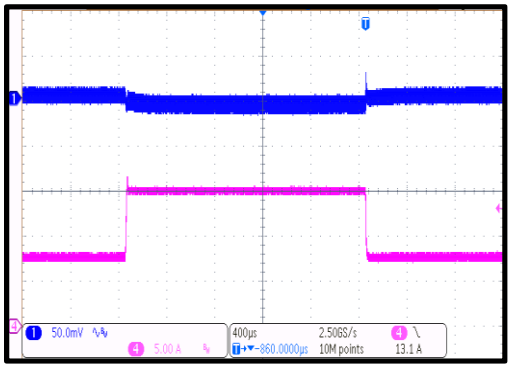
Short-Circuit Protection Recovery

I_{OUT} = 15A



Load Transient Response

7.5A to 15A, 2.5A/µs



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FUNCTIONAL BLOCK DIAGRAM

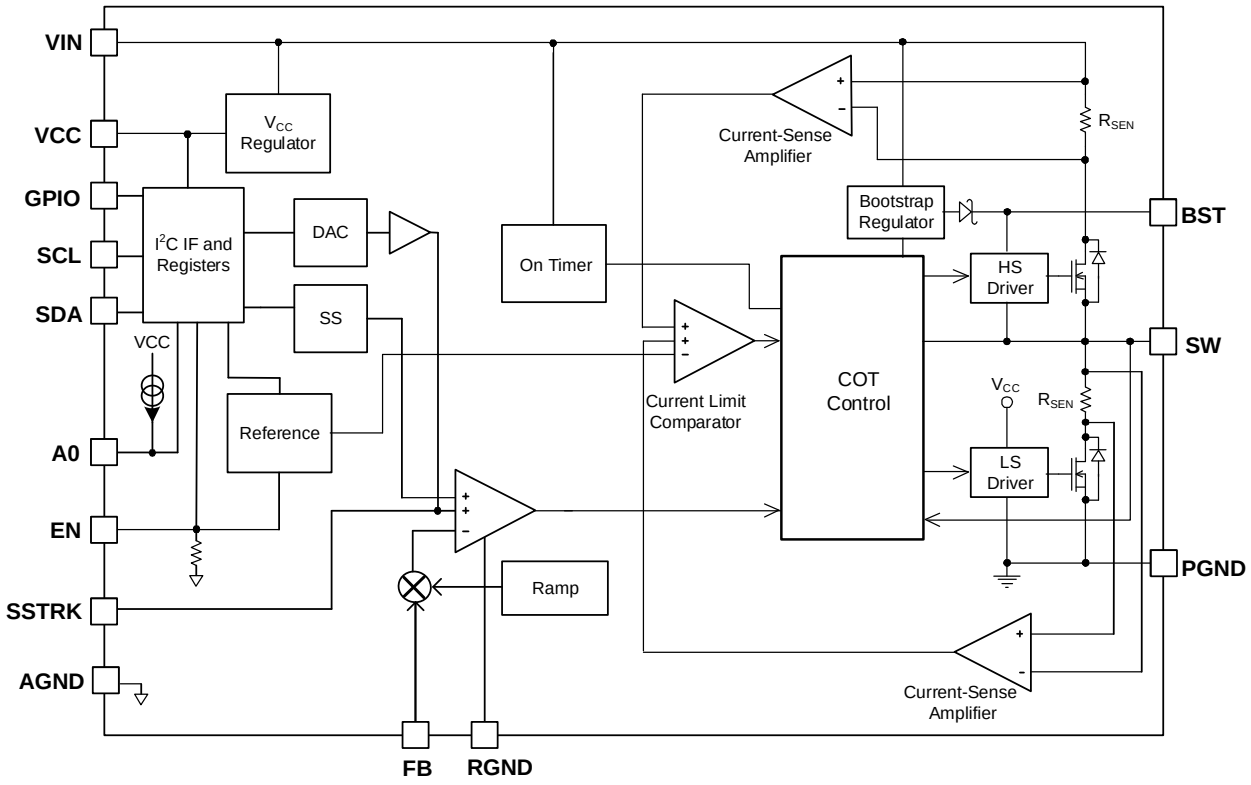


Figure 2: Functional Block Diagram

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OPERATION

Constant-On-Time (COT) Control

The MP8870 employs constant-on-time (COT) control to achieve a fast load transient response. Figure 3 shows the MP8870's detailed control stage.

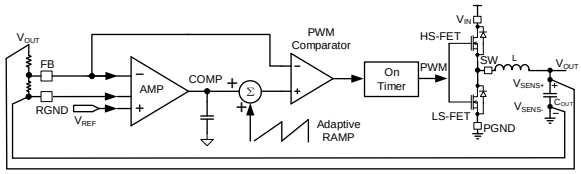


Figure 3: COT Control

The operational amplifier (AMP) corrects any error voltage between the FB pin and the reference voltage (V_{REF}). The MP8870 can use AMP to provide excellent load regulation across the entire load range in either pulse-frequency modulation (PFM) mode or pulse-width modulation (PWM) mode.

The dedicated RGND pin helps provide the differential output voltage remote sense feature. For the best performance, the pair of remote-sense traces should be kept in a low impedance.

The MP8870 has internal RAMP compensation to support a low-ESR MLCC output capacitor solution. The adaptive internal RAMP is optimized so that the MP8870 is stable across the entire operating input voltage (V_{IN}) and output voltage (V_{OUT}) ranges with a properly designed output LC filter.

Pulse-Width Modulation (PWM) Operation

Figure 4 shows how the pulse-width modulation (PWM) signal is generated. AMP corrects any error between the FB voltage (V_{FB}) and V_{REF}, and generates a fairly smooth DC voltage (COMP).

The internal RAMP is superimposed onto COMP, which is compared to the FB signal. If the FB signal drops below the superimposed COMP, the integrated high-side MOSFET (HS-FET) turns on. The HS-FET remains on for a fixed turn-on time. The fixed on time is determined by V_{IN}, V_{OUT}, and the selected switching frequency (f_{SW}). After the on period elapses, the HS-FET turns off. It turns on again when FB drops below the superimposed COMP. By repeating this operation, the MP8870 regulates V_{OUT}.

To minimize conduction loss, the integrated low-side MOSFET (LS-FET) turns on when the HS-FET is off. A dead short occurs between VIN and PGND if both the HS-FET and the LS-FET turn on at the same time. This is called a shoot-through. To avoid a shoot-through, a dead time (DT) is generated internally between the HS-FET off period and the LS-FET on period, and vice versa.

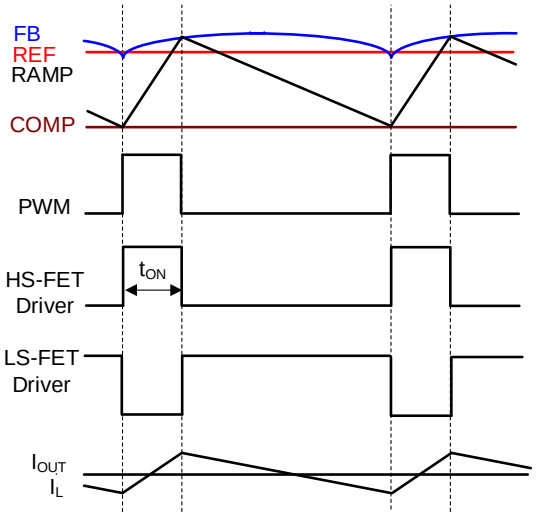


Figure 4: Heavy-Load Operation

Continuous Conduction Mode (CCM) Operation

Continuous conduction mode (CCM) occurs when the output current (I_{OUT}) is high, and the inductor current (I_L) is always above zero amps (see Figure 4). The MP8870 can also be configured to operate in forced continuous conduction mode (FCCM) when I_{OUT} is low (see the Mode Selection section on page 21 for more details).

During CCM, f_{SW} is fairly constant. This means that the output voltage ripple remains almost constant across the entire load range.

Pulse-Skip Operation

Under light-load conditions, the MP8870 can be configured to work in pulse-skip mode (also called PFM mode) to optimize efficiency. When the load decreases, I_L decreases as well. Once I_L reaches zero, the MP8870 transitions from CCM to pulse-skip mode, assuming that the MP8870 is configured to operate in this way.

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Figure 5 shows pulse-skip mode under light-load conditions. When FB drops below the superimposed COMP, the HS-FET turns on for a fixed interval. When the HS-FET turns off, the LS-FET turns on until I_L reaches zero. In pulse-skip mode, FB does not reach the superimposed COMP when I_L approaches zero. The LS-FET driver turns into tri-state (Hi-Z) when I_L reaches zero. Then the output capacitors discharge slowly to PGND through the LS-FET. Under light-load conditions, the HS-FET does not turn on as frequently in pulse-skip mode as it would in FCCM. As a result, the efficiency in pulse-skip mode is much higher than the efficiency in FCCM.

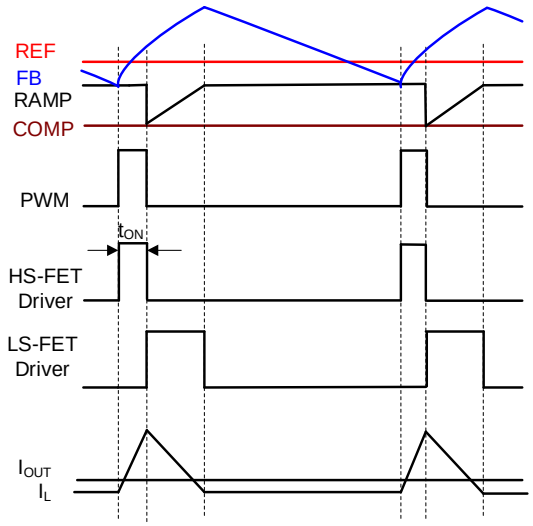


Figure 5: Pulse-Skip Mode under Light Loads

As I_{OUT} increases from light loads, the time period during which the current modulator regulates becomes shorter. The HS-FET turns on more frequently, and f_{SW} increases accordingly. I_{OUT} reaches a critical level when the current modulator time is zero. The critical level for I_{OUT} can be calculated with Equation (1):

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times f_{SW} \times V_{IN}} \quad (1)$$

Where f_{SW} is the switching frequency.

The MP8870 enters CCM once I_{OUT} exceeds its critical level. Afterward, f_{SW} remains fairly constant across the I_{OUT} range.

Mode Selection

The MP8870 provides both FCCM and pulse-skip operation under light-load conditions. The operation mode is selected via the I²C register MFR_VOUT_FREQUENCY_SWITCH (D4h). When D4h, bits[4:3] = 2b'00, the device operates in PFM mode. When D4h, bits[4:3] = 2b'01, the device operates in FCCM mode. these bits are set to 00 by default.

Soft Start

The MP8870 employs a soft start (SS) mechanism to ensure that there is a smooth output during start-up.

After the EN pin goes high, an internal current source starts to charge the SS capacitors. The SS voltage (V_{SS}) overrides V_{REF} to the PWM comparator, so that V_{OUT} smoothly ramps up as V_{SS} rises. Once V_{SS} reaches V_{REF}, V_{REF} takes over the PWM comparator. Then the soft-start period is considered complete, and the part enters steady state operation.

SS prevents the converter's V_{OUT} from overshooting during start-up.

The typical soft-start time (t_{SS}), set by the SS capacitors between the SSTRK and GND pins, can be estimated with Equation (2):

$$t_{ss}(ms) = \frac{V_{REF}(V) \times C_{ss}(nF)}{4\mu A} \quad (2)$$

Where V_{REF} is the reference voltage set by VOUT_COMMAND (21h) (it is set to 0.4V by default), and C_{SS} is the total capacitance between C_{SS1} and C_{SS2}. Both C_{SS1} and C_{SS2} are required to ensure that V_{REF} is stable during soft start. A minimum value of 1nF for C_{SS1} and C_{SS2} is required.

The minimum soft-start time is limited to 1ms internally. This value can be increased via TON_RISE (61h), or by increasing the SS capacitance between SSTRK and RGND.

To set a longer SS time using the capacitors, use Equation (2). To simplify the calculation and set-up, it is recommended to use a 4.7nF capacitor for C_{SS2}, then adjust the capacitance of C_{SS1} to obtain the target soft start time. For example, with a 4.7nF capacitor for C_{SS2}, and a 22nF capacitor for C_{SS1}, t_{SS} is 2.7ms.

Note that the real t_{SS} is the maximum value between the internal TON_RISE (61h) register and the external SS capacitors.

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Pre-Biased Start-Up

The MP8870 is designed for monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, the IC disables switching for both the HS-FET and LS-FET until the voltage on the SSTRK capacitor exceeds the sensed output voltage at FB. Before the SSTRK voltage reaches the pre-biased FB level, if the BST voltage (from BST to SW) is below 2.3V, the LS-FET turns on to allow the BST voltage to be charged through VCC. The LS-FET turns on for very narrow pulses, so the drop in the pre-biased level is negligible.

Current Sense and Over-Current Protection (OCP)

The MP8870 features a configurable positive current limit threshold. The threshold can be configured via the MFR_OC_FAULT_LIMIT (D5h) register.

The current-limit circuit employs both a high-side current limit and a low-side valley current-sensing algorithm. The MP8870 uses the $R_{DS(ON)}$ of the LS-FET as a current-sensing element for the valley current limit. If the high-side current-sense signal exceeds the current-limit threshold, the on timer's pulse is terminated, and the LS-FET turns on. Afterward, I_L is monitored by the voltage between GND and SW. GND is used as the positive current-sensing node, so GND should be connected to the source terminal of the bottom MOSFET. The HS-FET does not turn on before I_L falls to the valley threshold.

Over-current protection (OCP) hiccup mode is active after SS finishes. If OCP hiccup mode is active, there are two ways that OCP can be activated:

- The MP8870 detects an OC condition for 18 consecutive cycles and the FB voltage (V_{FB}) drops below 70% of V_{REF} (UVP1)
- The MP8870 detects an OC condition once, and V_{FB} drops below 50% of V_{REF} (UVP2)

If OCP is triggered, the MP8870 latches off the HS-FET immediately, and it latches off the LS-FET after zero-current detection (ZCD) is detected. Meanwhile, the SSTRK capacitor discharges. After about 20ms, the MP8870 attempts to soft start automatically. If the OC condition still remains when soft start finishes, the MP8870 repeats this operation cycle until the OC condition disappears. Then V_{OUT} smoothly rises back to its regulation level.

OCP can configured to latch off via MFR_FAULT_RESPONSE (D6h), bit[2].

Negative Inductor Current Limit

When the LS-FET detects a negative current below its limit, the part turns off the LS-FET and turns on the HS-FET for a certain period of time to limit the negative current.

Input Over-Voltage Protection (V_{IN} OVP)

The MP8870 monitors the VIN pin to detect an input over-voltage (OV) event. The MP8870's input OVP function can be enabled via MFR_FAULT_RESPONSE (D6h), bit[4]. When bit[4] = 1b'0, the V_{IN} OVP function is disabled. When bit[4] = 1b'1, the V_{IN} OVP function is enabled.

When the output is in an OVP discharge state, or EN turns off if soft stop is enabled, an output discharge can cause V_{IN} to be charged high. If V_{IN} OVP is triggered, neither the HS-FET nor LS-FET turn on to stop charging V_{IN}. Once V_{IN} drops below the V_{IN} OVP hysteresis threshold, the IC starts switching again.

Output Over-Voltage Protection (V_{OUT} OVP)

The MP8870 monitors the voltage on the FB pin. If V_{FB} exceeds 120% of V_{REF}, OVP is triggered. The output OVP response can be configured via MFR_FAULT_RESPONSE, bits[1:0]. When OVP is triggered, the MP8870 can be set to respond with latch-off mode, output discharge, or no action. The response is set to output discharge by default.

If the MP8870 is set to PFM mode when V_{OUT} OVP is triggered, and the response is set to output discharge, the LS-FET turns on for about 200ns, and then it turns off for about 2.5us. The LS-FET repeats this cycle until V_{OUT} drops below the OVP falling threshold. This discharges the output and tries to keep it within the normal range. If the response is set to no action, the MP8870 stops switching once OVP is triggered.

If the MP8870 is set to FCCM when V_{OUT} OVP occurs, and the response is set to output discharge or no action, the MP8870 continues switching and triggers a negative current limit to discharge V_{OUT}.

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If the response is set to latch off, the MP8870 latches off. VIN or EN must be recycled to enable the MP8870 again.

The OVP function is enabled after SS finishes.

Over-Temperature Protection (OTP)

The MP8870 provides over-temperature protection (OTP). The MP8870 monitors the junction temperature internally. If the junction temperature exceeds the threshold value (typically 150°C), OTP is triggered. After OTP is triggered, the device enters hiccup mode or latches off, depending on MFR_FAULT_RESPONSE (D6h), bit[3]. If bit[3] = 1b'1, it is a non-latch protection.

There is a hysteresis of about 20°C. Once the junction temperature drops to about 130°C, a soft start is initiated. The OTP function is effective once the MP8870 is enabled. If bit[3] = 1b'0, the device latches off. VIN or EN must be recycled to enable the MP8870 again.

GPIO

The MP8870 has a GPIO pin that can be configured as power good (PG) or a PMBus Alert (PMBUS_ALERT) via MFR_SYS_CTRL (D7h), bits[5]. When bit[5] = 1b'1, the GPIO pin functions as a PG pin. If bit[5] = 1b'0, the GPIO pin functions as a PMBus alert pin.

Power Good (PG)

The MP8870 has a power good (PG) output when the GPIO pin is set to act as PG via MFR_SYS_CTRL (D7h), bit[5]. PG is an open-drain output. For power good indication, this pin requires an external pull-up resistor (typically 100kΩ) to connect PG to VCC or an external voltage source. After applying the input voltage, the MOSFET turns on, so PG is pulled to GND before SSTRK is ready.

After V_{FB} reaches 90% of V_{REF}, PG is pulled high after a 0.1ms (default value) delay. PG implements an adjustable deglitch time via MFR_SYS_CTRL, bits[4:2] whenever V_{OUT} crosses the UV or OV rising and falling threshold. This guarantees correct power good indication when V_{OUT} is scaled through the I²C.

The PG output is pulled low immediately if EN under-voltage lockout (UVLO), input UVLO, OCP, or OTP are triggered.

If the V_{OUT} OVP, OTP, or OCP action is not latch-off when V_{FB} drops to 80% of the V_{REF}, or V_{FB} exceeds 120% of V_{REF}, PG is pulled low. PG can be pulled high again after V_{FB} rises to 90% of V_{REF}, or if it drops to 110% of V_{REF}.

If the V_{IN} supply fails to power the MP8870, PG is clamped to about 0.7V.

PMBus Alert (PMBUS_ALERT)

When the GPIO pin is configured to act as PMBUS_ALERT, it reports an alert to the host if any alert items are detected. This pin is an open-drain output that outputs high to indicate that no alert item has occurred, while it pulls low to indicate that an alert item has occurred.

Enable (EN) Configuration

The MP8870 has an enable (EN) control pin. EN is a high-voltage pin that can be directly connected to VIN (or through a resistor) for automatic start-up.

The MP8870 turns on when EN goes high and the OPERATION command sets the device on; the MP8870 turns off when EN pulls low or is floating. EN can also be driven by an analog or digital control logic signal to enable or disable the device. The MP8870 provides accurate EN thresholds, so a resistor divider connected from VIN to AGND can configure the V_{IN} threshold. If there is no dedicated EN control logic signal, it is recommended to use a resistor divider in applications to avoid possible UVLO bouncing during start-up and shutdown. The resistor divider values can be calculated with Equation (3):

$$V_{IN_{START}}(V)=1.26V\times\frac{R_{UP}+R_{DOWN}//1500}{R_{DOWN}//1500} \quad (3)$$

Where R_{UP} and R_{DOWN} are in kΩ. For example, if R_{UP} = 499kΩ and R_{DOWN} = 100kΩ, set $V_{IN\text{-}START}$ to 8V. Figure 6 on page 24 shows how to set up the resistor dividers.

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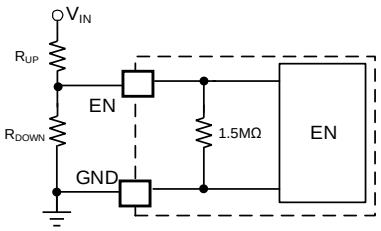


Figure 6: Setting the V_{IN} UVLO Threshold

Output Voltage Setting and Dynamic Scaling

The output voltage can be set to external voltage divider mode or I²C-configurable mode via MFR_VOUT_CTRL (D2h), bit[4].

When the device is set to I²C-configurable mode, the VOUT_SCALE_LOOP command is ignored. The output voltage range can be set from 0.3V to 1.536V or 0.6V to 3.072V via MFR_VOUT_CTRL (D2h), bit[0].

When the device is set to external voltage divider mode, V_{REF} is limited between 0.3V and 1.536V. If VOUT_COMMAND and VOUT_SCALE_LOOP set V_{REF} to exceed 1.536V, then V_{REF} is limited to 1.536V; if V_{REF} is set below 0.3V (e.g. 0.2V), then V_{REF} may be inaccurate. When the MP8870 is enabled, V_{OUT} starts to ramp up with a configured soft-start time. After that, the I²C bus can communicate with the master. If there is no communication on the I²C bus line, the MP8870 acts similar to a traditional non-I²C part. Once the I²C receives a valid output reference and voltage scaling instruction, V_{OUT} is determined by the resistor dividers (R1 and R2) and V_{REF}. V_{OUT} can be estimated with Equation (4):

$$V_{OUT} = V_{REF} \times (\frac{R1}{R2} + 1) \quad (4)$$

Where V_{REF} is 0.4V. The output voltage scaling is realized by adjusting V_{REF}, which is the non-inverted input of the error amplifier. After the MP8870 receives valid data for the V_{REF} setting, it sends the command to adjust V_{REF} with a controlled slew rate. The slew rate can be configured via MFR_VOUT_TRANSITION_RATE.

Reference Voltage Setting

Figure 7 shows how V_{REF} is set.

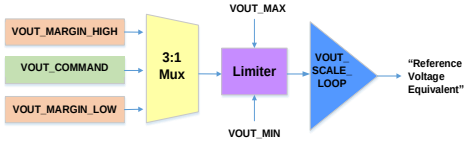


Figure 7: Reference Voltage Setting

At first, the nominal V_{OUT} is selected from one of three input sources: VOUT_COMMAND, VOUT_MARGIN_HIGH, and VOUT_MARGIN_LOW. The input source is selected by the OPERATION command, and passed on to the rest of the V_{OUT} command process.

Then the commanded voltage is compared to the limits set by the VOUT_MAX and VOUT_MIN commands. If the calculated voltage command creates a V_{OUT} that exceeds VOUT_MAX or is below VOUT_MIN, the PMBus device limits the commanded voltage passed to the controller to the VOUT_MAX or VOUT_MIN value.

Lastly, the same scaling factor is applied to the calculated voltage by multiplying the calculated voltage command by VOUT_SCALE_LOOP. If the MP8870 operates in an I²C-configurable mode, the VOUT_SCALE_LOOP command should be ignored. At this point, the device has a calculated value that is used as the equivalent value to the reference voltage in a standard analog controller.

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I²C/PMBUS INTERFACE

I²C/PMBus Serial Interface Description

The I²C/PMBus interface is a two-wire, bidirectional serial interface consisting of a data line (SDA) and a clock line (SCL). The lines are pulled to a bus voltage externally when they are idle. When connecting to the line, a master device generates the SCL signal and device address, then arranges the communication sequence. The MP8870 interface is an I²C slave. The I²C interface adds flexibility to the power supply solution. The output voltage, transition slew rate, and other parameters can be controlled by the I²C interface instantaneously.

Data Validity

One clock pulse is generated for each data bit transferred. The data on the SDA line must be stable during the high period of the clock. The high or low state of the data line can only change when the clock signal on the SCL line is low (see Figure 8).

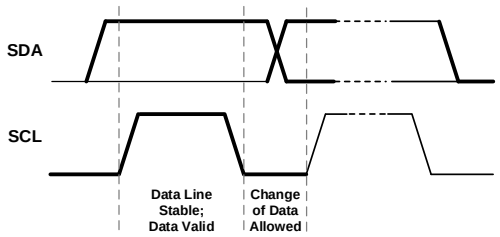


Figure 8: Bit Transfer on the I²C Bus

Start and stop are signaled by the master device, which signifies the beginning and the end of the I²C transfer. The start command is defined as the SDA signal transitioning from high to low while the SCL is high. The stop command is defined as the SDA signal transitioning from low to high while the SCL is high (see Figure 9).

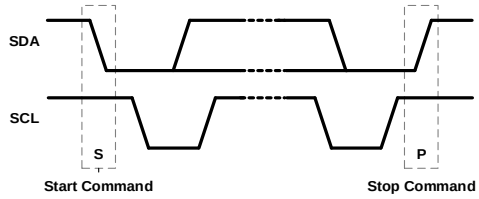


Figure 9: Start and Stop Commands

Start and stop commands are always generated by the master. The bus is considered to be busy after the start command, and it is considered to be free again after a minimum of 4.7µs after the stop command. The bus remains busy if a repeated start (Sr) command is generated instead of a stop command. The start (S) and repeated start (Sr) commands are functionally identical.

Transfer Data

Every byte put on the SDA line must be eight bits long. Each byte has to be followed by an acknowledge (ACK) bit. The acknowledge-related clock pulse is generated by the master. The transmitter releases the SDA line (high) during the acknowledge clock pulse. The receiver must pull down the SDA line during the acknowledge clock pulse so that it remains stable low during the high period of this clock pulse.

Figure 10 shows the data transfer format. After the start command, a slave address is sent. This address is 7 bits long, followed by an eighth bit data direction bit (R/W). A 0 indicates a transmission (write), and a 1 indicates a request for data (read). A data transfer is always terminated by a stop command generated by the master. However, if a master still wishes to communicate on the bus, it can generate a repeated start command and address another slave without first generating a stop command.

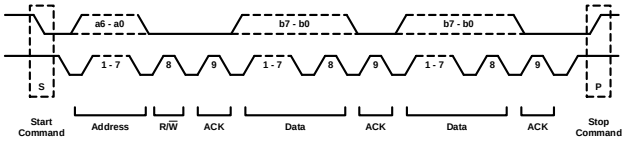


Figure 10: Complete Data Transfer

The MP8870 requires a start condition, a valid I²C address, a register address byte, and a data byte for a single data update. After receiving each byte, the MP8870 acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the MP8870. The MP8870 performs an update on the falling edge of the LSB byte.

I²C Slave Address

To support multiple devices used on the same I²C bus, the A0 pin can be used to configure the MP8870's address. There is 10µA of current flowing out of A0. Connect a resistor between A0 and AGND to set the A0 voltage.

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The internal circuit changes the I²C address accordingly. When the master sends an 8-bit address value, the 7-bit I²C address should be followed by a 0 or 1 to indicate a write or read operation, respectively. Table 1 shows the recommend I²C address selection for the A0 resistor. A resistor with a 1% accuracy must be used to set the address.

Table 1: Recommend I²C Slave Address Selection by A0 Resistor

A0 Pull-Down Resistor (R_{A0_DOWN}, in kΩ)	I²C Slave Address	
	Binary	Hex
0	100 0000	40h
30	100 0001	41h
47	100 0010	42h
68	100 0011	43h
88.7	100 0100	44h
107	100 0101	45h
NC	100 0110	46h

Packet Error Checking (PEC)

The MP8870 PMBus interface supports the use of a packet error checking (PEC) byte. The PEC byte is transmitted by the MP8870 during a read transaction, or it is sent by the bus host to the MP8870 during a write transaction.

The PEC byte is used by the bus host or the MP8870 to detect errors during a bus transaction (depending on whether the transaction is a read or a write).

If the host determines that the PEC byte read during a read transaction is incorrect, it can decide to repeat the read if necessary. If the MP8870 determines that the PEC byte sent during a write transaction is incorrect, it ignores the command (does not execute it) and sets a status flag. Within a group command, the host can choose to send or not send a PEC byte as part of the message to the MP8870.

Multi-Time Programmable (MTP) Memory

The MP8870 has built-in multiple-time programmable (MTP) memory cells to store user configurations. The standard command STORE_USER_ALL (15h) is used for the MTP.

When the MTP is being configured, V_{CC} may rise as high as 5V. Consider this possibility if VCC is connected to circuits that cannot support such a high voltage. MTP programming typically takes about 400ms.

The standard version of this device (MP8870-0000) can be configured twice.

Figure 11 shows a send byte without PEC and a send byte with PEC. Figure 12 shows a write byte without PEC and a write byte with PEC. Figure 13 on page 27 shows a write word without PEC and a write word with PEC. Figure 14 on page 27 shows a read byte without PEC and a read byte with PEC. Figure 15 on page 27 shows a write word without PEC and a write word with PEC.

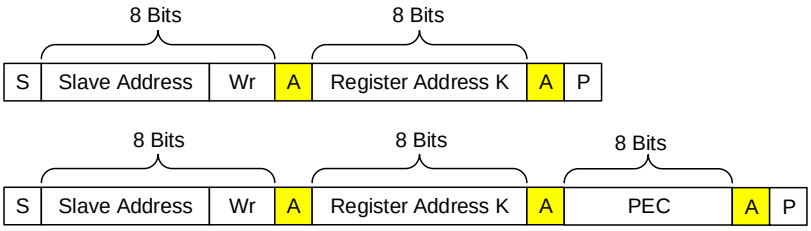


Figure 11: Send Byte without PEC and Send Byte with PEC

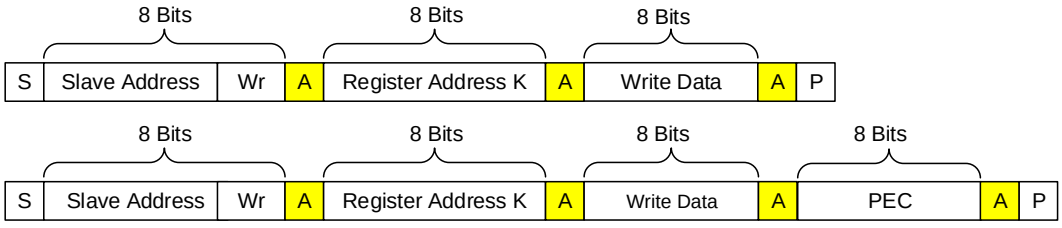


Figure 12: Write Byte without PEC and Write Byte with PEC

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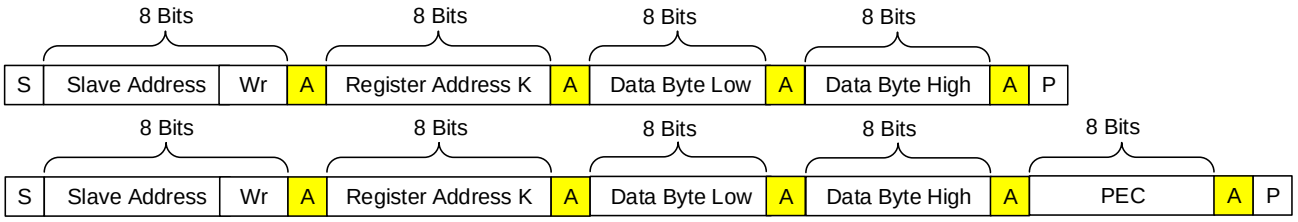


Figure 13: Write Word without PEC and Write Word with PEC

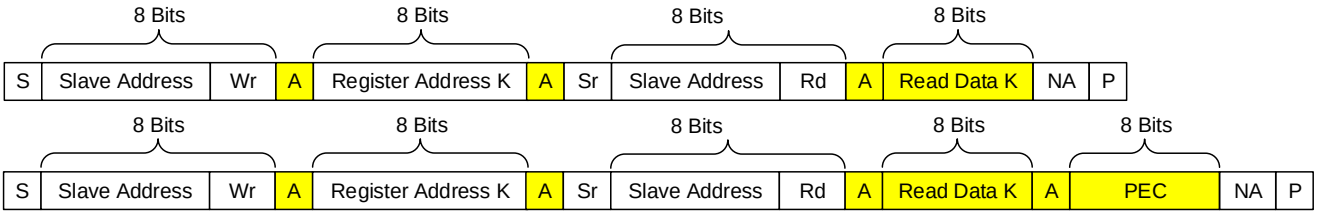


Figure 14: Read Byte without PEC and Read Byte with PEC

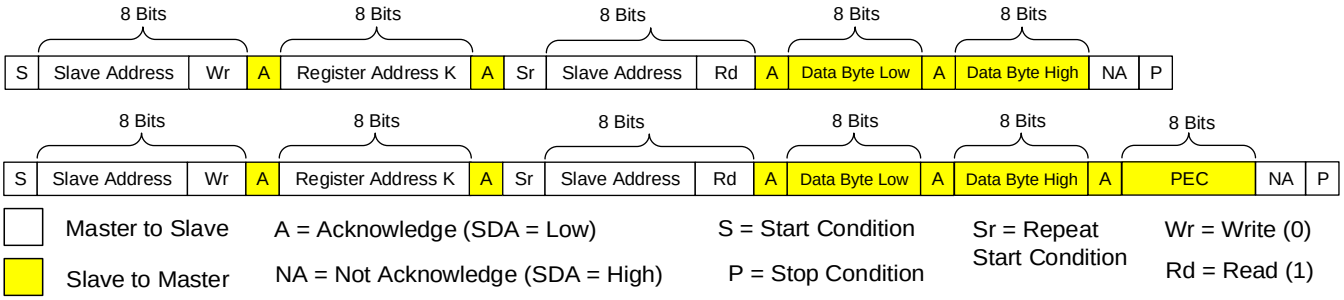


Figure 15: Read Word without PEC and Read Word with PEC

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PMBUS REGISTER MAP

Command Name	Command Code	Type	Data Format	Bytes	Default Value	MTP
OPERATION	01h	R/W	Reg	1	0x80	Yes
CLEAR_FAULTS	03h	Send Byte	-	0	-	No
WRITE_PROTECT	10h	R/W	Reg	1	0x00	No
STORE_USER_ALL	15h	Send Byte	-	0	-	No
RESTORE_USER_ALL	16h	Send Byte	-	0	-	No
CAPABILITY	19h	R	Reg	1	0x50	No
VOUT_MODE	20h	R	Reg	1	0x16	No
VOUT_COMMAND	21h	R/W	Linear L16	2	0x0400	Yes
VOUT_MAX	24h	R/W	Linear L16	2	0x7FFF	Yes
VOUT_MARGIN_HIGH	25h	R/W	Linear L16	2	0x0625	Yes
VOUT_MARGIN_LOW	26h	R/W	Linear L16	2	0x0200	Yes
VOUT_SCALE_LOOP	29h	R/W	Linear L11	2	0xB8CD	Yes
VOUT_MIN	2Bh	R/W	Linear L16	2	0x0000	Yes
TON_RISE	61h	R/W	Linear L11	2	0x0000	Yes
TOFF_FALL	65h	R/W	Linear L11	2	0x0000	Yes
STATUS_BYTE	78h	R	Reg	1	0x00	No
STATUS_WORD	79h	R	Reg	2	0x1000	No
STATUS_VOUT	7Ah	R	Reg	1	0x00	No
STATUS_IOUT	7Bh	R	Reg	1	0x00	No
STATUS_INPUT	7Ch	R	Reg	1	0x00	No
STATUS_ TEMPERATURE	7Dh	R	Reg	1	0x00	No
STATUS_CML	7Eh	R	Reg	1	0x00	No
STATUS_ MFR_SPECIFIC	80h	R	Reg	1	0x02	No
PMBUS_REVISION	98h	R/W	Reg	1	0x33	No

Data Format Linear16 and Linear11

The Linear16 (L16) format is used for most V_{OUT} related commands (see Figure 16).

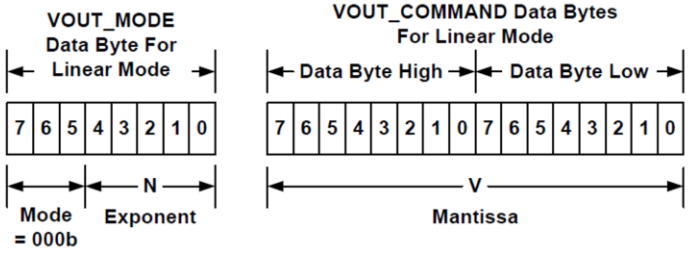


Figure 16: Linear16 Format

The MODE bits are set to 000b. The voltage (in V) can be calculated with Equation (5):

$$Voltage = V \times 2^{N} \quad (5)$$

Where Voltage is the parameter of interest (in V), V is a 16-bit unsigned binary integer, and N is a 5-bit, two's complement, binary integer. The Linear11 (L11) format is used for other commands (see Figure 17 on page 29).

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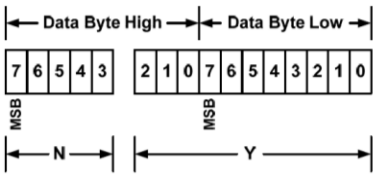


Figure 17: Linear11 Format

The relationship between Y, N and the real-world value can be estimated with Equation (6):

$$X = Y \times 2^N \quad (6)$$

Where X is the real-world value; Y is an 11-bit, two's complement integer; and N is a 5-bit, two's complement integer.

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PMBUS REGISTERS

OPERATION (01h)

The OPERATION command turns the converter output on or off in conjunction with the input from the EN pin. OPERATION also sets the output voltage (V_{OUT}) to the upper or lower margin voltages. The MP8870 remains in the commanded operating mode until a subsequent OPERATION command is received, or a change in the state of the EN pin instructs the converter to change to another mode.

Command	OPERATION							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R	R	R	R
Function	ON/OFF				X	X	X	X
Default (0x80)	1	0	0	0	0	0	0	0

Bits	Name	Default	Description
D[7]	ON/OFF	1	0: Off 1: On
D[6]	OFF_BEHAVIOR	0	0: Turn off immediately. Any shutdown sequencing commands are ignored 1: Soft shutdown. The soft shutdown time is set by TOFF_FALL
D[5:4]	OUTPUT_VOLTAGE_SOURCE	00	00: The nominal V_{OUT} is set by the VOUT_COMMAND register 01: The nominal V_{OUT} is set by the VOUT_MARGIN_LOW register 10: The nominal V_{OUT} is set by the VOUT_MARGIN_HIGH register
D[3:0]	RESERVED	0000	Reserved.

CLEAR_FAULTS (03h)

The CLEAR_FAULTS command clears any fault bits that have been set. This command clears all bits in all status registers simultaneously. At the same time, the device clears its ALT# signal output if the device is asserting the ALT# signal. If the MP8870 has latched off due to a fault condition, issuing a CLEAR_FAULTS command does not restart the device. If the fault is still present when the bit is cleared, then the fault bit immediately sets again, and the host is notified. This command is write-only. There is no data byte for this command.SYS

WRITE_PROTECT (10h)

The WRITE_PROTECT command controls writing to the MP8870. This command is meant to provide protection against accidental changes.

Command	WRITE_PROTECT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R	R
Default (0x00)	0	0	0	0	0	0	0	0

Bits	Name	Default	Description
D[7:4]	WRITING_PROTECT_RANGE	0000	Controls the writing protection range. 1000: Disable all writes except to the WRITE_PROTECT command 0100: Disable all writes except to the WRITE_PROTECT and OPERATION commands 0010: Disable all writes except to the WRITE_PROTECT, OPERATION, and VOUT_COMMAND commands 0000: Enable writes to all commands
D[3:0]	RESERVED	0000	Reserved.

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Note that SENDBYTE commands are not protected by WRITE_PROTECT. When 10h is set to a value other than 0x00, the SENDBYTE commands are valid.

STORE_USER_ALL (15h)

The STORE_USER_ALL command instructs the PMBus device to copy the entire contents of the operating memory (the I²C register) to the matching locations in the non-volatile user store memory (the MTP). Any items in operating memory that do not have matching locations in the user store are ignored.

The MP8870 automatically increases V_{CC} to 5V and turns EN off (set the OPERATION register to 0x00), then it writes all the data from the converter's memory map to the internal MTP. After the MP8870 finishes writing to the MTP block, it reduces V_{CC} to 3.5V and restarts (set OPERATION register to 0x80) with the new configuration data from MTP. This process begins when the MP8870 receives a STORE_USER_ALL command from the I²C interface. The standard version of the MP8870GL-0000 can be configured two times. After the MP8870 has been configured twice, the MTP register configuration can no longer be configured.

This command has no data bytes. This command is write-only.

RESTORE_USER_ALL (16h)

The RESTORE_USER_ALL command instructs the PMBus device to copy the entire contents of the MTP to the matching locations in the operating memory. The values in the operating memory are overwritten by the value retrieved from the user store. Any items in user store that do not have matching locations in the operating memory are ignored.

The RESTORE_USER_ALL command can be used while the device has been configured by the MTP. While restoring MTP data to the user memory, the device executes a CRC calculation and compares the calculation result with the stored CRC check result in the MTP cell. The MTP value is restored to the operating memory only when these values match one another.

This command has no data bytes. This command is write-only.

CAPABILITY (19h)

The CAPABILITY command returns information about the PMBus functions supported by the MP8870. This command is read with the PMBus read byte protocol.

Command	CAPABILITY							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	PEC_EN_FLAG			X	X	X	X	X
Default (0x50)	0	1	0	1	0	0	0	0

Bits	Name	Default	Description
D[7]	PEC_EN_FLAG	0	Indicates the status of the PEC_EN flag. 0: PEC_EN = 0 1: PEC_EN = 1
D[6:5]	MAXIMUM_BUS_SPEED	10	The maximum supported bus speed is 1MHz.
D[4:0]	RESERVED	10000	Reserved.

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VOUT_MODE (20h)

The VOUT_MODE command returns the V_{OUT} mode. The MP8870 only supports linear mode, so the MODE bits are set to 000b by default. N is fixed to -10.

Command	VOUT_MODE							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	MODE			N				
Default	0	0	0	1	0	1	1	0

Bits	Name	Default	Description
D[7:5]	MODE	000	Indicates that the MP8870 supports linear mode.
D[4:0]	N	10110	Fixed to -10.

VOUT_COMMAND (21h)

The VOUT_COMMAND command sets V_{OUT}. The feedback reference voltage can be calculated with (VOUT_COMMAND x VOUT_SCALE_LOOP).

Command	VOUT_COMMAND															
Format	Linear															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	V															
Default	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Bits	Name	Default	Description
D[15]	SIGN	0	Signed bit. This bit is fixed to 0.
D[14:0]	V	0x0400	V_{OUT} (in V) can be calculated with the following equation: V_{OUT} (V) = V x 2^N Where N is fixed to -10.

The default value of VOUT_COMMAND (21h) is 1V, which is 0x0400. The V_{OUT} command accuracy is 1.5mV/K, where K is the VOUT_SCALE_LOOP value.

VOUT_MAX (24h)

The VOUT_MAX command sets an upper limit on the nominal V_{OUT} that the converter can command, regardless of any other commands or combinations. This command provides a safeguard against V_{OUT} being accidently set to a destructive value. It is not the primary output over-voltage protection (OVP).

Command	VOUT_MAX															
Format	Linear															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	V															
Default	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Name	Default	Description
D[15]	SIGN	0	Signed bit. This bit is fixed to 0.
D[14:0]	V	0x7FFF	V_{OUT_MAX} (in V) can be calculated with the following equation: V_{OUT_MAX} (V) = V x 2^N Where N is fixed to -10.

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VOUT_MARGIN_HIGH (25h)

The VOUT_MARGIN_HIGH command sets the high margin for V_{OUT}.

Command	VOUT_MARGIN_HIGH															
Format	Linear															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function		V														
Default	0	0	0	0	0	1	1	0	0	0	1	0	0	1	0	1

Bits	Name	Default	Description
D[15]	SIGN	0	Signed bit. This bit is fixed to 0.
D[14:0]	V	0x0625	$V_{OUT_MARGIN_HIGH}$ (in V) can be calculated with the following equation: $V_{OUT_MARGIN_HIGH}$ (V) = V x 2^N Where N is fixed to -10.

The default value of VOUT_MARGIN_HIGH (25h) is 1.536V, which is 0x0625.

VOUT_MARGIN_LOW (26h)

The VOUT_MARGIN_LOW command sets the low margin for V_{OUT}.

Command	VOUT_MARGIN_LOW															
Format	Linear															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function		V														
Default	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Bits	Name	Default	Description
D[15]	SIGN	0	Signed bit. This bit is fixed to 0.
D[14:0]	V	0x0200	$V_{OUT_MARGIN_LOW}$ (in V) can be calculated with the following equation: $V_{OUT_MARGIN_LOW}$ (V) = V x 2^N Where N is fixed to -10.

The default value of 26h is 0.5V, which is 0x0200

VOUT_SCALE_LOOP (29h)

The VOUT_SCALE_LOOP command helps set the reference voltage.

Command	VOUT_SCALE_LOOP															
Format	Linear															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	N						Y									
Default	1	0	1	1	1	0	0	0	1	1	0	0	1	1	0	1

Bits	Name	Default	Description
D[15:11]	N	10111	Fixed to -9.
D[10]	SIGN	0	Signed bit. This bit is fixed to 0.
D[9:0]	Y	0011001101	$V_{OUT_SCALE_LOOP}$ (in V) can be calculated with the following equation: $V_{OUT_SCALE_LOOP}$ (V) = Y x 2^N Where N is fixed to -9, and VOUT_SCALE_LOOP is the value for K (0.4 by default).

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Note that changing VOUT_SCALE_LOOP is only valid after EN turns off (set the OPERATION register to 0x00) and restarts (set the OPERATION register to 0x80). After writing to the register, write OPERATION to off and then on to enable the new configuration of VOUT_SCALE_LOOP.

VOUT_MIN (2Bh)

The VOUT_MIN command sets a lower limit on the nominal V_{OUT} that the converter can command, regardless of any other commands or combinations. This command provides a safeguard against V_{OUT} being accidently set to a destructive value. It is not the primary output under-voltage protection (UVP).

Command	VOUT_MIN															
Format	Linear															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function		V														
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Default	Description
D[15]	SIGN	0	Signed bit. This bit is fixed to 0.
D[14:0]	V	0x0000	V_{OUT_MIN} (in V) can be calculated with the following equation: V_{OUT_MIN} (V) = V x 2^N Where N is fixed to -10.

TON_RISE (61h)

The TON_RISE command sets the time (in ms) from when the output starts to rise until the voltage has reached the regulation point.

Command	TON_RISE															
Format	Linear															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W
Function	N					X	X	X	X	X	X	X	Y			
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Default	Description
D[15:11]	N	00000	N is fixed to 0
D[10:4]	RESERVED	0000000	Reserved.
D[3:0]	Y	0000	t_{ON_RISE} (in ms) can be calculated with the following equation: t_{ON_RISE} (ms) = Y x 2^N + 1 Where N is fixed to 0.

The default value of TON_RISE (61h) is 1ms, which is 0x0000.

TON_FALL (65h)

The TOFF_FALL command sets the time (in ms) from when the output starts to fall until the voltage has reached the regulation point.

Command	TOFF_FALL															
Format	Linear															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W
Function	N					X	X	X	X	X	X	X	Y			
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bits	Name	Default	Description
D[15:11]	N	00000	N is fixed to 0
D[10:4]	RESERVED	0000000	Reserved.
D[3:0]	Y	0000	t_{ON_FALL} (in ms) can be calculated with the following equation: t_{ON_FALL} (ms) = Y x 2^N + 1 Where N is fixed to 0.

The default value of TON_FALL (65h) is 1ms, which is 0x0000.

STATUS_BYTE (78h)

The STATUS_BYTE command returns the value of a number of flags that indicate the state of the MP8870. To clear the bits in this register, remove the underlying fault and issue a CLEAR_FAULTS command.

Bits	Name	Behavior	Default	Description
D[7]	UNIT_BUSY	Live	0	Flag that indicates if the unit is busy. 0: No fault has been detected 1: A fault was declared because the device was busy and unable to respond
D[6]	OFF	Live	0	Flag that indicates whether the IC is off. 0: The IC is enabled 1: The IC is disabled due to an over-current (OC) latch-off fault, over-temperature (OT) latch-off fault, over-voltage (OV) latch-off fault, under-voltage (UV) latch-off fault, or an OPERATION off command
D[5]	VOUT_OV	Live	0	Flag the indicates whether a V_{OUT} over-voltage (OV) fault has occurred. 0: No output OV fault has occurred 1: An output OV fault has occurred
D[4]	IOUT_OC	Live	0	Flag the indicates whether an I_{OUT} over-current (OC) fault has occurred. 0: No OC fault has occurred 1: An OC fault has occurred
D[3]	RESERVED	-	0	Reserved.
D[2]	OT_FAULT	Live	0	Flag the indicates whether an IC over-temperature (OT) fault has occurred. 0: No OT fault has been detected 1: An OT fault has been detected.
D[1]	CUMM_ERROR	Live	0	Flag that indicates if a communication error has been received. 0: No command error has been received 1: A command that is not supported has been received.
D[0]	NONE_OF_THE_ABOVE	Live	0	0: No other fault has occurred 1: A fault not listed in bits[7:1] has occurred

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STATUS_WORD (79h)

The STATUS_WORD command returns the value of a number of flags that indicate the state of the MP8870. To clear the bits in this register, remove the underlying fault and issue a CLEAR_FAULTS command.

Bits	Name	Behavior	Default	Description
D[15]	VOUT_STATUS	Live	0	0: STATUS_VOUT = 0 1: One bit (or more) in the STATUS_VOUT register = 1
D[14]	IOUT_STATUS	Live	0	0: STATUS_IOUT = 0 1: One bit (or more) in the STATUS_IOUT register = 1
D[13]	VIN_STATUS	Live	0	0: STATUS_IOUT = 0 1: One bit (or more) in the STATUS_INPUT register = 1
D[12]	RESERVED	-	11	Reserved.
D[11]	PG_STATUS	Live	0	0: The PG signal has asserted 1: No PG signal has asserted
D[10:8]	RESERVED	-	000	Reserved.
D[7:0]	STATUS_BYTE	Live	0x00	STATUS_BYTE is the lower byte of STATUS WORD.

STATUS_VOUT (7Ah)

The STATUS_VOUT command returns one data byte with content regarding V_{OUT}. To clear the bits in this register, remove the underlying fault and issue a CLEAR_FAULTS command.

Bits	Name	Behavior	Default	Description
D[7]	VOUT_OV_ FAULT	Live	0	Indicates whether V_{OUT} exceeds 120% of the nominal output voltage. 0: No output over-voltage (OV) fault has occurred 1: An output OV fault has occurred
D[6:5]	RESERVED	-	00	Reserved.
D[4]	VOUT_UV_ FAULT	Live	0	Indicates whether V_{OUT} is below 90% of the nominal output voltage. 0: No V_{OUT} under-voltage (UV) fault has occurred 1: a V_{OUT} UV fault has occurred
D[3]	VOUT_MAX	Live	0	0: No VOUT_MAX warning has occurred 1: An attempt has been made to set V_{OUT} to a value higher than allowed value by the VOUT_MAX command
D[2:0]	RESERVED	-	000	Reserved.

STATUS_IOUT (7Bh)

The STATUS_IOUT command returns one data byte with content regarding I_{OUT}. To clear the bits in this register, remove the underlying fault and issue a CLEAR_FAULTS command.

Bits	Name	Behavior	Default	Description
D[7]	IOUT_OC_ FAULT	Live	0	0: No I_{OUT} over-current (OC) fault has occurred 1: An I_{OUT} OC fault has occurred
D[6:0]	RESERVED	-	0	Reserved.

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STATUS_INPUT (7Ch)

The STATUS_INPUT command returns the value of flags indicating the MP8870's input voltage status. To clear the bits in this register, remove the underlying fault and issue a CLEAR_FAULTS command.

Bits	Name	Behavior	Default	Description
D[7]	VIN_OV_FAULT	Live	0	0: No V_{IN} over-voltage (OV) fault has occurred 1: A V_{IN} OV fault has occurred
D[6:0]	RESERVED	-	0	Reserved.

STATUS_TEMPERATURE (7Dh)

The STATUS_TEMPERATURE command returns the value of flags indicating the MP8870's silicon temperature status. To clear the bits in this register, remove the underlying fault and issue a CLEAR_FAULTS command.

Bits	Name	Behavior	Default	Description
D[7]	OT_FAULT	Live	0	The over-temperature (OT) fault threshold is 150°C. 0: No OT fault has occurred 1: An OT fault has occurred
D[6:0]	RESERVED	-	0	Reserved.

STATUS_CML (7Eh)

The STATUS_CML command returns the value of flags indicating the MP8870's PMBus command status. To clear the bits in this register, remove the underlying fault and issue a CLEAR_FAULTS command.

Bits	Name	Behavior	Default	Description
D[7]	CMD_FAULT	Live	0	0: No invalid or unsupported commands have been received 1: An invalid or unsupported command has been received.
D[6]	DATA_FAULT	Live	0	0: No invalid or unsupported data has been received 1: Invalid or unsupported data has been received
D[5]	PEC_FAULT	Live	0	0: No PEC error has occurred 1: A PEC error has occurred
D[4]	OTP_FAULT	Live	0	0: No OTP CRC error, OTP invalid error, or store fail error has occurred 1: An OTP CRC error, OTP invalid error, or store fail error has occurred
D[3:2]	RESERVED	-	0	Reserved.
D[1]	PMBUS_FAULT	Live	0	0: No PMBus start and end signal error, or long length error has occurred 1: A PMBus start and end signal error, or long length error has occurred
D[0]	RESERVED	-	0	Reserved.

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STATUS_MFR_SPECIFIC (80h)

The STATUS_MFR_SPECIFIC command returns the value of flags indicating the MP8870's status. To clear the bits in this register, remove the underlying fault and issue a CLEAR_FAULTS command.

Bits	Name	Behavior	Default	Description
D[7]	RESERVED	-	0	Reserved.
D[6]	CHECK_SUM_ FLAG	Live	0	0: The MTP page has passed the CRC or checksum check 1: The MTP page has a CRC or checksum error
D[5]	OC_FLAG	Live	0	0: No over-current (OC) fault has occurred 1: An OC fault has occurred
D[4]	OT_FAULT	Live	0	0: No over-temperature (OT) fault has occurred 1: An OT fault has occurred
D[3]	RESERVED	-	0	Reserved.
D[2]	PG_FLAG	Live	0	0: The output is within the PG window 1: The output is outside of the PG window
D[0]	VO_REJECT_ FLAG	Live	0	0: No reject events have occurred 1: One of the following events has occurred: • The code for VOUT_COMMAND exceeds the value set by VOUT_MAX • The I²C writes a DAC reference while V_{OUT} is ramping up or ramping down • I²C writes a DAC reference during soft start VO_REJECT_FLAG does not report ALERT.

PMBUS_REVISION (98h)

The PMBUS_REVISION command stores or reads the revision of the PMBus to which the MP8870 is compliant.

Bits	Name	Default	Description
D[7:4]	PMBUS_PART_I REVISION	0011	Indicates Part I Revision 1.3
D[3:0]	PMBUS_PART_II_ REVISION	0011	Indicates Part II Revision 1.3

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MFR REGISTER MAP

Command Name	Command Code	Type	Data Format	Bytes	Default Value (MP8870GL-0001)	MTP
MFR_VOUT_CTRL	D2h	R/W	Reg	1	0x00	Yes
MFR_VOUT_TRANSITION_RATE	D3h	R/W	Reg	1	0x01	Yes
MFR_FREQUENCY_SWITCH	D4h	R/W	Reg	1	0x02	Yes
MFR_OC_FAULT_LIMIT	D5h	R/W	Reg	1	0x12	Yes
MFR_FAULT_RESPONSE	D6h	R/W	Reg	1	0x19	Yes
MFR_SYS_CTRL	D7h	R/W	Reg	1	0x08	Yes
MFR_FAULT_MASK	D8h	R/W	Reg	1	0xFF	Yes
MFR_VENDER_ID	D9h	R	Reg	1	0xA0	No
MFR_USER_ID0	DAh	R/W	Reg	1	0x00	Yes
MFR_USER_CODE	DBh	R/W	Reg	1	0x01	Yes
MFR_USER_REVISION	DCh	R/W	Reg	1	0x00	Yes
MFR_PRODUCTION_ID	DDh	R	Reg	1	0x70	No
MFR_SILICON_REVISION	DEh	R	Reg	1	0x00	No
MFR_MTP_STATUS	EAh	R	Reg	1	0x04	No

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MFR REGISTERS

MFR_VOUT_CTRL (D2h)

The MFR_CTRL_VOUT command adjusts the V_{OUT} behaviors.

Bits	Name	Default	Description
D[7:5]	RESERVED	000	Reserved.
D[4]	OUTPUT_VOLTAGE_ SET_MODE	0	0: External voltage divider mode 1: I²C-configurable mode
D[3:1]	RESERVED	000	Reserved.
D[0]	VREF_RANGE_I2C_ MODE	0	0: 1/1 range (0.3V to 1.536V) 1: 1/2 range (0.6V to 3.072V)

Note that changing MFR_VOUT_CTRL is only valid after EN turns off (set the OPERATION register to 0x00) and restarts (set the OPERATION register to 0x80). After writing to the register, write OPERATION to off and then on to enable the new configuration of MFR_VOUT_CTRL.

MFR_VOUT_TRANSITION_RATE (D3h)

The MFR_VOUT_TRANSITION_RATE command adjusts the transition slew rate of the reference voltage.

Bits	Name	Default	Description
D[7:3]	RESERVED	0	Reserved.
D[2:0]	VREF_TRANS_RATE	001	Sets the reference voltage transition slew rate. 000: K x 0.025mV/µs 001: K x 0.0625mV/µs 010: K x 0.125mV/µs 011: K x 0.25mV/µs 100: K x 0.5mV/µs 101: K x 1.25mV/µs 110: K x 2.5mV/µs Other: Reserved Where K is VOUT_SCALE_LOOP register value in external voltage divider mode. K = 1 in I²C-configurable mode.

MFR_VOUT_FREQUENCY_SWITCH (D4h)

The MFR_VOUT_FREQUENCY_SWITCH command adjusts the MP8870's light-load operation mode and f_{SW}.

Bits	Name	Default	Description
D[7:5]	RESERVED	0	Reserved.
D[4:3]	LIGHT_LOAD_ OPERATION_MODE	00	Sets the operation mode. 00: Pulse-frequency modulation (PFM) mode 01: Forced continuous conduction mode (FCCM) Others: Reserved
D[2:0]	CCM_MODE_ SWITCHING_ FREQUENCY	010	Sets the switching frequency (f_{SW}): 000: 300kHz 001: 500kHz 010: 650kHz 011: 1MHz 100: 1.4MHz 101: 2MHz Others: Reserved

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MFR_OC_FAULT_LIMIT (D5h)

The MFR_OC_FAULT_LIMIT command set the current limit thresholds.

Bits	Name	Default	Description
D[7:3]	RESERVED	00010	Reserved.
D[2:0]	OC_FAULT_LIMIT	010	Sets the current limit. Note that the peak current limit is PCL, the valley current limit is VCL, and the negative current limit is NCL. 000: PCL = 26A; VCL = 22A; NCL = I0A 001: PCL = 24A; VCL = 20A; NCL = -9A 010: PCL = 20A; VCL = 16A; NCL = -8A 011: PCL = 18A; VCL = 14A; NCL = -7A 100: PCL = 16A; VCL = 12A; NCL = -6A 101: PCL = 12A; VCL = 9A; NCL = -5A 110: PCL = 10A; VCL = 7A; NCL = -4A 111: PCL = 8A; VCL = 6A; NCL = -3A

MFR_FAULT_RESPONSE (D6h)

The MFR_FAULT_RESPONSE command sets the responses for V_{IN} OVP, OTP, OCP, and V_{OUT} OVP.

Bits	Name	Default	Description
D[7:5]	RESERVED	000	Reserved.
D[4]	VIN_OV_FAULT_ RESPONSE	1	Sets the V_{IN} over-voltage protection (OVP) behavior. 0: Normal switching. There is no protection 1: Hiccup mode, then automatic retry when V_{IN} falls below VIN_OV
D[3]	OT_FAULT_ RESPONSE	1	Sets the over-temperature protection (OTP) behavior. 0: Latch-off. Restart VIN or EN to enable the IC again 1: Automatic retry. The IC automatically retries after the silicon temperature falls below the hysteresis
D[2]	OCP_FAULT_ RESPONSE	0	Sets the response when the output inductor current exceeds CURRENT_LIMIT bit. In addition to what is listed below, the MP8870 executes the following: • Sets the IOUT_OC_FAULT bit in STATUS BYTE • Sets the IOUT_STATUS bit in STATUS_WORD • Sets the IOUT_OC_FAULT bit in STATUS_IOUT This bit sets the over-current (OC) behavior after under-voltage protection (UVP) has been triggered. 0: Hiccup mode 1: Latch-off mode
D[1:0]	OUT_OV_FAULT_ RESPONSE	01	Sets the V_{OUT} OVP behavior. 00: Latch-off mode 01: Output discharge 10: No action Others: Reserved

MFR_SYS_CTRL (D7h)

The MFR_SYS_CTRL command configures the system control.

Bits	Name	Default	Description
D[7]	PEC_EN	0	Sets the PEC behavior: 0: Disable PEC 1: Enable PEC

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D[6]	VOUT_DISCHARGE	0	Controls the output discharge behavior when EN is low. 0: No soft shutdown when the external EN pin is off 1: Soft shutdown while the external EN pin is off
D[5]	PG/ALERT SEL	0	Sets the GPIO pin's working mode. 0: The GPIO pin works as PG 1: The GPIO pin works as PMBUS_ALERT
D[4:2]	PG_DELAY	010	Sets the PG delay time. 000: 10μs 001: 50μs 010: 100μs 011: 200μs 100: 500μs 101: 1ms 110: 5ms 111: 10ms
D[1:0]	RESERVED	00	Reserved.

MFR_FAULT_MASK (D8h)

The MFR_FAULT_MASK command determines the faults of report alert. PMBUS_ALERT is pulled low to indicate faults that are not masked via this command.

Bits	Name	Default	Description
D[7]	CML_FAULT_MASK	1	0: No mask. If a CML fault occurs, ALERT = 0 1: Mask. ALERT is always 1
D[6]	IOUT_FAULT_MASK	1	0: No mask. If an I_{OUT} fault occurs, ALERT = 0 1: Mask. ALERT is always 1
D[5]	TEMPERATURE_ FAULT_MASK	1	0: No mask. If a temperature fault occurs, MFRALERT = 0 1: Mask. ALERT is always 1
D[4]	VOUT_FAULT_MASK	1	0: No mask. If a V_{OUT} fault occurs, ALERT = 0 1: Mask. ALERT is always 1.
D[3]	VIN_FAULT_MASK	1	0: No mask. If a V_{IN} fault occurs, ALERT = 0 1: Mask. ALERT is always 1.
D[2]	MFR_FAULT_MASK	1	0: No mask. If an MFR fault occurs, ALERT = 0 1: Mask. ALERT is always 1.
D[1]	BUSY_FAULT_MASK	1	0: No mask. If a PMBus busy fault occurs, ALERT = 0 1: Mask. ALERT is always 1
D[0]	SMALERT_MASK	1	0: No mask 1: Mask all of the above faults to report ALERT

MFR_VENDOR_ID (D9h)

Bits	Name	Default	Description
D[7:4]	VENDER_CODE	1010	Represents "MPS."
D[3:0]	RESERVED	0000	Reserved.

MFR_USER_ID0 (DAh)

Bits	Name	Default	Description
D[7:0]	MFR_USER_ID0	0x00	Can be used by the user. This is an MTP R/W register.

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MFR_USER_CODE (DBh)

Bits	Name	Default	Description
D[7:0]	MFR_USER_CODE	0x01	Returns the MTP configuration code. For example, “0x00” refers to the standard MP8870 (MP8870-0000), while “0x01” refers to the MP8870-0001.

MFR_USER_REVISION (DCh)

Bits	Name	Default	Description
D[7:0]	MFR_USER_ REVISION	0x00	Returns the MTP revision number. The MTP value may be updated, so the revision number is stored here.

MFR_PRODUCT_NAME (DDh)

Bits	Name	Default	Description
D[7:0]	PRODUCT_NAME	0x70	Represents “MP8870”. These bits are read-only.

MFR_SILICON_REV (DEh)

Bits	Name	Default	Description
D[7:0]	PRODUCT_ RELEASED_ REVERSION	0x00	Returns the MP8870’s released version number

MFR_MTP_STATUS (EAh)

Bits	Name	Default	Description
D[7:3]	RESERVED	0	Reserved.
D[2:0]	CURRENT_MTP_ PAGE_INDEX	110	Stores the current MTP page index information. 100: Default page. There are two pages left 110: First page 111: Second page. MTP can no longer be programmed Others: Reversed

Do not change the value of the RESERVED bits, even if they have R/W access.

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APPLICATION INFORMATION

Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply AC current to the converter while maintaining the DC input voltage. Use ceramic capacitors for the best performance. During layout, place the input capacitors as close to VIN as possible.

The capacitance can vary significantly with temperature. Ceramic capacitors with X5R and X7R dielectrics are recommended because they are fairly stable across a wide temperature range and offer very low ESR.

The capacitors must have a ripple current rating that exceeds the converter's maximum input ripple current. Estimate the input ripple current with Equation (7):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (7)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, calculated with Equation (8):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (8)$$

For simplification, choose an input capacitor with an RMS current rating that exceeds half of the maximum load current. The input capacitor value determines the converter's input voltage ripple. If there is an input voltage ripple requirement in the system, select an input capacitor that meets the specification.

Estimate the input voltage ripple with Equation (9):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (9)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, calculated with Equation (10):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (10)$$

Selecting the Output Capacitor

The output capacitor maintains the DC output voltage. Use POSCAP or ceramic capacitors.

Estimate the output voltage ripple with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (11)$$

When using ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes the majority of the output voltage ripple. For simplification, calculate the output voltage ripple with Equation (12):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^{2} \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (12)$$

When using capacitors with a larger ESR (e.g. POSCAP, OSCON), the ESR dominates the switching frequency impedance. In this scenario, the output voltage ripple can be determined by the ESR values. For simplification, the output voltage ripple can be estimated with Equation (13):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (13)$$

Selecting the Inductor

The inductor supplies a constant current to the output load while being driven by the switching input voltage. A larger-value inductor reduces the ripple current and output ripple voltage, but a larger-value inductor also has a larger physical size, higher series resistance, and a lower saturation current.

Design the peak inductor current such that it is below the maximum switch current limit. Calculate the inductance value with Equation (14):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_{L}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (14)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

Choose an inductor that does not saturate under the maximum inductor peak current. The peak inductor current can be calculated with Equation (15):

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2 \times f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (15)$$

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MPS inductors are optimized and tested for use with our complete line of integrated circuits.

Table 2 lists our power inductor recommendations. Select a part number based on your design requirements.

Table 2: Power Inductor Selection

Part Number	Inductor Value	Manufacturer
MPL-AY	0.47µH	MPS
MPL-AY1050-R47	0.47µH	MPS

Visit MonolithicPower.com under Products > Inductors for more information.

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PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best performance, refer to Figure 18 and follow the guidelines below:

1. Place the input MLCC capacitors as close to VIN and PGND as possible.
2. Place the major MLCC capacitors on the same layer as the MP8870.
3. Maximize the VIN and PGND copper plane to minimize the parasitic impedance.
4. Place as many PGND vias as close to PGND as possible to minimize both parasitic impedance and thermal resistance.
5. Place the VCC decoupling capacitor close to the device.
6. Connect AGND and PGND at the point of the VCC capacitor's ground connection.
7. Place the bootstrap (BST) capacitor as close to the BST and SW pins as possible, with a minimum 20mil trace to route the path. In addition, it is recommended for this capacitor to be between 0.1µF and 1µF.
8. Place a via at least 10mm away from the positive side of the first input decoupling capacitor, and close to the IC if it must be placed on the GPIO pad. This prevents the input voltage from being interrupted.

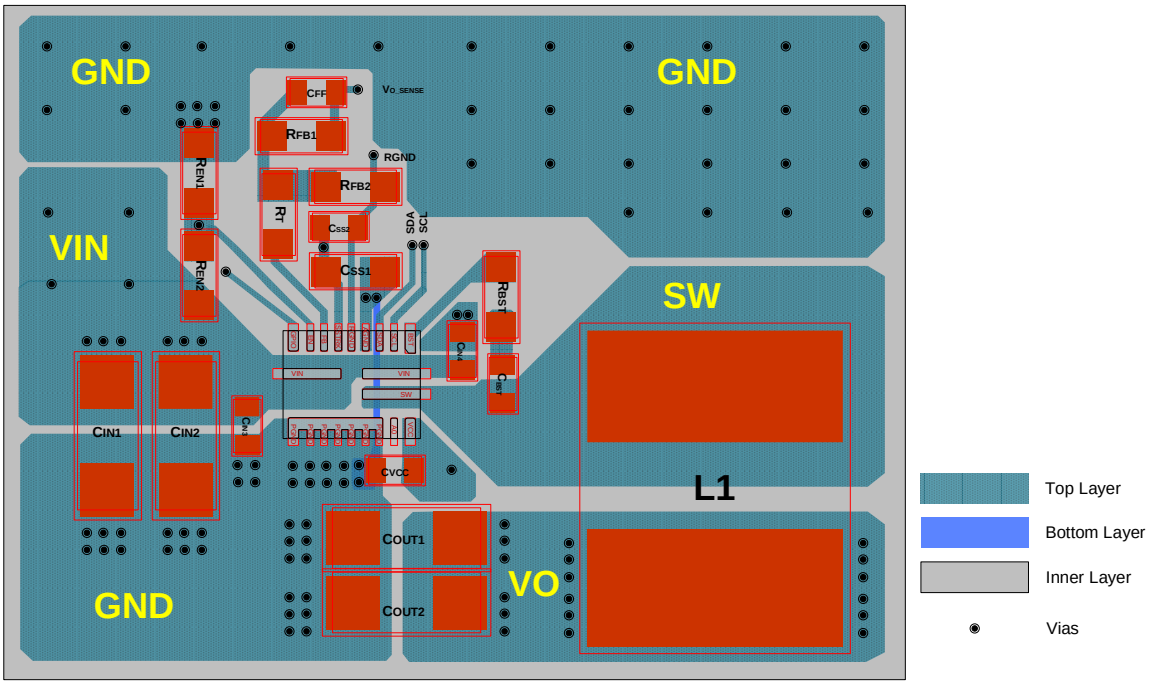


Figure 18: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUIT

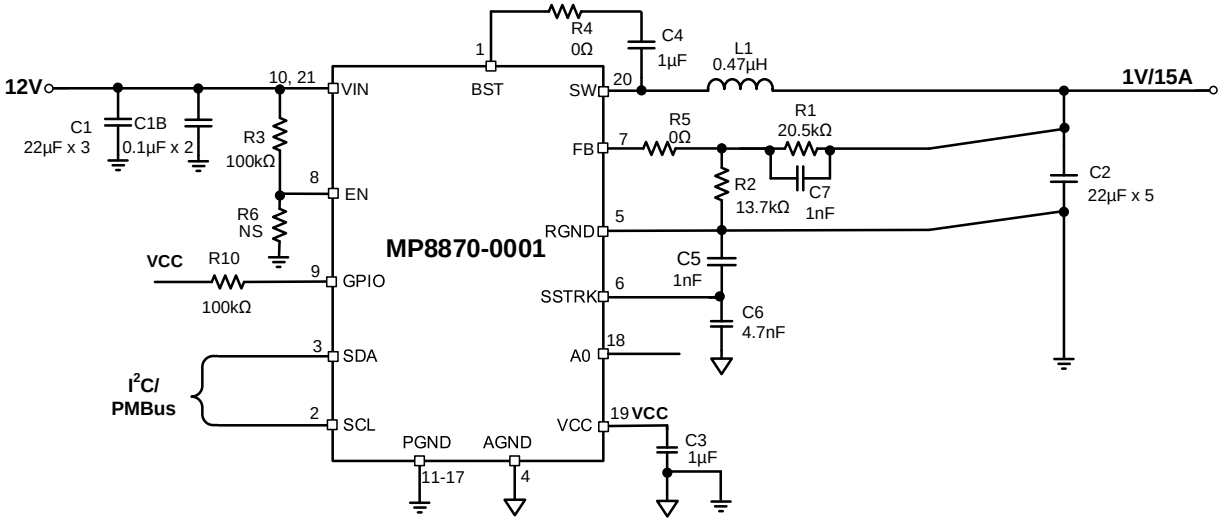


Figure 19: Typical Application Circuit (V_{IN} = 12V, V_{OUT} = 1V, I_{OUT} = 15A)

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APPENDIX

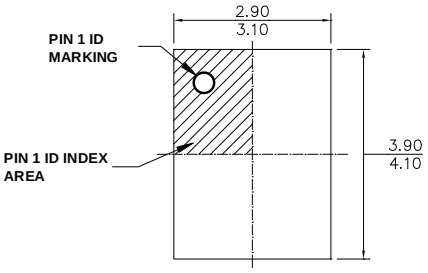
MTP-EFUSE SELECTED TABLE BY STANDARD (MP8870GL-0000)

One-Time Programmable Items	Configuration Value
Reference Voltage	0.40V
Output Voltage Set Mode	External voltage divider mode
Initial On/Off	On
MODE	Auto PFM/PWM mode
Valley Current Limit	16A
Soft-Start Time (0% to 100% V_{OUT})	1ms
Soft Stop when EN Off	Disabled
Switching Frequency	650kHz
GPIO	PG
PG Delay Time	100µs
Protection Mode (OCP, OTP, and UVP)	Hiccup
V_{IN} OV Fault Response	Normal switching
Output OV Fault Response	Output discharge
MTP Configuration Code	0x00
MTP Revision Number	0x00

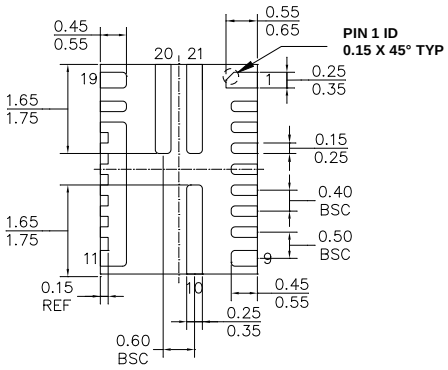
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PACKAGE INFORMATION

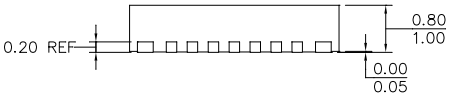
QFN-21 (3mmx4mm)



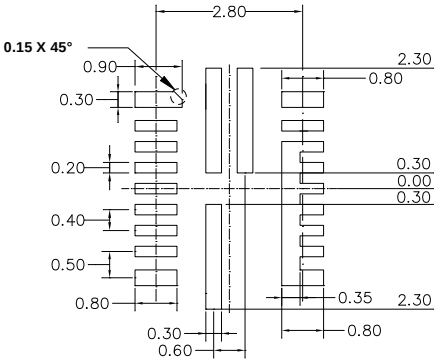
TOP VIEW



BOTTOM VIEW



SIDE VIEW



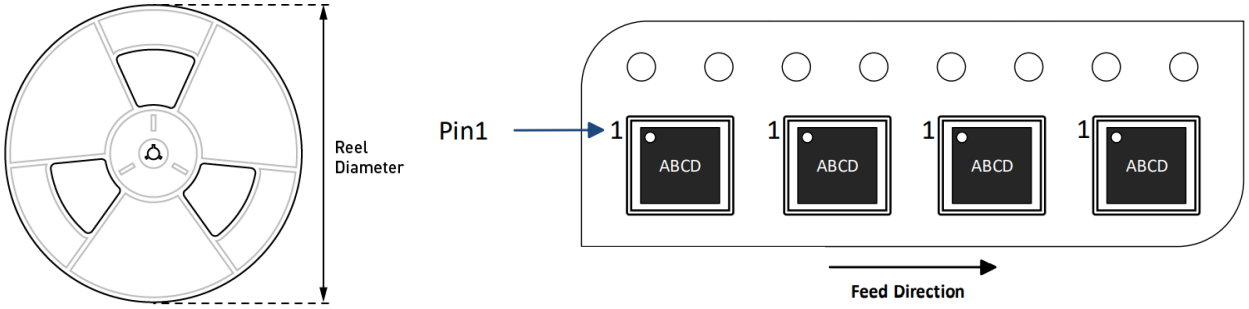
RECOMMENDED LAND PATTERN

NOTE:

1) LAND PATTERN OF PIN1,9,10,11,19,20 AND 21 HAVE THE SAME WIDTH.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-220.
6) DRAWING IS NOT TO SCALE.

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CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP8870GL-0001-Z	QFN-21 (3mmx4mm)	5000	N/A	N/A	13in	12mm	8mm
MP8870GL-xxxx-Z							

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	9/21/2022	Initial Release	-

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