HF300

High-Frequency, Ideal-Clamping Flyback Controller

DESCRIPTION

The HF300 is an intelligent, high-frequency, flyback, ideal clamping controller that is used to replace the passive resistor-capacitor-diode (RCD) snubber in a flyback circuit to clamp the drain-source voltage spike caused by the leakage inductance (L_{LKG}) after the primary main switch turns off. The HF300 is compatible with many flyback operating modes, such as continuous conduction mode (CCM), discontinuous conduction mode (DCM), quasi-resonant (QR) operation, and zero-voltage switching (ZVS). The HF300 can support up to 300kHz flyback applications, and can also improve the efficiency of a flyback circuit.

The HF300 is the ideal substitute for a traditional passive RCD snubber. Replacing this traditional snubber does not bring increase complexity and or system cost.

Full protection features and flexible parameter settings guarantee safe operation of the flyback circuit.

The HF300 is available in a space-saving TSOT23-6 package.

FEATURES

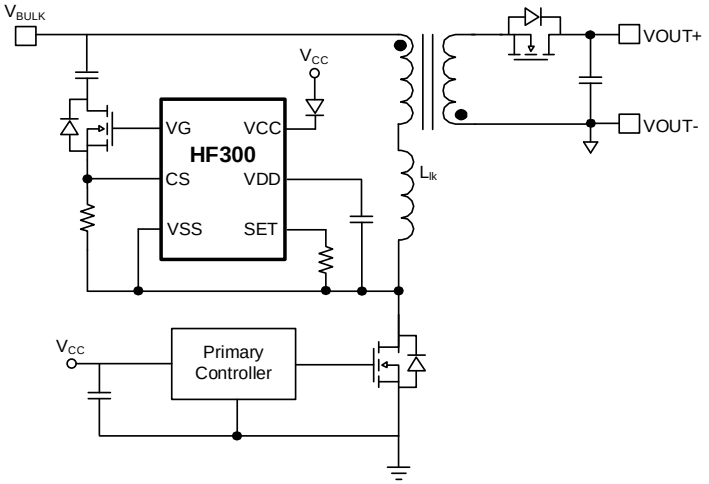
- Active-Clamp Drain-Source Voltage Spike
- Supports Continuous Conduction Mode (CCM), Discontinuous Conduction Mode (DCM), Quasi-Resonant (QR) Operation, and Zero-Voltage Switching (ZVS)
- Supports Up to 300kHz Switching Frequency (f_{SW})
- Easy to Use
- Extremely Low <5mW Standby Power Consumption
- Ultra-Wide VCC Range to Support USB PD Applications
- Intelligent Recycling Leakage Energy and Increased Flyback Converter Efficiency
- Under-Voltage Lockout (UVLO), Over-Current Protection (OCP), and Shoot-Through Prevention
- Available in a TSOT23-6 Package

APPLICATIONS

- USB Power Delivery (PD)/Quick Charge (QC) Chargers and Adapters
- Adapters
- High Power Density Flyback Power Supplies

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TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
HF300GJ	TSOT23-6	*See Below*	1

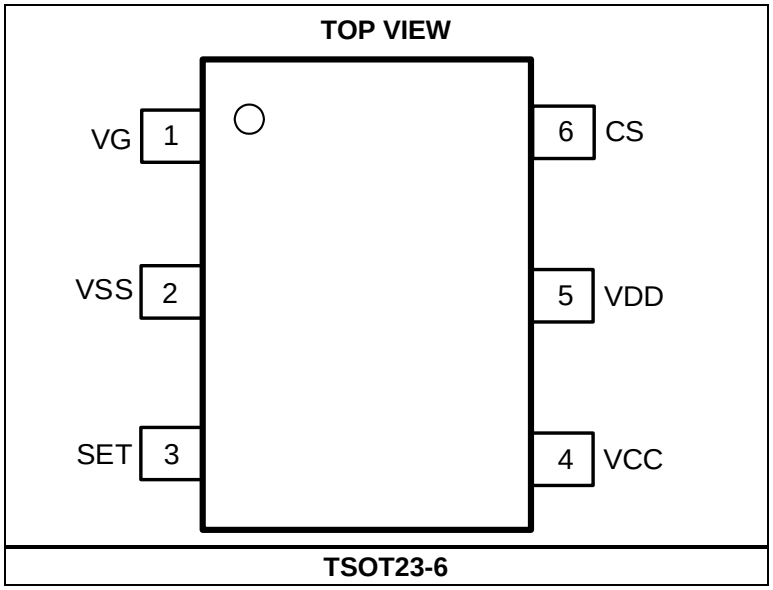
* For Tape & Reel, add suffix -Z (e.g. HF300GJ-Z).

TOP MARKING

BXEY

BXE: Product code of HF300GJ
Y: Year code

PACKAGE REFERENCE



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PIN FUNCTIONS

Pin #	Name	Description
1	VG	**Gate driver output.**
2	VSS	**IC ground.**
3	SET	**Configuration pin.** Connect the SET pin to a resistor.
4	VCC	**IC power supply.**
5	VDD	**Gate driver power regulator output.**
6	CS	**Current sensing.** The CS pin turns VG on and off.

ABSOLUTE MAXIMUM RATINGS (1)

VCC to VSS .....-0.3V to +180V
VDD, VG to VSS .....-0.3V to +12V
CS to VSS .....-3V to +6.5V
SET to VSS.....-0.3V to +6.5V
Continuous power dissipation (T_A = 25°C) (2)
..... 0.56W
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Storage temperature ..... -55°C to +150°C

ESD Ratings

Human body model (HBM) 2000V
Charged-device model (CDM).....2000V

Recommended Operating Conditions (3)

Supply voltage (V_{CC}) .....7.5V to 90V
CS to VSS..... -1 to +0.5V
Maximum junction temperature (T_J).....125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

TSOT23-6 ..... 220 .... 110.. °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on a JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

T_J = -40°C to +125°C, typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Voltage Management (VCC and VDD Pins)						
VCC maximum charging current		V_{DD} = V_{DD_START}, V_{CC} = 10V	20			mA
VDD start-up threshold	V_{DD_START}			5.15	5.4	V
VDD voltage (V_{DD}) under-voltage lockout (UVLO) hysteresis	V_{DD_HYS}			0.5		V
VDD regulation voltage	V_{DD_REG}	V_{CC} = 10V	7.6	8	8.6	V
VCC operating current	I_{OP_VCC}	V_{CC} = 10V, f_{SW} = 150kHz, C_{LOAD} = 1nF			3	mA
VDD quiescent current	I_{Q_VDD}	V_{CC} = 0V, R_{SET} = 45kΩ, V_{DD} = V_{DD_REG}		150	200	µA
VDD shutdown current	I_{SD_VDD}	V_{DD} = V_{DD_UVLO} - 0.1V (5)			80	µA
Gate Driver (VG Pin)						
Driver voltage high level	V_{G_HIGH}	C_{LOAD} = 1nF, V_{DD} = V_{DD_UVLO} + 0.1V (5)	4.6			V
		C_{LOAD} = 1nF, V_{DD} = 8V		8		V
Driver voltage low level	V_{G_LOW}	C_{LOAD} = 1nF, V_{DD} = 8V			0.02	V
Pull-up resistance				3		Ω
Pull-down resistance				1		Ω
Current Sense (CS Pin)						
Gate driver turn-on threshold	V_{CS_ON}		-50		-10	mV
Turn-on delay	t_{ON_DELAY}	C_{LOAD} = 1nF		75		ns
Zero-current detection (ZCD) threshold to turn-off the gate driver	V_{CS_ZCD}			10		mV
ZCD turn-off delay	t_{OFF_DELAY}	C_{LOAD} = 1nF		70		ns
Over-current protection (OCP) and shoot-through prevention threshold	V_{CS_OCP}		0.7	0.8	0.9	V
OCP and shoot-through prevention turn-off delay	t_{OCP_DELAY}	C_{LOAD} = 1nF		60		ns
Leading edge blanking (LEB)	t_{LEB}			230		ns
Time Configuration (SET Pin)						
SET pin voltage	V_{SET}	R_{SET} = 124kΩ		1.23		V
Maximum turn-on time	t_{ON_MAX}	R_{SET} = 24.9kΩ	0.36	0.52	0.68	µs

Note:

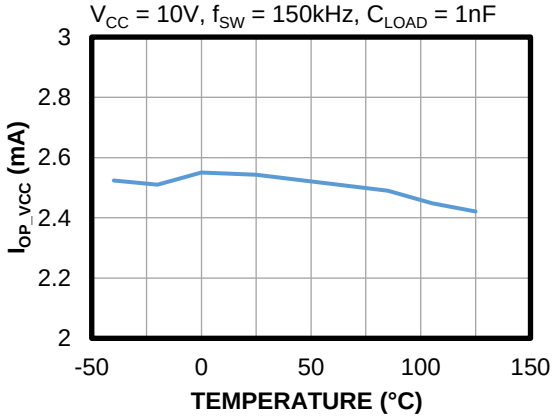
5) V_{DD_UVLO} = V_{DD_START} - V_{DD_HYS}.

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TYPICAL CHARACTERISTICS

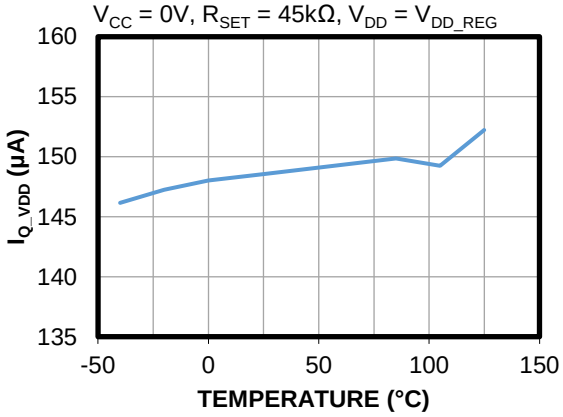
VCC Operating Current vs. Temperature

V_{CC} = 10V, f_{SW} = 150kHz, C_{LOAD} = 1nF

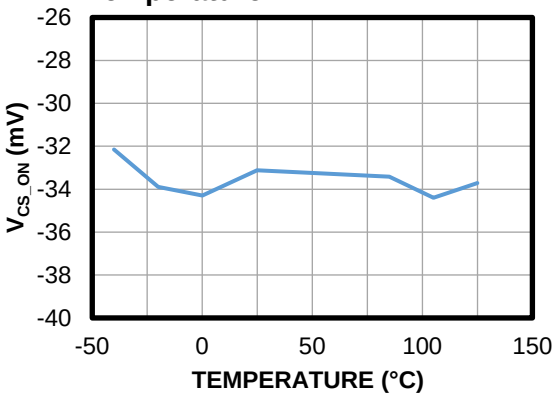


VDD Quiescent Current vs. Temperature

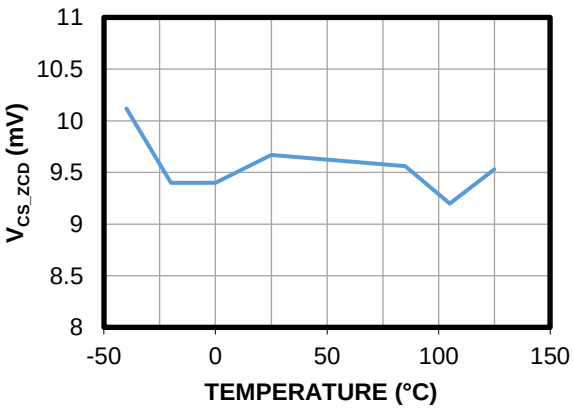
V_{CC} = 0V, R_{SET} = 45kΩ, V_{DD} = V_{DD_REG}



Gate Turn-on Threshold vs. Temperature

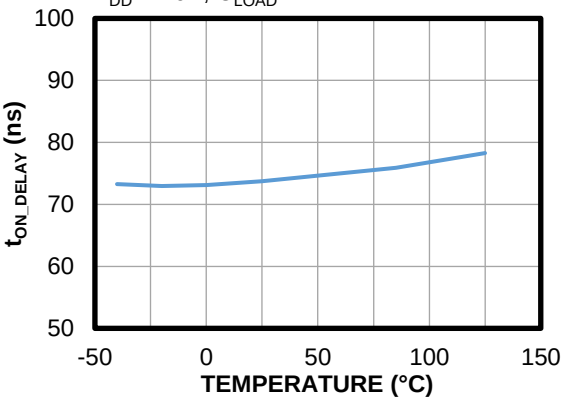


ZCD Threshold vs. Temperature



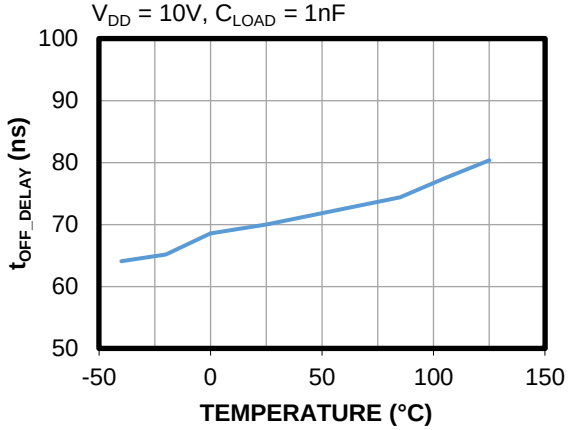
Turn-On Delay vs. Temperature

V_{DD} = 10V, C_{LOAD} = 1nF



ZCD Turn-Off Delay vs. Temperature

V_{DD} = 10V, C_{LOAD} = 1nF

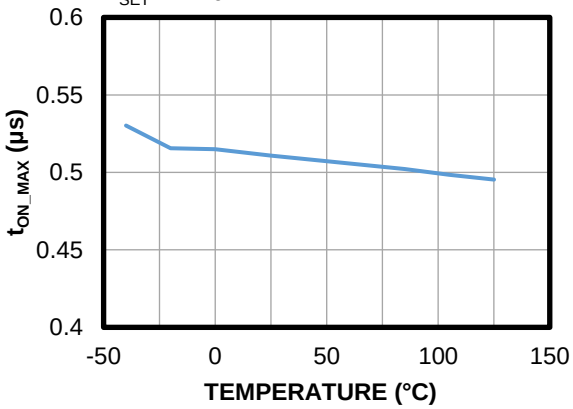


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TYPICAL CHARACTERISTICS *(continued)*

Maximum Turn-on Time vs. Temperature

R_{SET} = 24.9kΩ

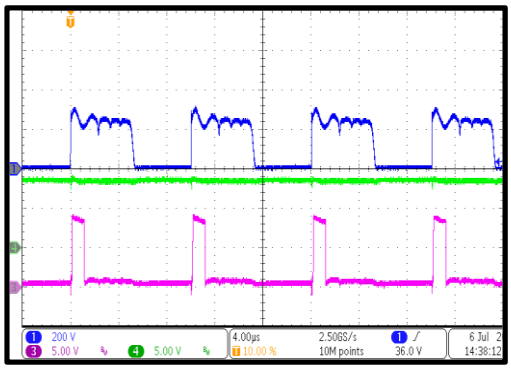


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TYPICAL PERFORMANCE CHARACTERISTICS

65W QR Flyback Application Operation

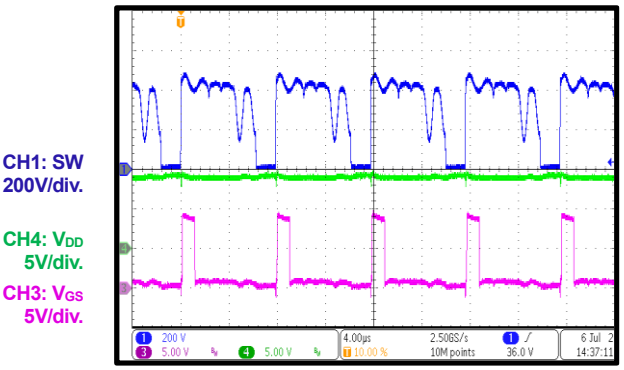
V_{IN} = 110V_{AC}, V_{OUT} = 20V, I_{OUT} = 3.25A



4μs/div.

65W QR Flyback Application Operation

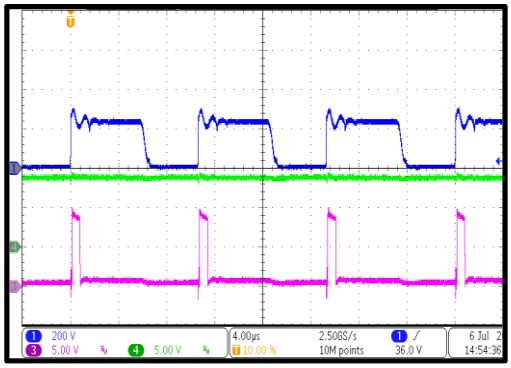
V_{IN} = 220V_{AC}, V_{OUT} = 20V, I_{OUT} = 3.25A



4μs/div.

120W QR Flyback Application Operation

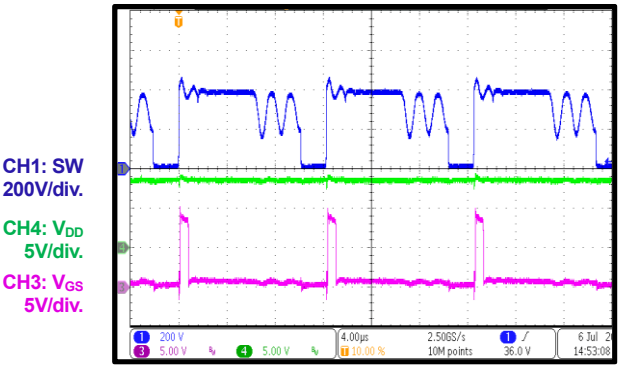
V_{IN} = 110V_{AC}, V_{OUT} = 20V, I_{OUT} = 6A



4μs/div.

120W QR Flyback Application Operation

V_{IN} = 220V_{AC}, V_{OUT} = 20V, I_{OUT} = 6A



4μs/div.

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FUNCTIONAL BLOCK DIAGRAM

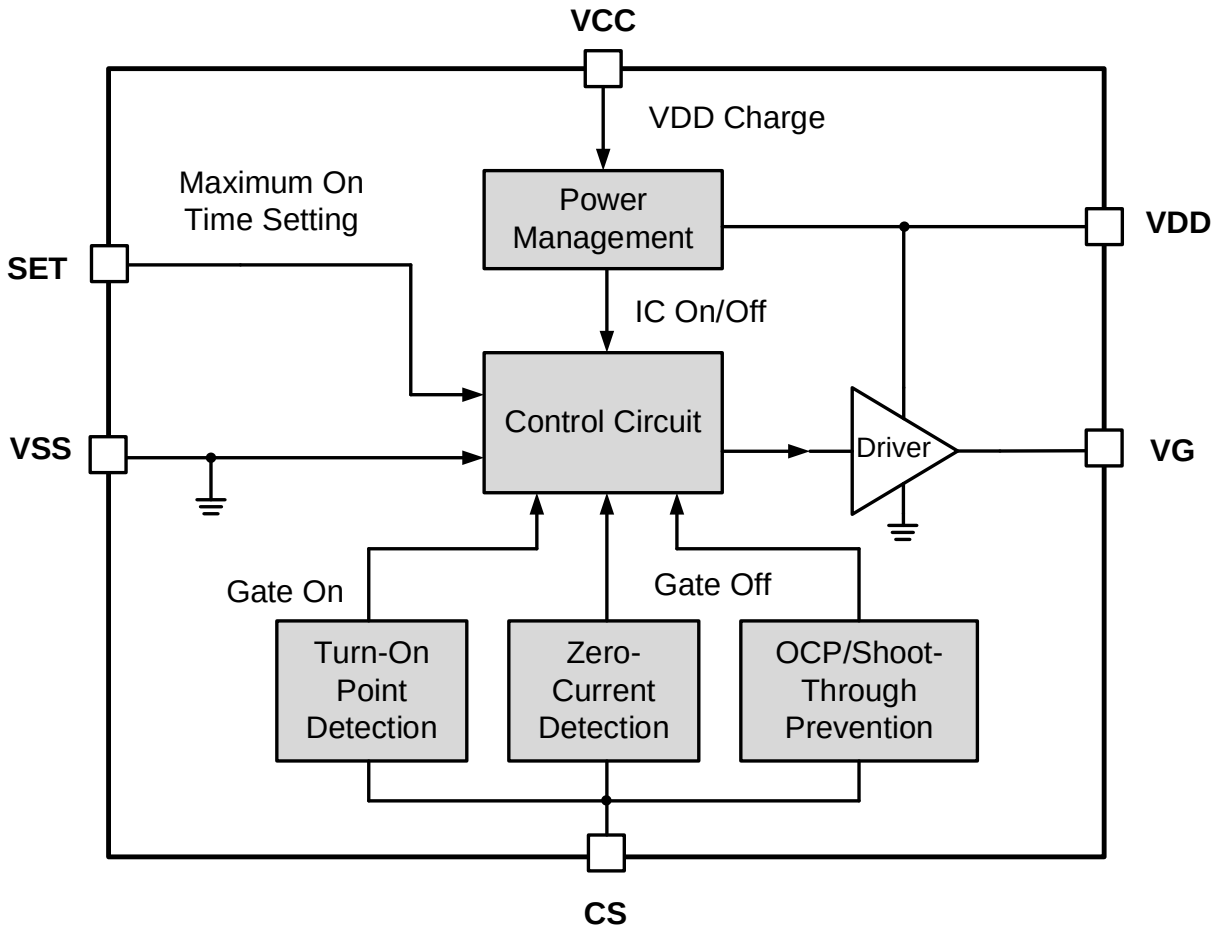


Figure 1: Functional Block Diagram

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OPERATION

The HF300 is an intelligent, high-frequency, flyback ideal clamping controller that recycles and reuses the leakage energy based on charge balance control. The HF300 supports discontinuous conduction mode (DCM), continuous conduction mode (CCM), quasi-resonant (QR) operation, and zero-voltage switching (ZVS) in flyback converters. Figure 2 shows the typical application circuit. Figure 3 and Figure 4 on page 10 show the HF300's key operating waveforms.

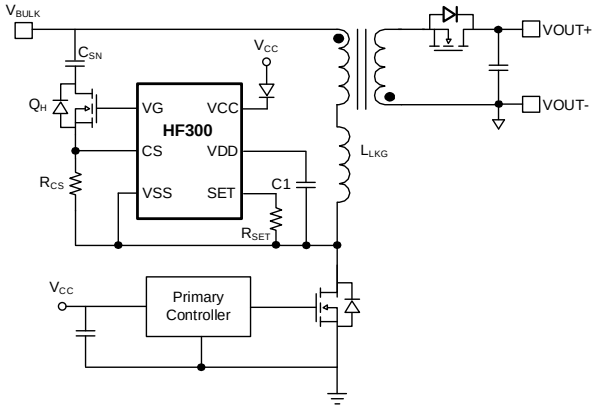


Figure 2: Typical Application Circuit

Power Supply

VCC is the linear regulator's input, and VDD is the regulator's output. VCC charges up the capacitor at VDD through built-in high voltage (HV) current source. VDD supplies power to the HF300, which is regulated at the VDD regulation voltage (V_{DD_REG}).

Start-Up and Under-Voltage Lockout (UVLO)

VCC is connected to the primary controller's VCC supply capacitor through a bootstrap (BST) circuit. When the primary controller activates, the HV current source starts to charge VDD. Once the VDD voltage (V_{DD}) exceeds the VDD start-up threshold (V_{DD_START}), the HF300 exits under-voltage lockout (UVLO) and is enabled. There is a V_{DD} UVLO hysteresis (V_{DD_HYS}) when the HF300 enters UVLO from an enabled state. If V_{DD} drops below (V_{DD_START} - V_{DD_HYS}), the HF300 enters UVLO, and the gate driver voltage (V_{GS}) is pulled down.

Gate Driver

The driver capability is specified in the Electrical Characteristics section on page 4. V_{GS} is clamped internally at the driver voltage high level (V_{G_HIGH}) to guarantee that the external MOSFET can operate safely and reduce the internal power supply's VCC operating current (I_{OP_VCC}) and power loss.

Turn-On Phase

Once the HF300 is enabled, the CS pin senses the current from the leakage inductance (L_{LKG}) after the primary main switch turns off. When the CS pin voltage (V_{CS}) reaches the turn-on threshold (V_{CS_ON}), the gate driver turns on after a turn-on delay (t_{ON_DELAY}) (see Figure 3).

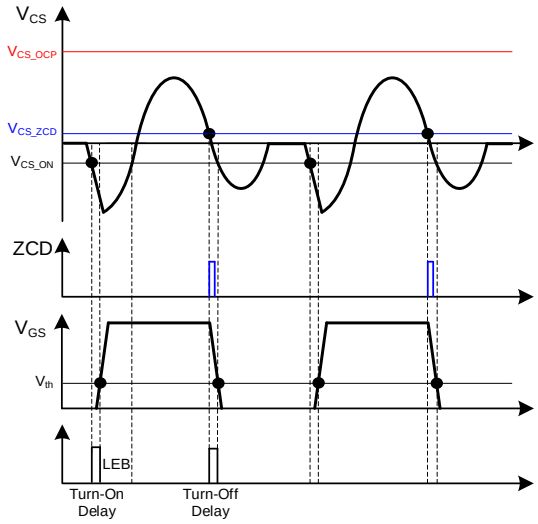


Figure 3: Key Operating Waveforms

Leading Edge Blanking (LEB)

The control circuitry contains a blanking function. To avoid accidental, premature turn-off by the switching noise, an internal leading-edge blanking (LEB) unit is employed after the gate driver turns on (see Figure 3). During the blanking time, the turn-off comparator is disabled, and the gate driver cannot turn off.

Conduction Phase and Turn-Off Phase

During gate driver turn-on, the leakage energy is recycled into the clamping capacitor (C_{SN}), and then sent to the secondary-side output through a transformer when the leakage current (I_{LLKG}) has a negative resonance (i.e. the opposite direction/polarity). When the leakage is fully recycled and delivered again to the output, I_{LLKG} resonates back to 0A, and the gate driver turns off (see Figure 3).

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When V_{CS} reaches the zero-current detection threshold (V_{CS_ZCD}), the gate driver turns off after a turn-off delay (t_{OFF_DELAY}) (see Figure 3 on page 9).

Cycle-by-Cycle Over-Current Protection (OCP)

The HF300's cycle-by-cycle over-current protection (OCP) limits the C_{SN} maximum discharge current. Once V_{CS} reaches the OCP/shoot-through prevention threshold (V_{CS_OCP}), the gate driver turns off after the OCP/shoot-through prevention turn-off delay (t_{OCP_DELAY}) (see Figure 4).

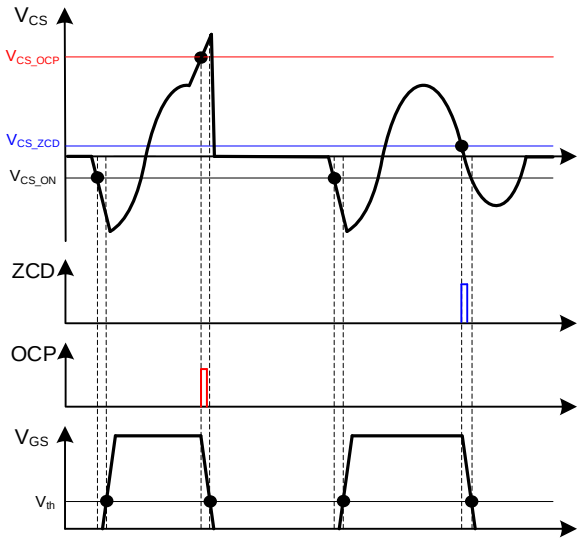


Figure 4: OCP/Shoot-Through Prevention

Configurable Maximum Turn-On Time

To enhance system reliability and support various applications (e.g. applications with a different switching frequency [f_{SW}] or leakage inductance), the HF300 has the flexibility to set up the maximum turn-on time (t_{ON_MAX}) through the SET pin's resistor (R_{SET}).

t_{ON_MAX} (µs) can be configured with Equation (1):

$$t_{ON_MAX} = (0.015 \times R_{SET} + 140) \times 10^{-3} \quad (1)$$

Once the gate driver turn-on time reaches t_{ON_MAX}, V_{GS} is pulled down immediately. The maximum turn-on time ensures that the HF300's gate driver can turn off safely, regardless of whether V_{CS} does not detect V_{CS_ZCD} and V_{CS_OCP}.

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APPLICATION INFORMATION

Selecting the Current-Sense Resistor (C_{CS})

Choose the current-sense resistor (C_{CS}) to be between 100mΩ and 300mΩ. If C_{CS} is too large, the CS voltage (V_{CS}) can easily reach the OCP/shoot-through prevention threshold (V_{CS_OCP}), which can cause an early turn-off. If C_{CS} is too small, reaches the gate driver turn-on threshold (V_{CS_ON}) is not triggered in time. It is recommended that C_{CS} be 200mΩ.

Selecting the Clamping Capacitor (C_{SN})

The clamping capacitor (C_{SN}) should be selected according to the leakage inductance (L_{LKG}). The gate driver turn-on time (about 3/4 of the C_{SN} and L_{lk} resonant period) should be shorter than the primary side's minimum turn-off time ($t_{OFF_MIN_PRI}$). $t_{OFF_MIN_PRI}$ can be calculated with Equation (2):

$$\frac{3}{2}\pi\sqrt{L_{LKG}C_{SN}} \le t_{OFF_MIN_PRI} \quad (2)$$

C_{SN} has a clamping effect on the drain-to-source voltage spike. Select a suitable C_{SN} to adjust the primary switch's voltage spike.

Selecting the External MOSFET

Selecting the external MOSFET is a trade-off between the one resistance ($R_{DS(ON)}$) and cost. For higher efficiency and improved thermal performance, a MOSFET with a smaller $R_{DS(ON)}$ is recommended. However, MOSFETs with a smaller $R_{DS(ON)}$ are typically more expensive. Additionally, MOSFETs with a body diode with a long reverse recovery time are recommended to facilitate the charge balance after the leakage inductance energy is recycled.

Setting the Maximum Turn-on Time

The maximum turn-on time (t_{ON_MAX}) is set by an external resistor on the SET pin. It is recommended that t_{ON_MAX} is slightly longer than the typical gate driver turn-on time. t_{ON_MAX} can be calculated with Equation (3):

$$\frac{3}{2}\pi\sqrt{L_{LKG}C_{SN}} < t_{ON_MAX} \quad (3)$$

Then t_{ON_MAX} can guarantee that the gate driver turns off, even if V_{CS} does not reach the zero-current detection threshold (V_{CS_ZCD}) to prevent shoot-through.

The SET pin voltage (V_{SET}) is susceptible to switching action that can lead to instability. It is recommended to connect a small capacitor across the SET pin's resistor (R_{SET}) to filter out high-frequency noise. R_{SET} and its filter capacitor should be in a small package.

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PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 5 and follow the guidelines below:

1. Place R_{SET} and its filter capacitor as close to the SET pin as possible.
2. Make the power loop and the sensing loop as small as possible.
3. Keep the IC out of the power loop to prevent the sensing loop and power loop from interrupting each other.
4. Place a ceramic decoupling capacitor from VDD to PGND close to the IC for adequate filtering.

Layout Example

Figure 5 shows a double-layer PCB layout example. VSS is the primary main switch's drain side. BUS is the positive side of the BUS capacitor, R1 is the current-sense resistor, and C1 is the clamping capacitor.

1. Place R_{SET} and its filter capacitor (R3 and C3) as close to the SET pin as possible. In this example, R3 and C3 are in a 0402 package.
2. Minimize the power loop (VSS to R1 to M1 to C1 to BUS) and the sensing loop (CS to R1, and the VSS pin to the VSS side).
3. Separate the sensing loop from the power loop.
4. Place the VDD decoupling capacitor (C2) next to the VDD pin.
5. The VCC pin is connected to the primary controller's VCC through a diode (D1).

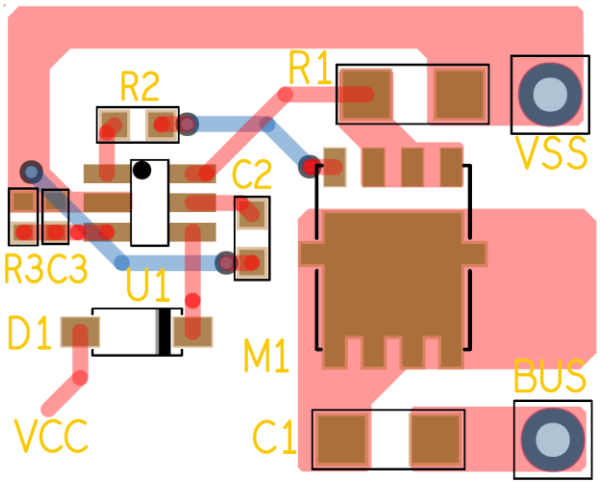


Figure 5: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUIT

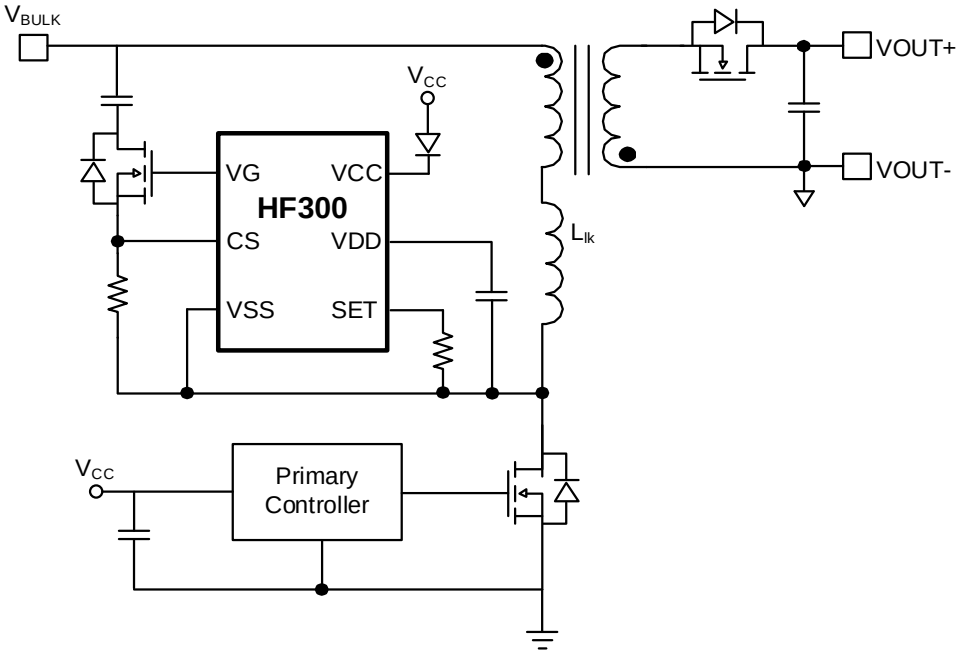
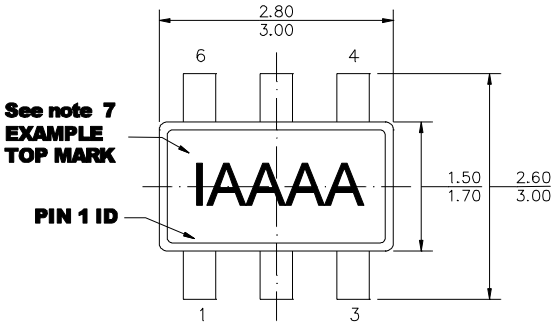


Figure 6: Typical Application Circuit

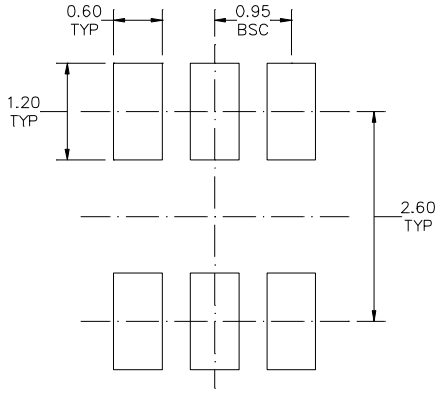
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PACKAGE INFORMATION

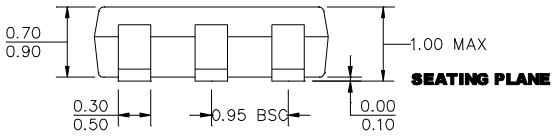
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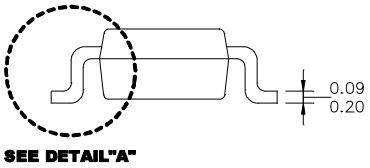
TOP VIEW



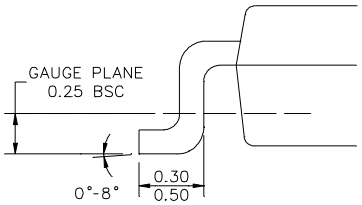
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



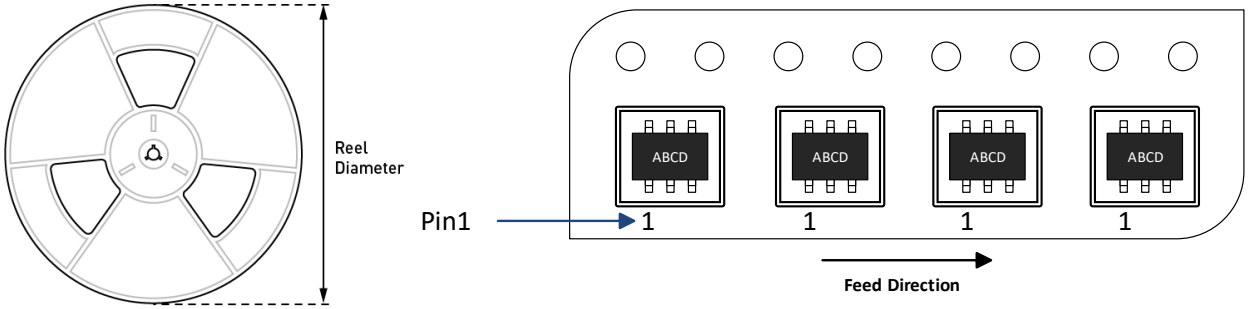
DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY(BOTTOM OF LEADS AFTER FORMING) SHALL BE0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO193, VARIATION AB.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK).

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CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
HF300GJ-Z	TSOT23-6	3000	N/A	N/A	7in	8mm	4mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	3/18/2024	Initial Release	-

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