MPM3551

36V, 3A, Low Quiescent Current, Synchronous Step-Down Module, AEC-Q100 Qualified

DESCRIPTION

The MPM3551 is an easy-to-use, fully integrated, synchronous step-down power module with a built-in inductor and power MOSFETs. It can achieve up to 3A of continuous output current (I_{OUT}), with excellent load and line regulation.

The wide 3.3V to 36V input voltage (V_{IN}) range and 42V load dump tolerance accommodates a variety of step-down applications in automotive input environments. A 1µA shutdown mode quiescent current (I_Q) allows the device to be used in battery-powered applications.

High power conversion efficiency across a wide load range is achieved by scaling down the switching frequency (f_{SW}) under light-load conditions to reduce the switching and gate driving losses.

An open-drain power good (PG) signal indicates whether the output is within 94.5% to 105.5% of its nominal voltage.

Frequency foldback helps prevent inductor current (I_L) runaway during start-up. Thermal shutdown provides reliable, fault-tolerant operation. High duty cycle and low-dropout (LDO) mode are provided for automotive cold-crank conditions.

The MPM3551 is ideal for a wide range of applications with constrained PCB areas. It is available in a QFN-20 (4mmx6mm) package, and is AEC-Q100 qualified.

FEATURES

- Designed for Automotive Applications:
  - 42V Load Dump Tolerance
  - Supports 3.1V Cold Crank Conditions
  - Low-Dropout (LDO) Mode
  - Up to 3A of Continuous I_{OUT}
  - Continuous Operation Up to 36V
  - -40°C to +150°C Operating T_J
- Increases Battery Life:
  - 1µA Shutdown Supply Current (I_{SD})
  - 20µA Sleep Mode (I_Q)
  - AAM Mode

FEATURES *(continued)*

- High Performance for Improved Thermals:
  - Integrated 70mΩ High-Side MOSFET and 50mΩ Low-Side MOSFET
  - 65ns Minimum On Time (t_{ON_MIN}) and 50ns Minimum Off Time (t_{OFF_MIN})
- Optimized for EMC and EMI:
  - Frequency Spread Spectrum (FSS) Modulation
  - Symmetric VIN Pinout
  - Integrated 1µH Power Inductor
  - CISPR25 Class 5 Compliant
  - 2.2MHz Fixed Switching Frequency (f_{SW})
  - MeshConnect™ Flip-Chip Package
- Additional Features:
  - Power Good (PG) Output
  - Adjustable Output from 0.8V
  - Fixed Output Options (1): 1V, 1.8V, 2.5V, 3V, 3.3V, 3.8V, or 5V
  - Over-Current Protection (OCP) in Hiccup Mode
  - Available in a QFN-20 (4mmx6mm) Package with Wettable Flanks
  - Available in AEC-Q100 Grade 1
- Functional Safety System Design Capability:
  - Documents Available for MPSafe™ QM System Design

MPSafe™ QM

APPLICATIONS

- Automotive Infotainment
- Automotive Clusters
- Advanced Driver-Assistance Systems (ADAS)
- Industrial Power Systems

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Note:

1) See the Ordering Information section on page 3 for details regarding the fixed-output versions. Additional output voltages may be available. Contact MPS for details.

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TYPICAL APPLICATION

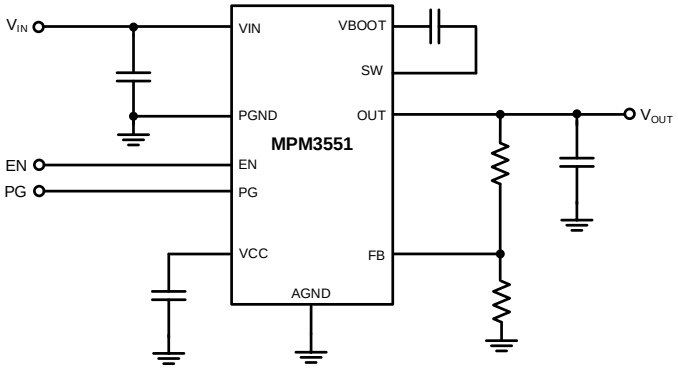
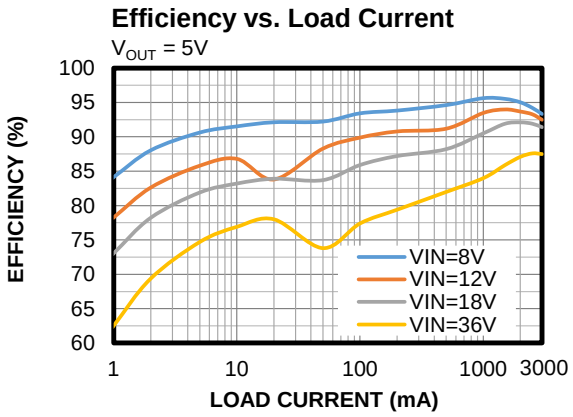


Figure 1: Typical Application (Adjustable Output)



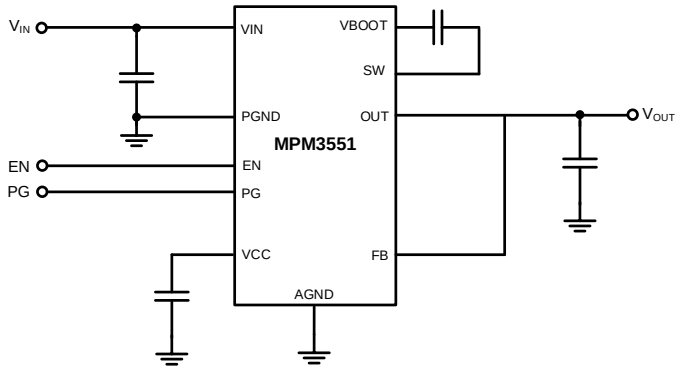


Figure 2: Typical Application (Fixed Output)

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ORDERING INFORMATION

Part Number [2]*	Package	Top Marking	MSL Rating**
MPM3551GQWE***	QFN-20 (4mmx6mm)	*See Below*	3
MPM3551GQWE-AEC1***	QFN-20 (4mmx6mm)	*See Below*	3

* For Tape & Reel, add suffix -Z (e.g. MPM3551GQWE-AEC1-Z).
**Moisture Sensitivity Level Rating
***Wettable flank

Note:

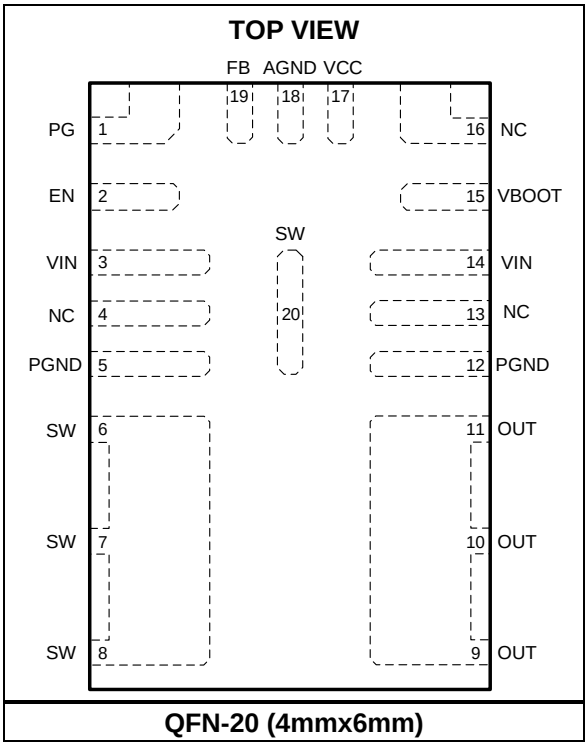
2) Additional output voltages may be available. Contact MPS for details.

TOP MARKING

MPSYWW
MP3551
LLLLLL
ME

MPS: MPS prefix
Y: Year code
WW: Week code
MP3551: Part number
LLLLLL: Lot number
M: Module
E: Wettable flank

PACKAGE REFERENCE



QFN-20 (4mmx6mm)

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PIN FUNCTIONS

Pin #	Name	Description
1	PG	**Power good indicator.** The PG pin is an open-drain output. If used, connect PG to a pull-up resistor set logic high. If the output voltage (V_{OUT}) is within 94.5% to 105.5% of the nominal voltage, then PG is pulled high. If V_{OUT} exceeds 107% or drops below 93% of the nominal voltage, then PG goes low. Float this pin if not used.
2	EN	**Enable.** Pull the EN pin above the specified threshold (about 1.02V) to turn the chip on; pull EN below the specified threshold (about 0.85V) to turn it off. To avoid uncertain status, do not float EN since there is no internal pull-up or pull-down resistor at the pin.
3, 14	VIN	**Input supply.** The VIN pins supply power to the internal regulator and the power MOSFET connected to the SW pin. The two VIN pins are connected internally. Place a decoupling capacitor connected to ground as close to each VIN pin as possible to minimize switching spikes.
4, 13, 16	NC	**Not connected.** These pins do not have an internal connection and can either be floated or used for routing other signals.
5, 12	PGND	**Power ground.** Connect the PGND pin with large copper areas to the negative terminals of the input capacitors.
6, 7, 8, 20	SW	**Switch output.** The SW pin is the source of the high-side MOSFET (HS-FET) and the drain of the low-side MOSFET (LS-FET). Connect SW to the power inductor internally.
9, 10, 11	OUT	**Power output.** Connect the OUT pin to the load. An output capacitor (C_{OUT}) is required to reduce the voltage ripple.
15	VBOOT	**Bootstrap.** The VBOOT pin is the positive power supply for the HS-FET driver connected to SW. Connect a bypass capacitor between the BOOT and SW pins.
17	VCC	**Bias supply.** The VCC pin is the output of the internal regulator that supplies power to the internal control circuit and gate drivers. Place a minimum 1µF decoupling capacitor between VCC and ground. The capacitor should be placed as close as possible to VCC.
18	AGND	**Analog ground.** The AGND pin is the ground reference for analog signals such as the FB pin. Connect AGND to regular ground.
19	FB	**Feedback.** For the fixed-output versions, connect the FB pin directly to V_{OUT}. For the adjustable-output version, connect FB to the middle point of the external feedback divider between the output and AGND to set V_{OUT}.

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ABSOLUTE MAXIMUM RATINGS (3)

VIN, EN……..42V for automotive load dump (4)
VIN, EN…….....-0.3V to +40V
SW……..-0.3V to V_{IN_MAX} + 0.3V
VBOOT…… ..... V_{SW} + 5.5V
FREQ, VCC……..….5.5V
All other pins…… .....-0.3V to +6V
Continuous power dissipation (T_A = 25°C) (5)
QFN-20 (4mmx6mm)…… 3.6W (9)
Operating junction temperature (T_J).....150°C
Lead temperature…….....260°C
Storage temperature……...-65°C to +150°C

ESD Ratings

Human body model (HBM)……..……..Class 2 (6)
Charged-device model (CDM).....Class C2b (7)

Recommended Operating Conditions

Supply voltage (V_{IN})…….3.3V to 36V
Minimum V_{IN} for start-up…….3.9V
Minimum V_{IN} after start-up……..…….....3.1V
Output voltage (V_{OUT})…….....0.8V to 0.95 x V_{IN}
Operating junction temp (T_J) ……..
……-40°C to +150°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-20 (4mmx6mm)
JESD51-7…..…..…….....46.2…....6.1...°C/W (8)
EVM3551-QW-00A…...…34.8.....°C/W (9)

Ψ_{JT}

JESD51-7…..…..……..…….....7.1.....°C/W (8)
EVM3551-QW-00A…….…..…....8.9....°C/W (9)

Notes:

3) Absolute maximum ratings are rated under room temperature, unless otherwise noted. Exceeding these ratings may damage the device.
4) Refer to ISO16750.
5) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the device to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
6) Per AEC-Q100-002.
7) Per AEC-Q100-011.
8) Measured on a JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application. The θ_{JC} value shows the thermal resistance from junction-to-case bottom, and the Ψ_{JT} value shows the characterization parameter from junction-to-case top.
9) Measured on the MPS MPM3551-AEC1 standard EVB: 8.3cmx8.3cm, 2oz copper thickness, 4-layer PCB. The Ψ_{JT} value shows the characterization parameter from junction-to-case top.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Supply						
V_{IN} under-voltage lockout (UVLO) rising threshold	$V_{IN_UVLO_RISING}$		3.4	3.65	3.9	V
V_{IN} UVLO falling threshold	$V_{IN_UVLO_FALLING}$		2.6	2.9	3.1	V
V_{IN} UVLO hysteresis	$V_{IN_UVLO_HYS}$			750		mV
VIN quiescent current	I_Q	V_{FB} = 0.85V, no load, T_J = 25°C		20	28	µA
		V_{FB} = 0.85V, no load, T_J = -40°C to +125°C (10)			34	µA
		V_{FB} = 0.85V, no load, T_J = -40°C to +150°C			80	µA
VIN quiescent switching current (10)	$I_{Q_SWITCHING}$	Switching, R_{FB1} = 1MΩ, R_{FB2} = 191kΩ, no load		25		µA
VIN shutdown current	I_{SHDN}	V_{EN} = 0V		1	10	µA
V_{IN} over-voltage protection (OVP) rising threshold	$V_{IN_OVP_RISING}$		35.5	37.5	40	V
V_{IN} OVP falling threshold	$V_{IN_OVP_FALLING}$		34.5	36.5	39	V
V_{IN} OVP hysteresis	$V_{IN_OVP_HYS}$			1		V
Frequency, Switches, and Inductor						
Switching frequency without frequency spread spectrum (FSS)	f_{SW}		1980	2200	2420	kHz
FSS span				±10		%
FSS modulation frequency				15		kHz
Minimum on time (10)	t_{ON_MIN}			65	80	ns
Minimum off time (10)	t_{OFF_MIN}			50	70	ns
Maximum duty cycle	D_{MAX}		98	99.5		%
Switch leakage current	I_{SW_LKG}	V_{EN} = 0V, V_{SW} = V_{BOOT} = 0V or V_{IN} (T_J = 25°C)		0.01	1	µA
		V_{EN} = 0V, V_{SW} = V_{BOOT} = 0V or V_{IN} (T_J = -40°C to +150°C)		0.01	8	µA
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)_HS}$	V_{BOOT} - V_{SW} = 5V		70	130	mΩ
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)_LS}$	V_{CC} = 5V		50	90	mΩ
Integrated inductance (11)	L		0.8	1	1.2	µH
DC resistance of integrated inductor (11)	R_L			30	36	mΩ
Output and Regulation						
FB voltage	V_{FB}	Adjustable-output version	0.790	0.8	0.810	V
FB input current	I_{FB}	Adjustable-output version		0	100	nA

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Output voltage (V_{OUT}) discharge current	$I_{DISCHARGE}$	V_{EN} = 0V, V_{OUT} = 0.3V	2	4		mA
VBOOT						
VBOOT - SW refresh rising threshold	V_{BOOT_RISING}			2.5	2.9	V
VBOOT - SW refresh falling threshold	$V_{BOOT_FALLING}$			2.3	2.7	V
VBOOT - SW refresh hysteresis	V_{BOOT_HYS}			0.2		V
Enable (EN)						
EN rising threshold	V_{EN_RISING}		0.97	1.02	1.07	V
EN falling threshold	$V_{EN_FALLING}$		0.8	0.85	0.9	V
EN threshold hysteresis	V_{EN_HYS}			170		mV
Soft Start (SS) and VCC						
Soft-start time	t_{SS}	EN high to SS finishes	3	5	7	ms
VCC voltage	V_{CC}	I_{VCC} = 0	4.7	5	5.3	V
VCC regulation		I_{VCC} = 30mA		1		%
VCC current limit	I_{LIMIT_VCC}	V_{CC} = 4V	50	70		mA
Power Good (PG)						
PG rising threshold (V_{FB} / V_{REF})	$V_{PG_VTH_RISING}$	V_{OUT} rising	93	94.5	96	%
		V_{OUT} falling	104	105.5	107	
PG falling threshold (V_{FB} / V_{REF})	$V_{PG_VTH_FALLING}$	V_{OUT} falling	91.5	93	94.5	
		V_{OUT} rising	105.5	107	108.5	
PG threshold hysteresis (V_{FB} / V_{REF})	$V_{PG_VTH_HYS}$			1.5		
PG low output voltage	V_{PG_LOW}	I_{SINK} = 1mA		0.1	0.3	V
PG rising deglitch time	t_{PG_R}			70		µs
PG falling deglitch time	t_{PG_F}			60		µs
Protections						
High-side (HS) peak current limit	I_{LIMIT_HS}	Duty cycle = 30%	4.3	5.8	7.3	A
Low-side (LS) valley current limit	I_{LIMIT_LS}		3	4.4	5.7	A
Zero-current detection (ZCD) current	I_{ZCD}		-0.05	0.05	+0.15	A
Thermal shutdown (10)	T_{SD}		160	175	185	°C
Thermal shutdown hysteresis (10)	T_{SD_HYS}			20		°C

Notes:

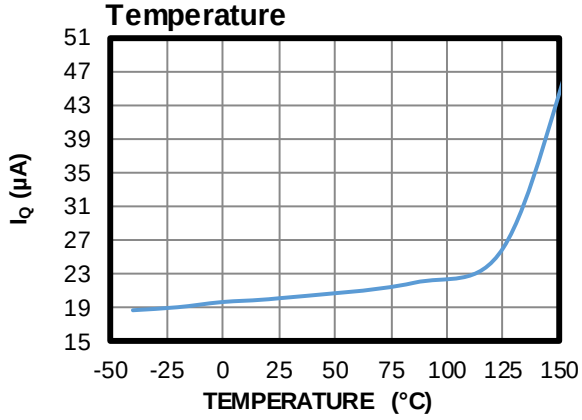
10) Not tested in production. Guaranteed by design and characterization.
11) Not tested in production. Guaranteed by manufacturer.

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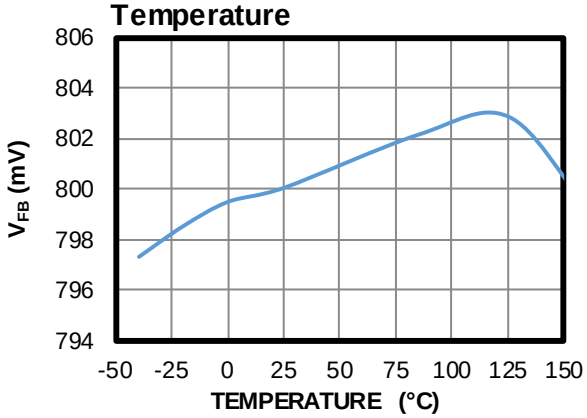
TYPICAL CHARACTERISTICS

V_{IN} = 12V, unless otherwise noted.

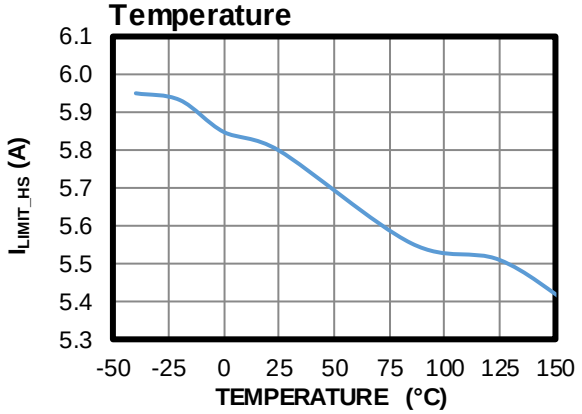
Quiescent Current vs. Temperature



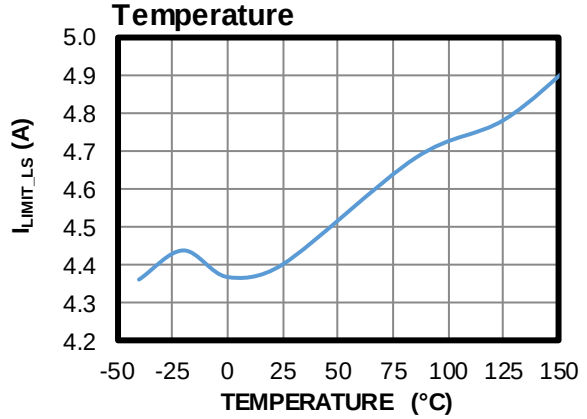
Feedback Voltage vs. Temperature



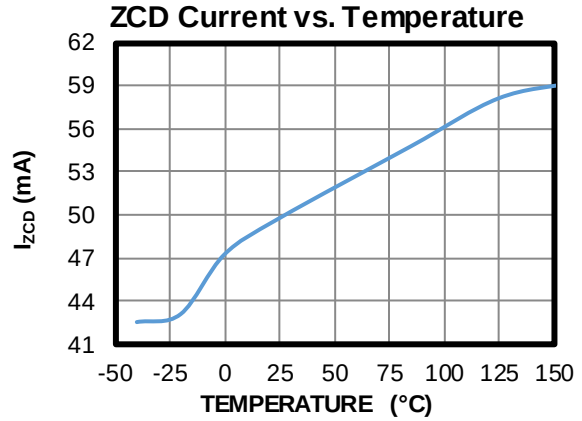
HS Peak Current Limit vs. Temperature



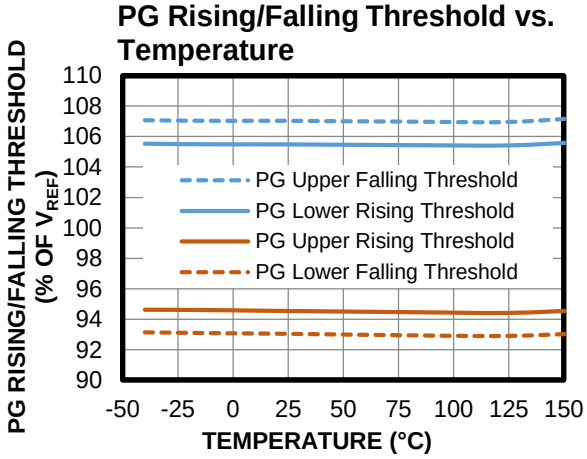
LS Valley Current Limit vs. Temperature



ZCD Current vs. Temperature



PG Rising/Falling Threshold vs. Temperature

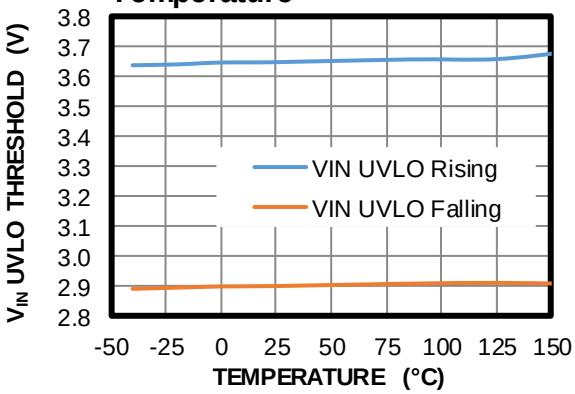


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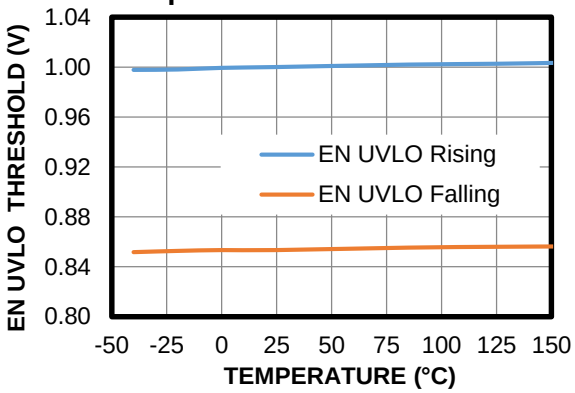
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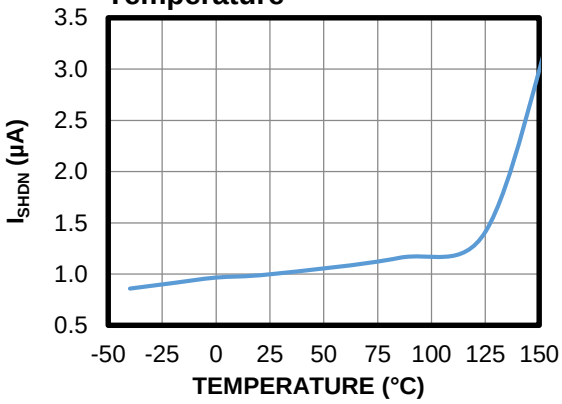
V_{IN} UVLO Threshold vs. Temperature



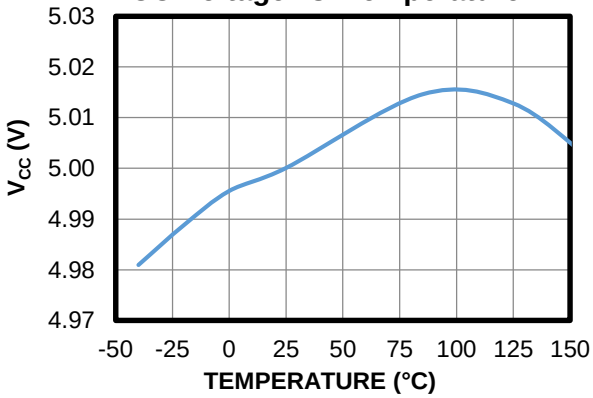
EN UVLO Threshold vs. Temperature



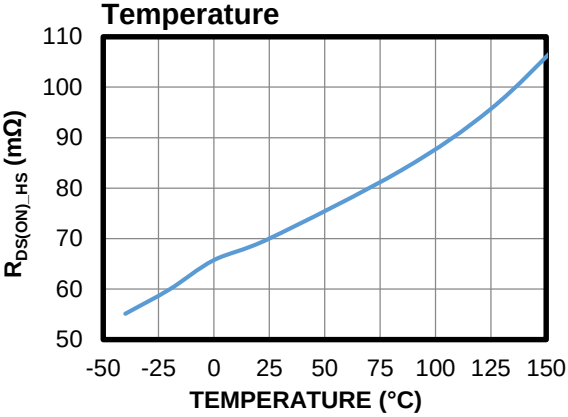
VIN Shutdown Current vs. Temperature



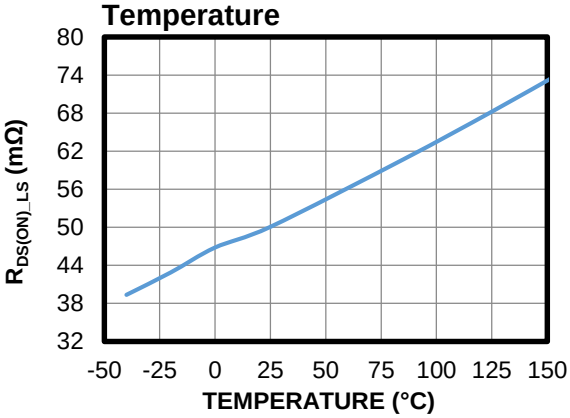
VCC Voltage vs. Temperature



HS-FET On Resistance vs. Temperature



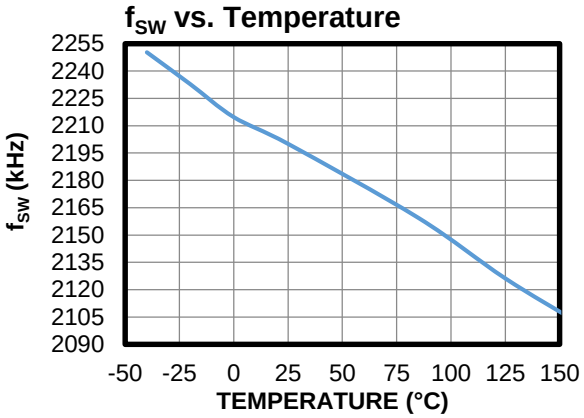
LS-FET On Resistance vs. Temperature



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TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, unless otherwise noted.



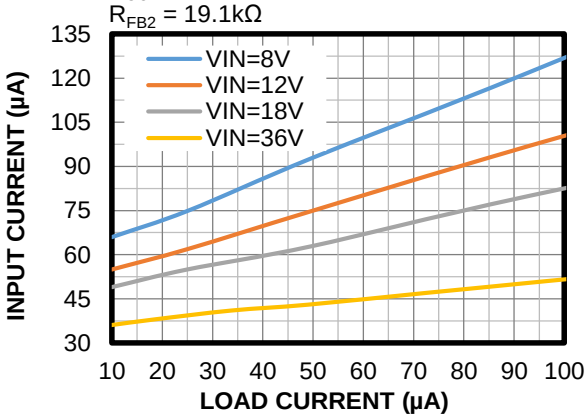
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TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 1µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

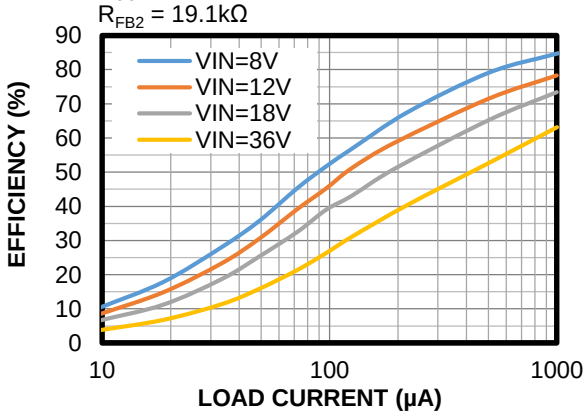
Input Current vs. Load Current

V_{OUT} = 5V, R_{FB1} = 100kΩ, R_{FB2} = 19.1kΩ



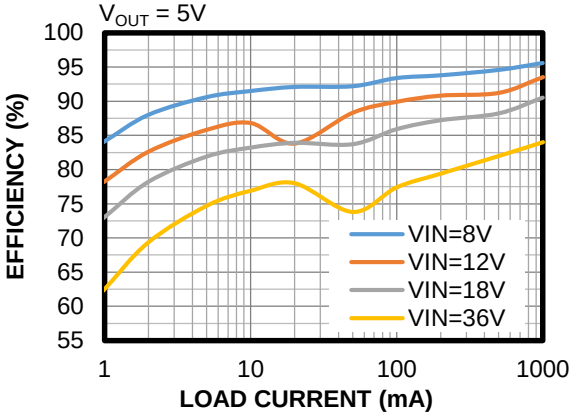
Efficiency vs. Load Current

V_{OUT} = 5V, R_{FB1} = 100kΩ, R_{FB2} = 19.1kΩ



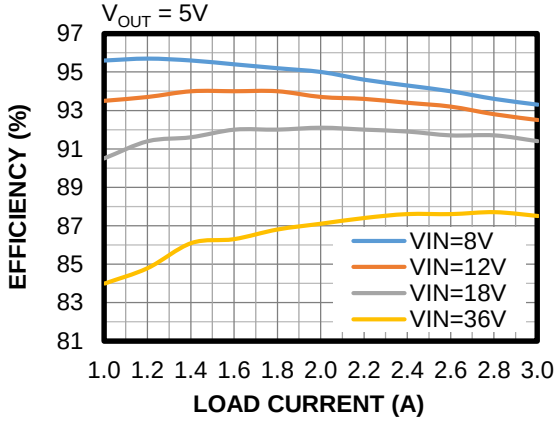
Efficiency vs. Load Current

V_{OUT} = 5V



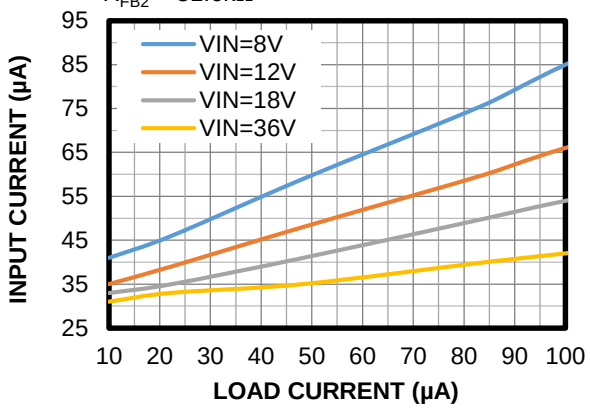
Efficiency vs. Load Current

V_{OUT} = 5V



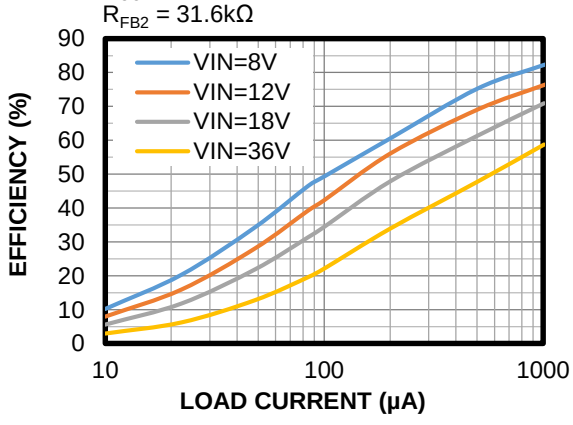
Input Current vs. Load Current

V_{OUT} = 3.3V, R_{FB1} = 100kΩ, R_{FB2} = 31.6kΩ



Efficiency vs. Load Current

V_{OUT} = 3.3V, R_{FB1} = 100kΩ, R_{FB2} = 31.6kΩ

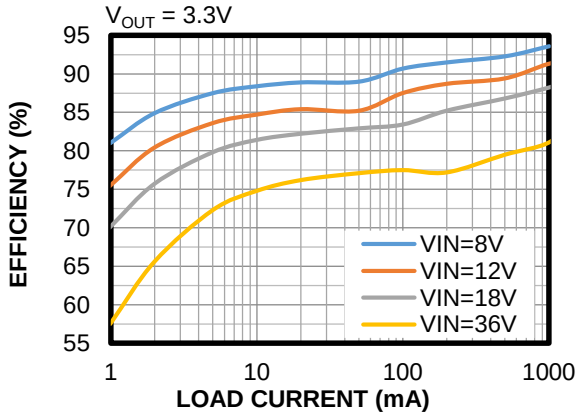


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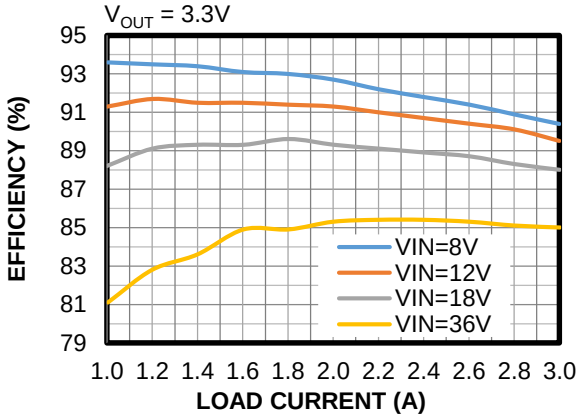
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 1µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

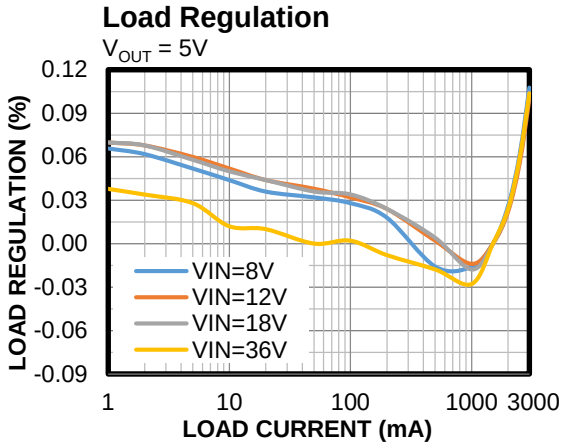
Efficiency vs. Load Current



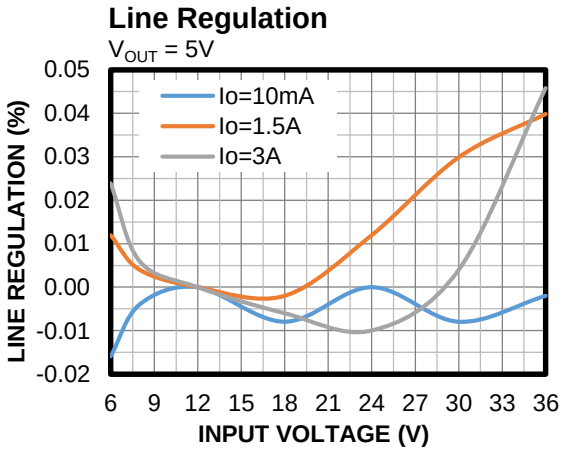
Efficiency vs. Load Current



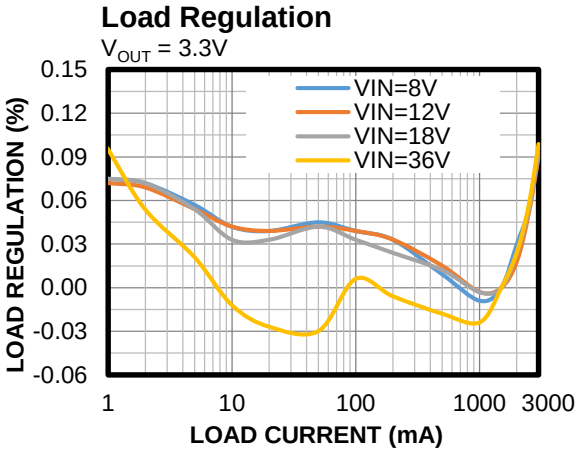
Load Regulation



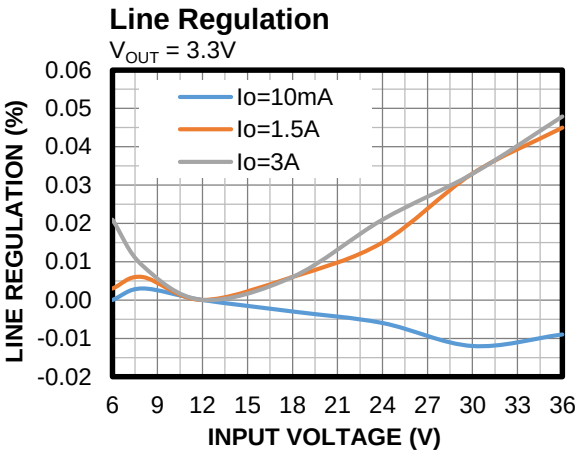
Line Regulation



Load Regulation



Line Regulation



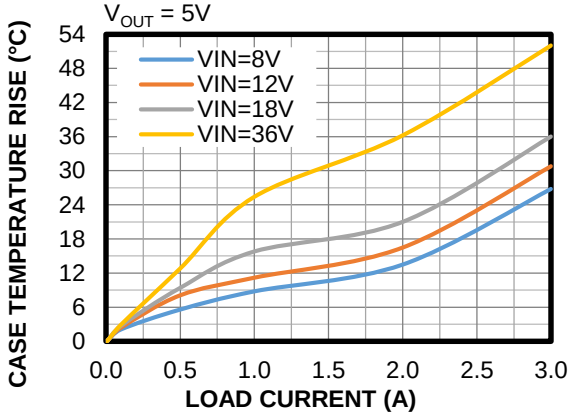
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 1µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

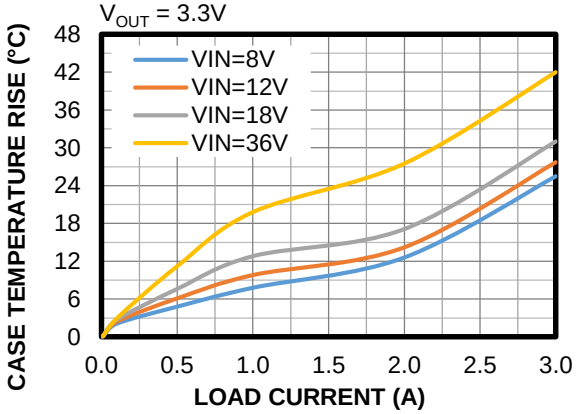
Case Temperature Rise

V_{OUT} = 5V



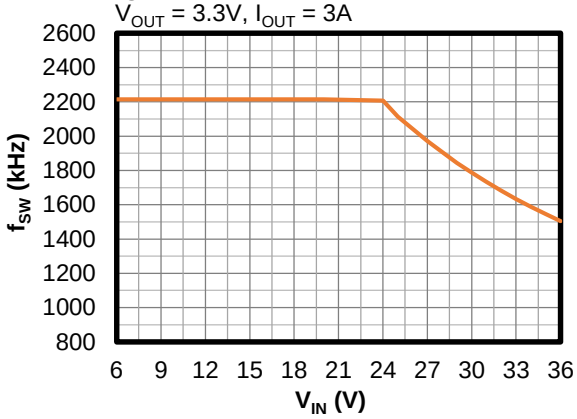
Case Temperature Rise

V_{OUT} = 3.3V



f_{SW} vs. V_{IN}

V_{OUT} = 3.3V, I_{OUT} = 3A



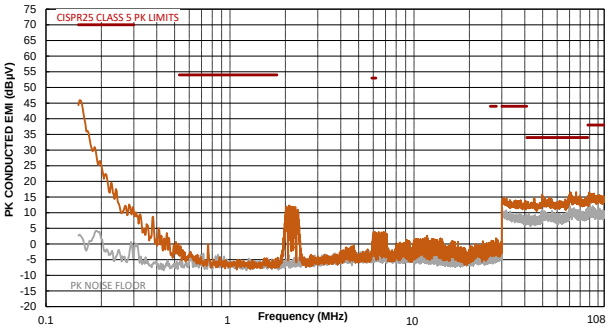
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 1µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted. (12)

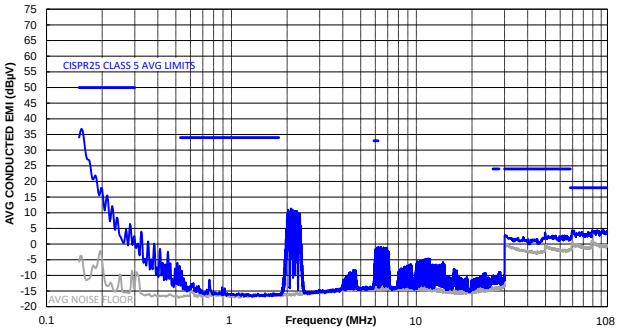
CISPR25 Class 5 Peak Conducted Emissions

150kHz to 108MHz



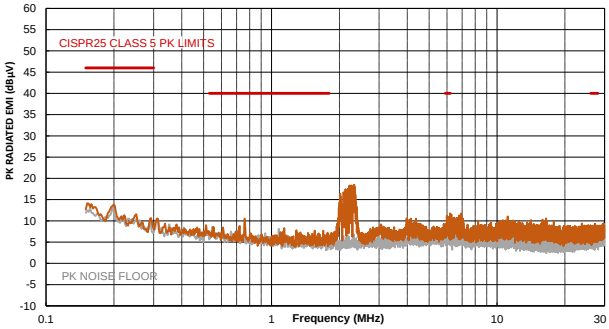
CISPR25 Class 5 Average Conducted Emissions

150kHz to 108MHz



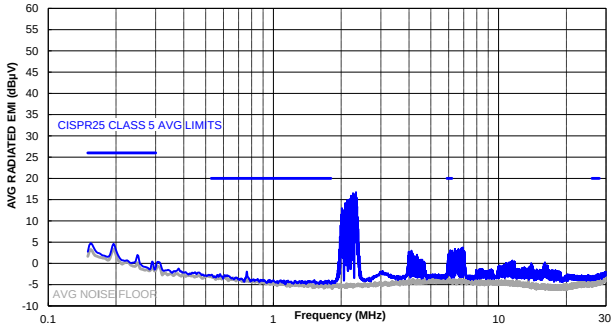
CISPR25 Class 5 Peak Radiated Emissions

150kHz to 30MHz



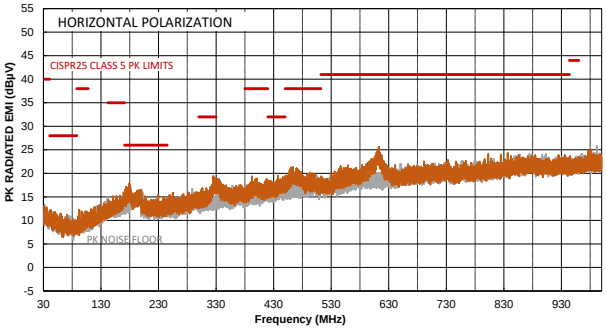
CISPR25 Class 5 Average Radiated Emissions

150kHz to 30MHz



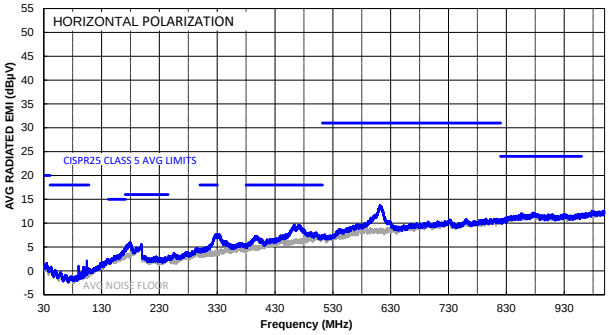
CISPR25 Class 5 Peak Radiated Emissions

Horizontal, 30MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

Horizontal, 30MHz to 1GHz



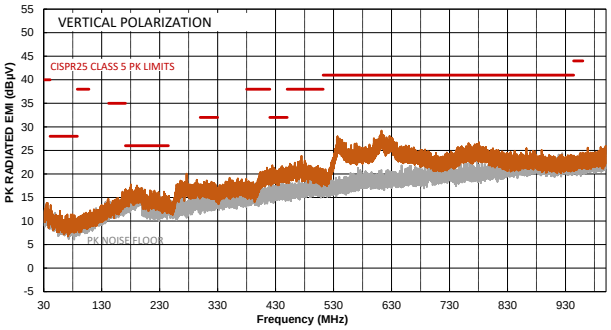
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 1µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted. (12)

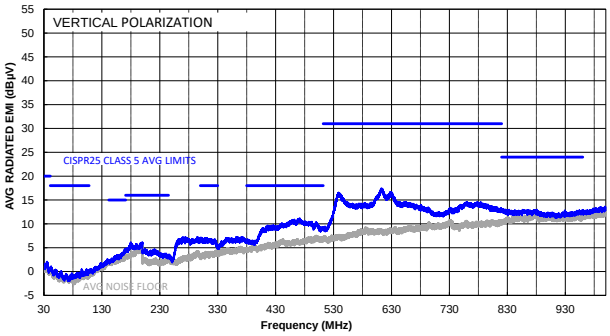
CISPR25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 1GHz



Note:

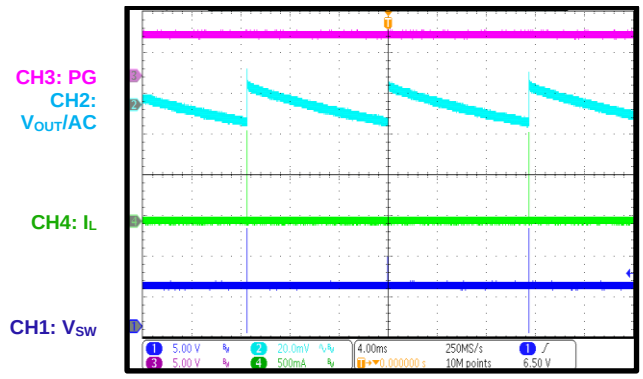
12) The EMC test results are based on the application circuit with EMI filters (see Figure 15 on page 32).

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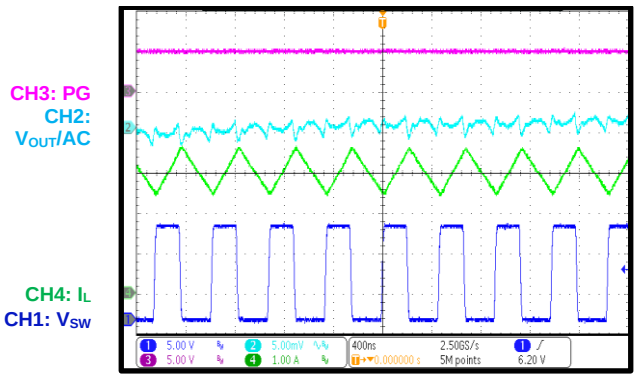
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 1µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

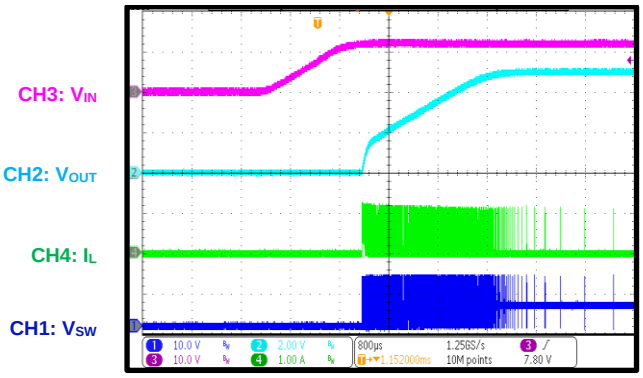
Steady State
I_{OUT} = 0A



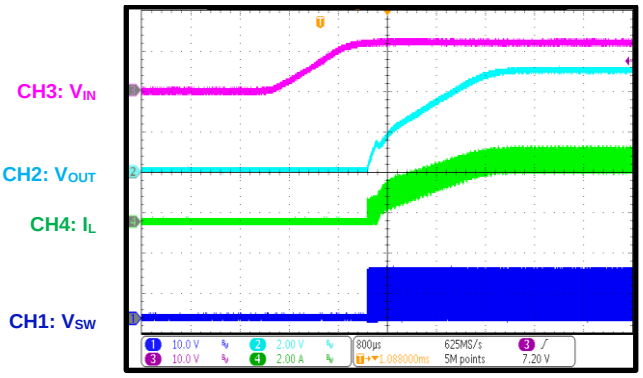
Steady State
I_{OUT} = 3A



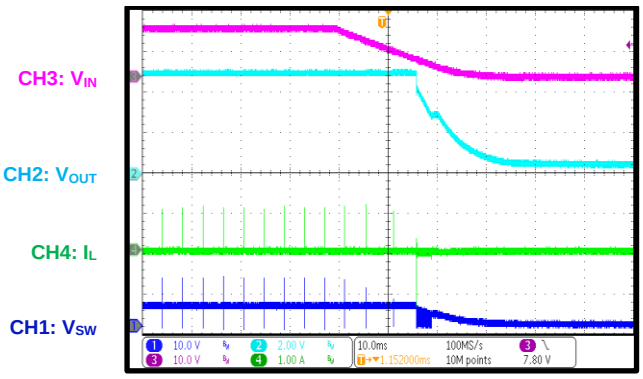
Start-Up through VIN
I_{OUT} = 0A



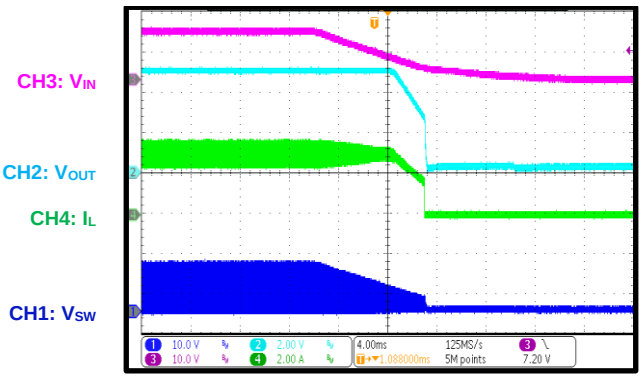
Start-Up through VIN
I_{OUT} = 3A



Shutdown through VIN
I_{OUT} = 0A



Shutdown through VIN
I_{OUT} = 3A

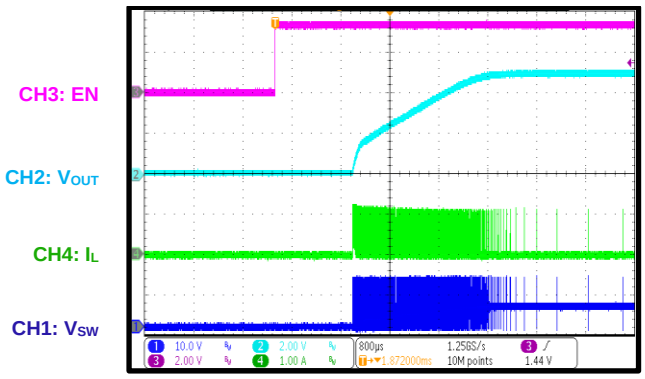


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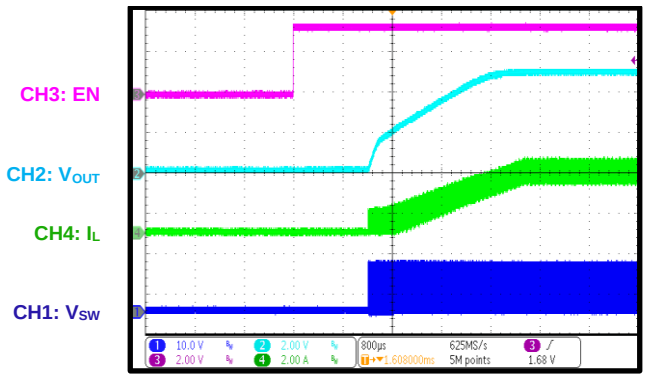
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 1µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

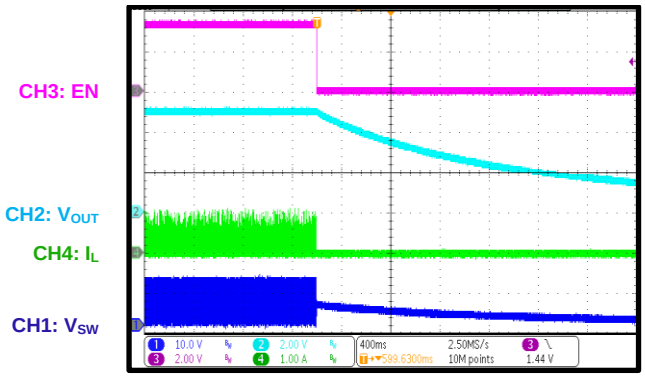
Start-Up through EN
I_{OUT} = 0A



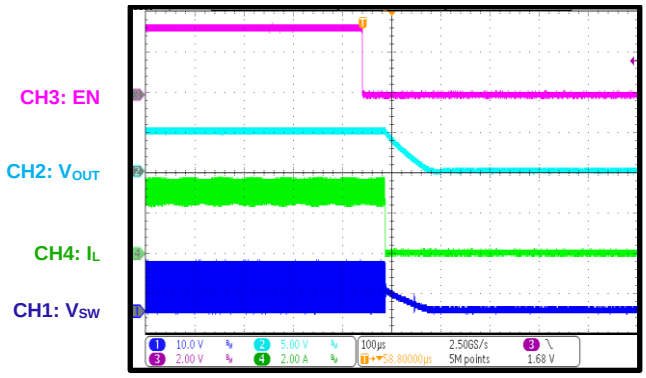
Start-Up through EN
I_{OUT} = 3A



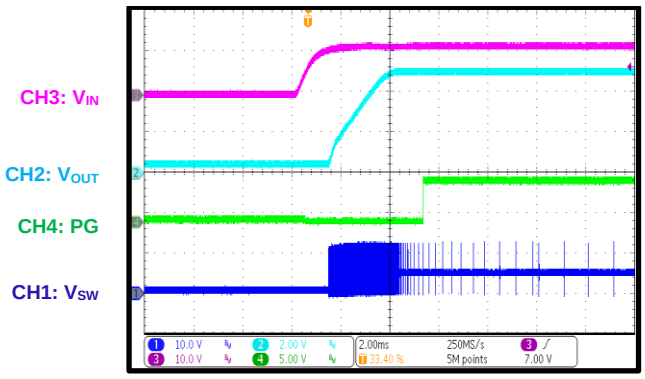
Shutdown through EN
I_{OUT} = 0A



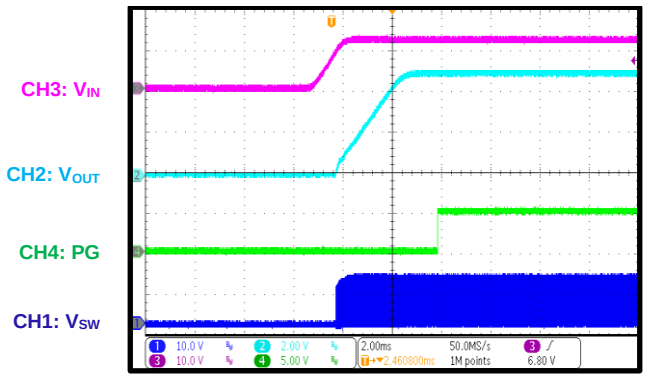
Shutdown through EN
I_{OUT} = 3A



PG in Start-Up through VIN
I_{OUT} = 0A



PG in Start-Up through VIN
I_{OUT} = 3A



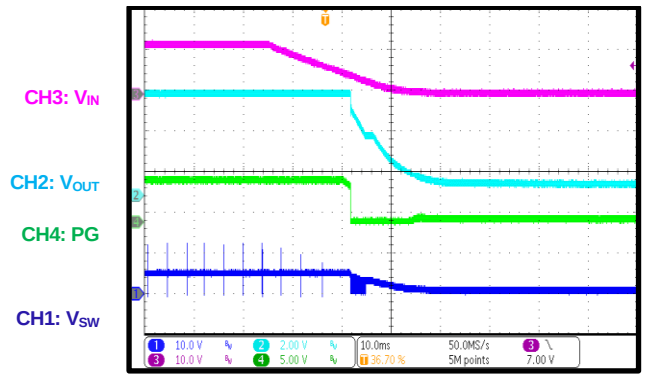
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 1µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

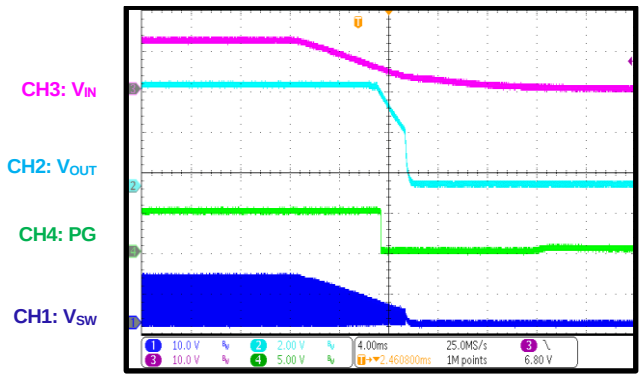
PG in Shutdown through VIN

I_{OUT} = 0A



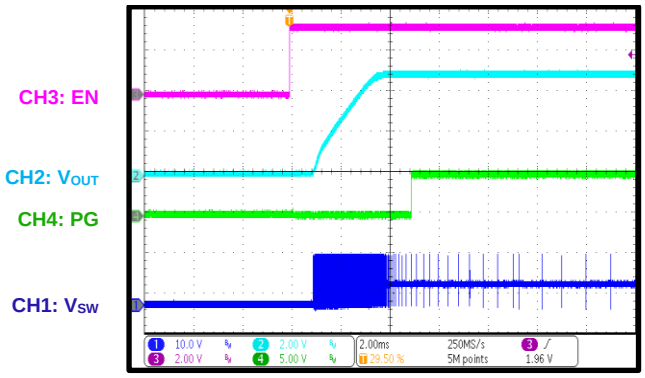
PG in Shutdown through VIN

I_{OUT} = 3A



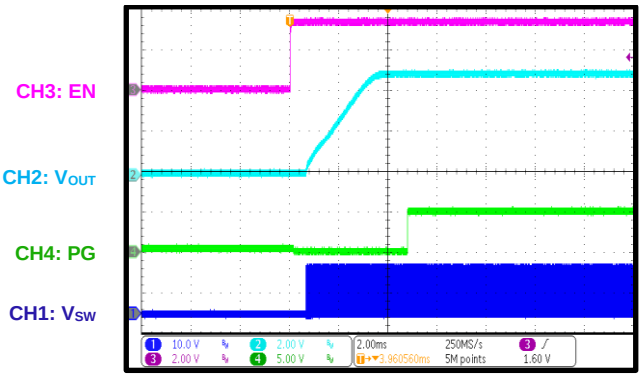
PG in Start-Up through EN

I_{OUT} = 0A



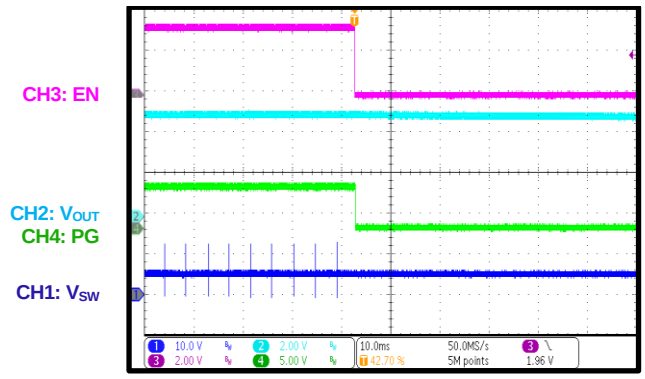
PG in Start-Up through EN

I_{OUT} = 3A



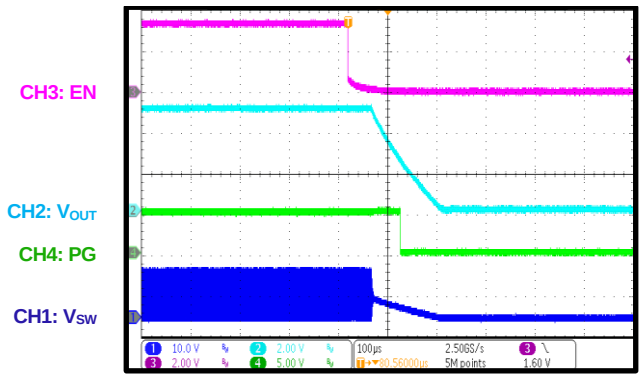
PG in Shutdown through EN

I_{OUT} = 0A



PG in Shutdown through EN

I_{OUT} = 3A



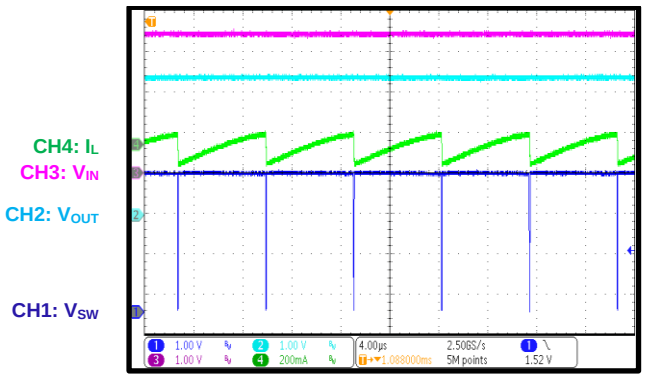
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 1µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

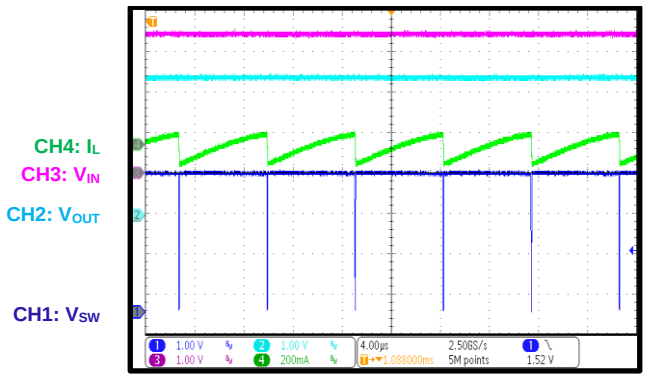
Low-Dropout Mode

I_{OUT} = 0A, V_{IN} = 3.3V



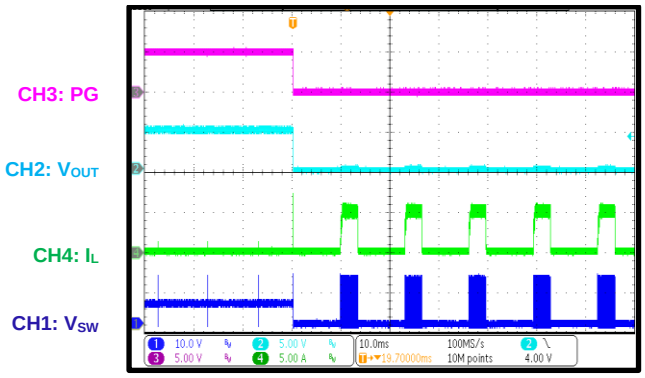
Low-Dropout Mode

I_{OUT} = 3A, V_{IN} = 3.3V



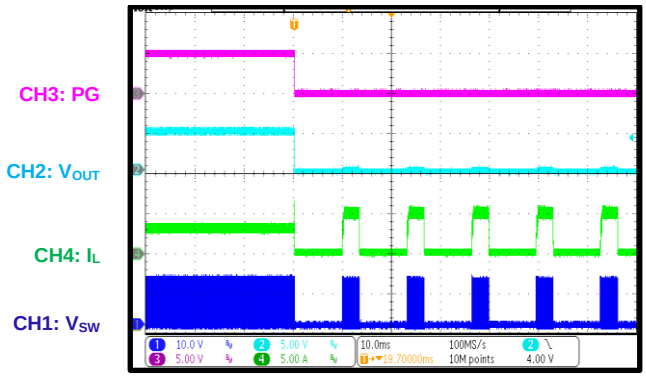
SCP Entry

I_{OUT} = 0A



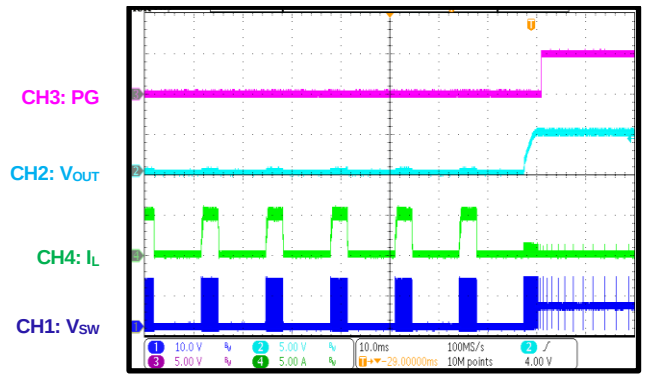
SCP Entry

I_{OUT} = 3A



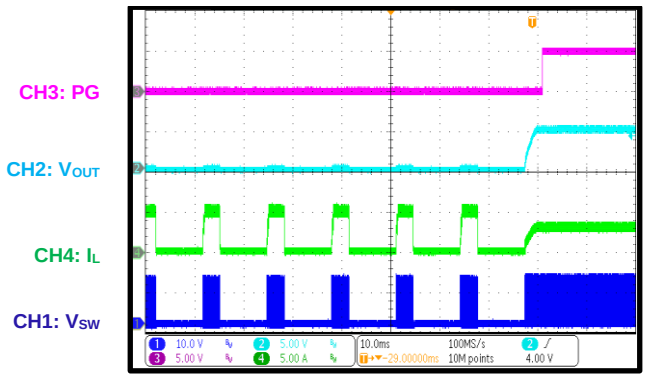
SCP Recovery

I_{OUT} = 0A



SCP Recovery

I_{OUT} = 3A



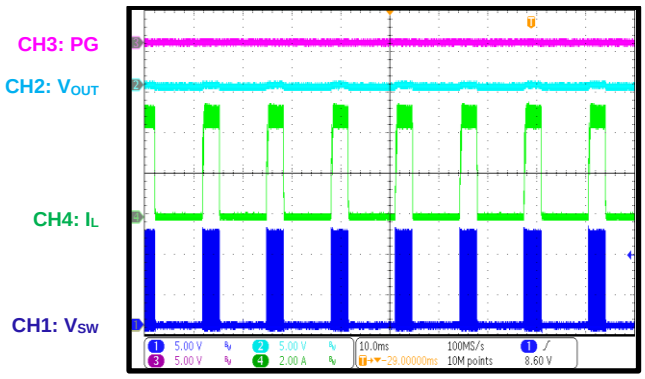
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 1µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

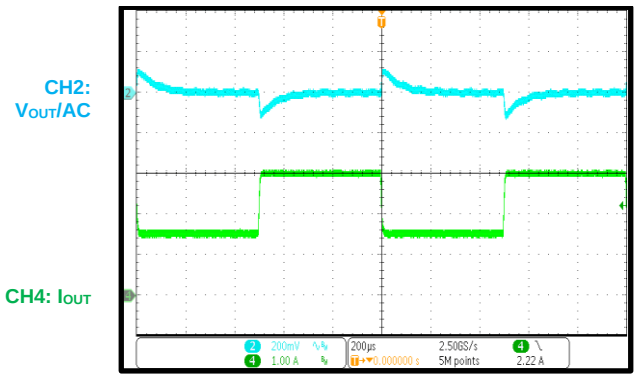
SCP Steady State

I_{OUT} = 0A



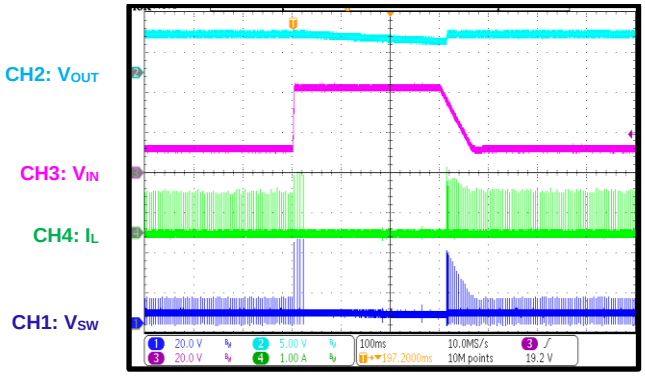
Load Transient

I_{OUT} = 1.5A to 3A, 1.6A/µs



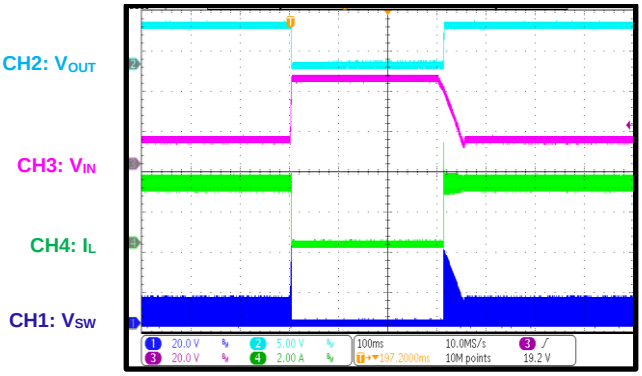
Load Dump

V_{IN} = 12V to 42V, I_{OUT} = 0A



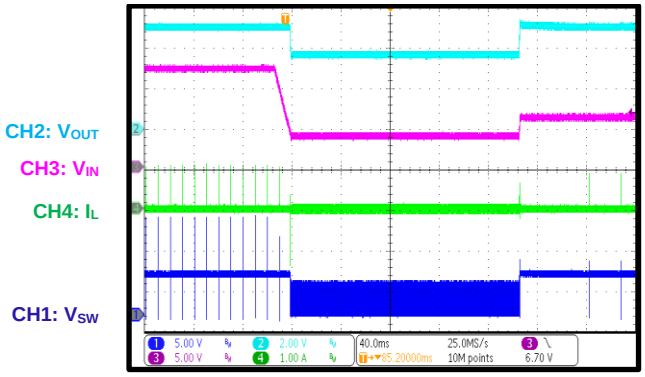
Load Dump

V_{IN} = 12V to 42V, I_{OUT} = 3A



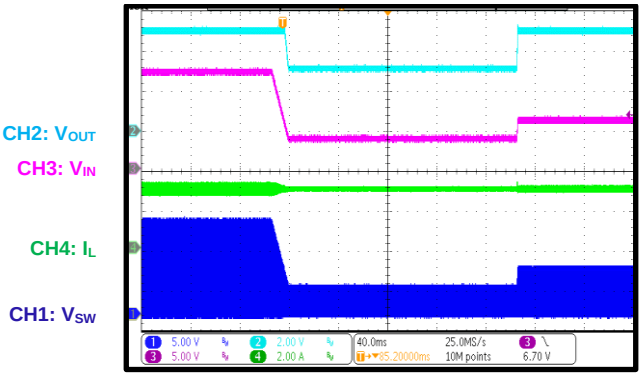
Cold Crank

V_{IN} = 12V to 3.3V to 6V, I_{OUT} = 0A



Cold Crank

V_{IN} = 12V to 3.3V to 6V, I_{OUT} = 3A



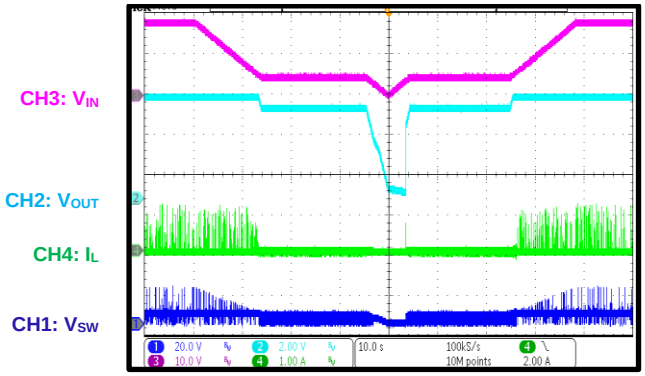
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 1µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

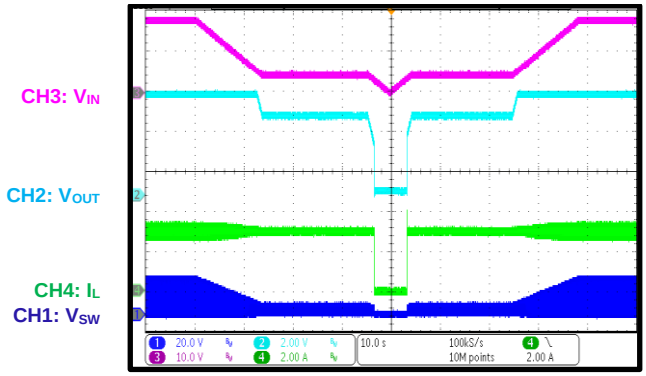
V_{IN} Ramping Down and Up

V_{IN} = 18V to 4.5V to 0V to 4.5V to 18V,
I_{OUT} = 0A



V_{IN} Ramping Down and Up

V_{IN} = 18V to 4.5V to 0V to 4.5V to 18V,
I_{OUT} = 3A



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FUNCTIONAL BLOCK DIAGRAM

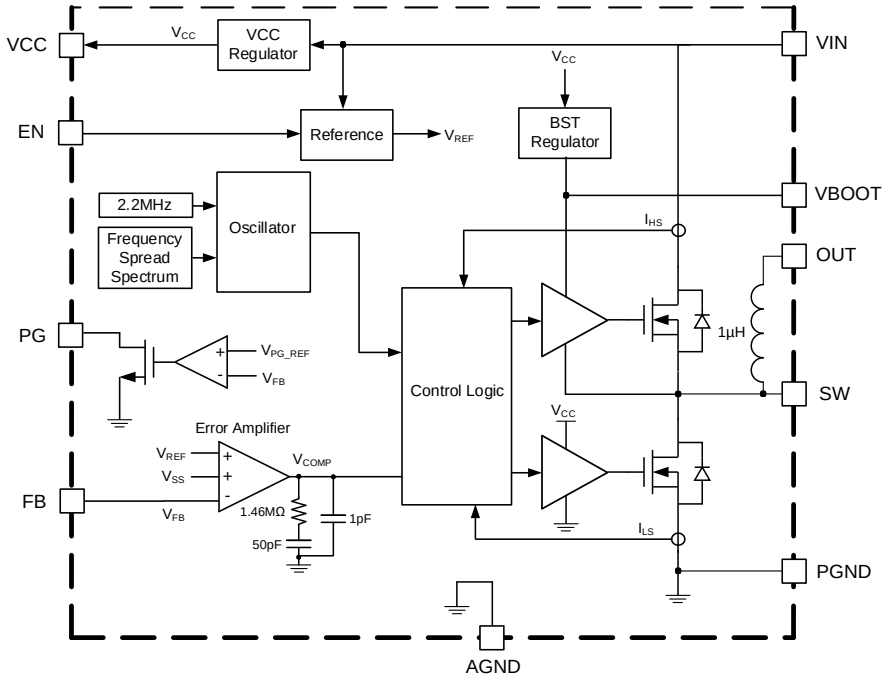


Figure 3: Functional Block Diagram (Adjustable-Output Version)

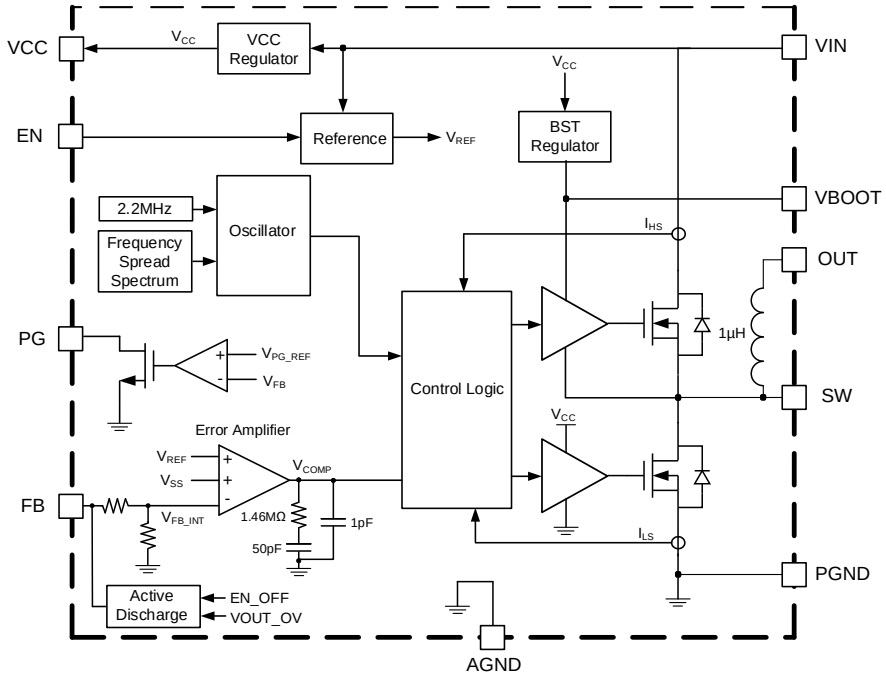


Figure 4: Functional Block Diagram (Fixed-Output Version)

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OPERATION

The MPM3551 is a synchronous, step-down power module with an integrated power inductor and high-side and low-side power MOSFETs (HS-FET and LS-FET, respectively). It provides up to 3A of highly efficient output current (I_{OUT}) with peak current mode control.

The MPM3551 features a wide input voltage (V_{IN}) range, fixed 2.2MHz switching frequency (f_{SW}), internal soft start (SS), and precise current limiting. The MPM3551's low operating quiescent current (I_Q) and small solution area makes it well-suited for battery-powered applications and high-density boards.

Peak Current Mode Control

At moderate to high output currents, the MPM3551 operates with a fixed frequency, peak current mode control to regulate the output voltage (V_{OUT}). A pulse-width modulation (PWM) cycle is initiated by the internal clock. At the clock's rising edge, the HS-FET turns on and remains on until the control signal reaches the value set by the internal COMP voltage (V_{COMP}).

When the HS-FET is off, the LS-FET turns on immediately and remains on until the next cycle starts or the inductor current (I_L) falls below the zero-current detection (ZCD) current. The LS-FET remains off for at least the minimum off time (t_{OFF_MIN}) before the next cycle starts.

If the current in the HS-FET cannot reach the value set by V_{COMP} within one PWM period, then the HS-FET remains on and skips a turn-off operation. The HS-FET is forced on until it reached the value set by V_{COMP}, or its maximum on time (t_{ON_MAX}) (7µs) is complete. This mode extends the duty cycle, which achieves a low dropout when $V_{IN} \approx V_{OUT}$.

Light-Load Operation

The MPM3551 operates in asynchronous advanced modulation (AAM) mode to optimize efficiency under light-load and no-load conditions.

The MPM3551 enters asynchronous operation as I_L approaches 0A under light-load conditions. If the load decreases further, V_{COMP} drops to its set value, and the device enters AAM mode (see Figure 5).

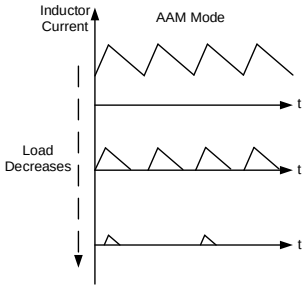


Figure 5: AAM Mode

In AAM mode, the internal clock resets once V_{COMP} reaches its set value. The crossover time is used as a benchmark for the next clock. If the load increases and V_{COMP} exceeds its set value, then the device operates in discontinuous conduction mode (DCM) or continuous conduction mode (CCM) with a constant f_{SW}.

Error Amplifier (EA)

The error amplifier (EA) compares the FB pin voltage (V_{FB}) with the internal reference voltage (V_{REF}) (typically 0.8V), and outputs a current proportional to the difference between the two voltages. This current charges the compensation network to form V_{COMP}, which controls the power MOSFET's duty cycle.

During normal operation, the minimum V_{COMP} is clamped to 0.9V, and the maximum V_{COMP} is clamped to 2V. If the IC shuts down, V_{COMP} is pulled down to AGND internally.

Frequency Spread Spectrum (FSS)

The MPM3551 employs a 15kHz modulation frequency with a maximum 128-step triangular profile to spread the internal oscillator frequency across a 20% (±10%) window. The steps vary with the set oscillator frequency to ensure that the exact f_{SW} steps cycle by cycle (see Figure 6).

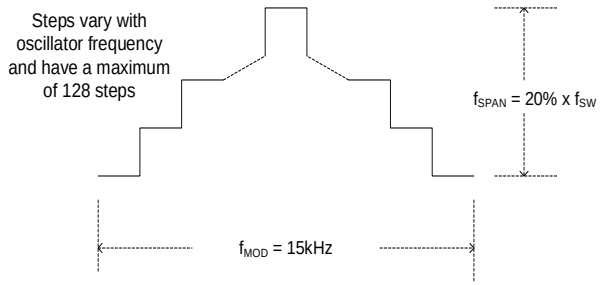


Figure 6: Frequency Spread Spectrum

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Sidebands are created by modulating f_{SW} via the triangle modulation waveform. The emission power of the fundamental f_{SW} and its harmonics are distributed into smaller pieces. This significantly reduces peak EMI noise.

Soft Start (SS)

Soft start (SS) is implemented to prevent V_{OUT} from overshooting during start-up. The soft-start time (t_{SS}) is fixed internally.

Once t_{SS} begins, the soft-start voltage (V_{SS}) rises from 0V to 1.2V with a set slew rate. If V_{SS} drops below the internal V_{REF} (0.8V), then V_{SS} takes over and the EA uses V_{SS} as its reference. If V_{SS} exceeds V_{REF}, then V_{REF} regains control.

During start-up through EN, the first pulse occurs after about 830µs. During this period, the VCC voltage (V_{CC}) is regulated, the internal bias is generated, and the compensator network is charged. After another 2.9ms, V_{OUT} ramps up and reaches its set value. SS is complete after another 1.5ms. PG is also pulled high after a 70µs delay.

Pre-Biased Start-Up

If V_{FB} exceeds V_{SS} during start-up, this means that the output has a pre-biased voltage. Both the HS-FET and LS-FET remain off until V_{SS} exceeds V_{FB}.

Thermal Shutdown

Thermal shutdown prevents the device from operating at exceedingly high temperatures and protects it from thermal runaway. If the silicon die temperature exceeds its upper threshold (175°C), the device shuts down the power MOSFETs. Once the temperature drops below its lower threshold (155°C), the device restarts and resumes normal operation.

Peak Current Limit and Valley Current Limit

Both the HS-FET and LS-FET have cycle-by-cycle current-limit protection. If I_L reaches the high-side (HS) peak current limit (I_{LIMIT_HS}) (typically 5.8A) while the HS-FET is on, the HS-FET is forced off immediately to prevent the current from further rising.

When the LS-FET is on, the next clock's rising edge is held until I_L drops below the low-side (LS) valley current limit (I_{LIMIT_LS}) (typically 4.4A). Once the HS-FET turns on again, I_L can drop to a sufficiently low value. This current limit scheme prevents current runaway if an overload or short-circuit event occurs.

Short-Circuit Protection (SCP)

If the output is shorted to ground and V_{OUT} drops below 70% of its nominal output, the MPM3551 shuts down and begins discharging V_{SS}. The device restarts with a full soft start when V_{SS} is fully discharged. This hiccup process is repeated until the fault is removed.

Output Over-Voltage Protection (OVP) and Discharge

The MPM3551 stops switching if V_{OUT} exceeds 130% of its nominal regulation value and an internal 75Ω discharge path from FB to AGND is activated to discharge V_{OUT}. This discharge path can only be activated if the output is fixed. The device resumes switching when V_{OUT} drops back to 125% of its nominal value. The discharge path is then disabled.

For a fixed output, the V_{OUT} discharge path is also activated if an EN shutdown occurs while V_{CC} exceeds its under-voltage lockout (UVLO) threshold. If V_{CC} drops to its UVLO threshold, this path is deactivated.

Start-Up and Shutdown

If both V_{IN} and the EN voltage (V_{EN}) exceed their respective thresholds, the IC starts up. The reference block starts up first to generate a stable V_{REF} and reference currents. Then the internal regulator is enabled to provide a stable supply for the remaining circuitries.

Once the internal supply rail is up, the internal circuits begin operating. If the VBOOT voltage (V_{BOOT}) does not exceed its refresh rising threshold (typically 2.5V), then the LS-FET turns on to charge VBOOT. The HS-FET remains off during this charging period. When the soft start block is enabled, V_{OUT} starts to ramp up slowly and smoothly until it reaches its target voltage. V_{OUT} should reach its target voltage within 5ms.

Three events can shut down the chip: EN going low, V_{IN} falling below its UVLO threshold, and thermal shutdown. During shutdown, the signaling path is blocked to avoid any fault triggering. Then V_{COMP} is pulled down and the floating driver disables the HS-FET.

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APPLICATION INFORMATION

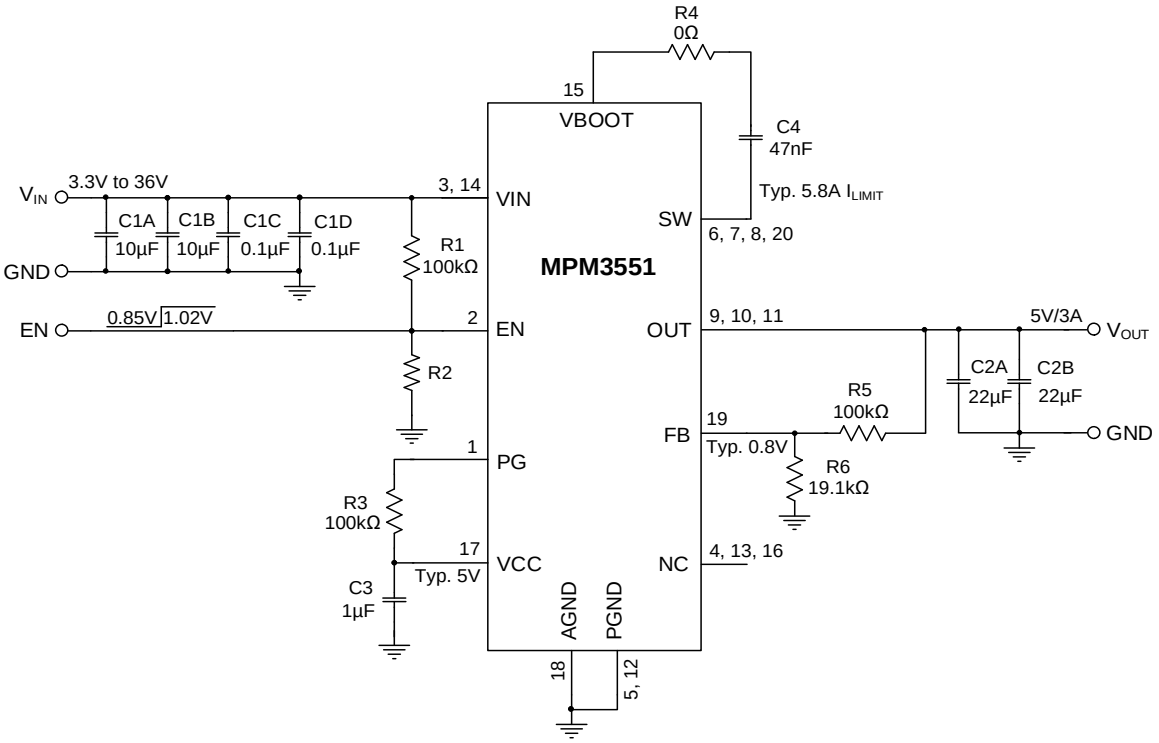


Figure 7: Typical Application Circuit (V_{OUT} = 5V, f_{SW} = 2.2MHz)

Table 1: Design Guide Index

Pin #	Pin Name	Component	Design Guide Index
1	PG	R3	Power Good (PG) Indicator (PG, Pin 8)
2	EN	R1, R2	Enable (EN) and Under-Voltage Lockout (UVLO) (EN, Pin 2)
3, 14	VIN	C1A, C1B, C1C, C1D	Selecting the Input Capacitors (VIN, Pins 3 and 14)
4, 13, 16	NC	-	Not Connected (NC, Pins 4, 13, and 16)
5, 12	PGND	-	Power Ground Connection (PGND, Pins 5 and 12)
6, 7, 8, 20	SW	-	Internal Power Inductor Connection (SW, Pins 6, 7, 8, and 20)
9, 10, 11	OUT	C2A, C2B	Selecting the Output Capacitors (OUT, Pins 9, 10, and 11)
15	VBOOT	R4, C4	Floating Driver and Bootstrap Charging (VBOOT, Pin 15)
17	VCC	C3	Setting the Internal VCC (VCC, Pin 17)
18	AGND		Analog Ground Connection (AGND, Pin 18)
19	FB	R5, R6	Feedback (FB, Pin 19)

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Power Good (PG) Indicator (PG, Pin 8)

The power good (PG_ resistor (R3, also called R_{PG}) should have a resistance of about 100kΩ.

The MPM3551 includes an open-drain PG output that indicates whether V_{OUT} is within its nominal range.

If using PG, connect it to a logic high level power source (e.g. 3.3V) via a pull-up resistor. If V_{OUT} is within 94.5% to 105.5% of the nominal voltage, then PG goes high; if V_{OUT} exceeds 107% or drops below 93% of the nominal voltage, then PG goes low. Float PG if it is not used.

Enable (EN) and Under-Voltage Lockout (UVLO) (EN, Pin 2)

EN is a digital control pin that turns the module on and off.

Enabled by an External Logic High/Low Signal

If V_{EN} reaches 0.7V, the bottom gate turns on when V_{IN} exceeds 2.7V. The bottom gate then provides an accurate V_{REF} for the EN threshold. Pull EN above its rising threshold (about 1.02V) to enable the part. Pull EN below 0.85V to shut down the part. There is no internal pull-up or pull-down resistor connected to the EN pin, so do not float EN. If the control signal cannot give an accurate high or low logic, then an external pull-up or pull-down resistor is required.

Configurable V_{IN} Under-Voltage Lockout (UVLO) Threshold

The MPM3551 has an internal, fixed UVLO threshold. The rising threshold is 3.65V, and the falling threshold is about 2.9V. For applications that require a higher UVLO threshold, place an external resistor divider between VIN and EN to raise the equivalent UVLO threshold (see Figure 8).

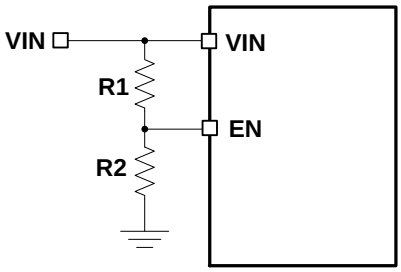


Figure 8: Configurable UVLO via the EN Divider

The UVLO rising threshold ($V_{IN_UVLO_RISING}$) can be calculated with Equation (1):

$$V_{IN_UVLO_RISING} = (1+\frac{R1}{R2}) \times V_{EN_RISING} \quad (1)$$

Where the EN rising threshold (V_{EN_RISING}) is 1.02V

The UVLO falling threshold ($V_{IN_UVLO_FALLING}$) can be calculated with Equation (2):

$$V_{IN_UVLO_FALLING} = (1+\frac{R1}{R2}) \times V_{EN_FALLING} \quad (2)$$

Where the EN falling threshold ($V_{EN_FALLING}$) is 0.85V.

If EN is not used to turn the IC on and off, connect EN to a high-voltage source (e.g. VIN) to turn the device on by default.

Selecting the Input Capacitors (VIN, Pins 3 and 14)

The step-down converter has a discontinuous input current, and requires a capacitor to supply AC current to the converter while maintaining the DC V_{IN}. For the best performance, use low-ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients.

For most applications, it is recommended to use a 4.7µF to 10µF capacitor. It is strongly recommended to use another, lower-value capacitor (e.g. 0.1µF) with a small package size (0603) to absorb high-frequency switching noise. Place the smaller capacitor as close to VIN and PGND as possible.

Since the input capacitor (C_{IN}) absorbs the input switching current, it requires an adequate ripple current rating. The RMS current for C_{IN} (I_{CIN}) can be estimated with Equation (3):

$$I_{CIN} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1-\frac{V_{OUT}}{V_{IN}})} \quad (3)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, which can be calculated with Equation (4):

$$I_{CIN} = \frac{I_{LOAD}}{2} \quad (4)$$

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For simplification, choose C_{IN} with an RMS current rating greater than half of the maximum load current.

C_{IN} can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g. 0.1µF) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input.

The input voltage ripple (ΔV_{IN}) caused by the capacitance can be estimated with Equation (5):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (5)$$

GND Connection (PGND, Pins 5 and 12; AGND, Pin 18)

See the PCB Layout Guidelines on page 29 for more details.

Internal Power Inductor Connection (SW, Pins 6, 7, 8, and 20)

The SW pin is the source of the HS-FET and the drain of the LS-FET. SW is connected to the power inductor internally.

Selecting the Output Capacitors (OUT, Pins 9, 10, and 11)

The peak inductor current (I_{L_PEAK}) can be calculated with Equation (6):

$$I_{L_PEAK} = I_{LOAD} + \frac{V_{OUT}}{2 \times f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (6)$$

Where f_{SW} is 2.2MHz and L is 1µH.

The worst-case condition for the integrated inductor occurs at a saturation rating of 4.5A. Ensure that any transient overload does not result in I_{LP} exceeding this value, which risks triggering the current limit.

The output voltage ripple (ΔV_{OUT}) can be estimated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (7)$$

Where L is the inductance, and R_{ESR} is the equivalent series resistance (ESR) of the output capacitor (C_{OUT}). C_{OUT} maintains the DC V_{OUT}. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For the best results, use low-ESR capacitors to keep ΔV_{OUT} low.

For ceramic capacitors**,** the capacitance dominates the impedance at f_{SW} and causes the majority of ΔV_{OUT}. For simplification, ΔV_{OUT} can be calculated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (8)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at f_{SW}. For simplification, ΔV_{OUT} can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (9)$$

When selecting C_{OUT}, consider the allowable overshoot in V_{OUT} if the load is suddenly removed. In this scenario, energy stored in the inductor is transferred to C_{OUT}, causing its voltage to rise. To achieve an optimal overshoot relative to the regulated voltage, C_{OUT} can be estimated with Equation (10):

$$C_{OUT} = \frac{I_{OUT}^2 \times L}{V_{OUT}^2 \times ((V_{OUT_MAX} / V_{OUT})^2 - 1)} \quad (10)$$

Where V_{OUTMAX} / V_{OUT} is the allowable maximum overshoot.

After calculating the capacitance that meets both the ripple and overshoot requirements, choose the larger capacitance.

The C_{OUT} characteristics also affect the stability of the regulation system. The MPM3551 can be optimized for a wide range of capacitances and ESR values.

Floating Driver and Bootstrap Charging (VBOOT, Pin 15)

The VBOOT capacitor (C4, also called C_{VBOOT}) is recommended to be between 22nF and 100nF**.**

It is not recommended to place a resistor (R_{VBOOT}) in series with C_{VBOOT}, unless there is a strict EMI requirement. R_{VBOOT} reduces EMI and voltage stress at high input voltages; however, it also generates additional power consumption and reduces efficiency. If necessary, R_{VBOOT} should be less than 4Ω.

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The voltage between the VBOOT and SW pins ($V_{BOOT-SW}$) is regulated to about 5V by the dedicated, internal VBOOT regulator. If $V_{BOOT-SW}$ drops below its regulated value, then a P-channel MOSFET pass transistor connected between VCC and VBOOT turns on to charge C_{VBOOT}. The external circuit should provide enough voltage headroom to facilitate charging. When the HS-FET is on, V_{BOOT} exceeds V_{CC} so C_{VBOOT} cannot charge.

At higher duty cycle operation, the time available for VBOOT charging is shorter, so C_{VBOOT} may not charge sufficiently. In this case, the external circuit has insufficient voltage and time to charge C_{VBOOT}. External circuitry can be used to ensure that V_{BOOT} remains within its normal operating range.

If V_{BOOT} reaches its UVLO threshold, then the HS-FET turns off and the LS-FET turns on for t_{MIN_OFF} to refresh V_{BOOT} via the set f_{SW}.

V_{IN} Over-Voltage Protection (OVP)

The MPM3551 stops switching when V_{IN} exceeds its over-voltage (OV) rising threshold (typically 37.5V). The device resumes normal regulation and switching when V_{IN} drops back to its OV falling threshold (typically 36.5V).

Setting the Internal VCC (VCC, Pin 17)

The VCC capacitor (C3, also called C_{VCC}) is recommended to be 1µF.

Most of the internal circuitry is powered by the internal 5V VCC regulator. This regulator uses V_{IN} as its input and operates across the entire V_{IN} range. If V_{IN} exceeds 5V, then V_{CC} is in full regulation. If V_{IN} drops below 5V, the VCC output degrades.

Feedback (FB, Pin 19)

For the adjustable-output version, the typical V_{FB} is 0.8V. The external resistor dividers (R5 and R6) connected to FB set V_{OUT} (see Figure 9).

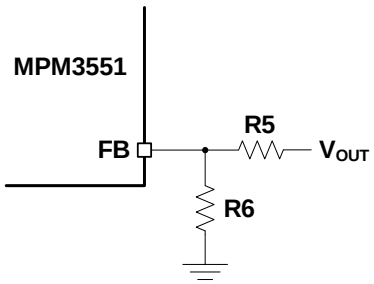


Figure 9: Feedback Divider Network for Adjustable-Output Version

R6 can be calculated with Equation (11):

$$R6 = \frac{R5}{\frac{V_{OUT}}{0.8V} - 1} \quad (11)$$

For the fixed-output version, the FB resistor dividers (R_{FB1} and R_{FB2}) are integrated internally (see Figure 10). Connect FB directly to the output to set V_{OUT}. The following fixed outputs can be selected: 1V, 1.8V, 2.5V, 3V, 3.3V, 3.8V, and 5V.

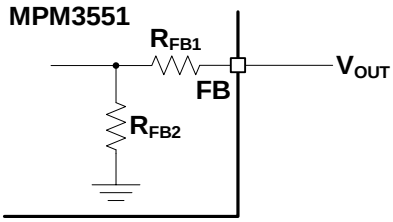


Figure 10: Feedback Divider Network for Fixed-Output Version

Table 2 shows the relationship between the internal R_{FB} and V_{OUT}.

Table 2: R_{FB} vs. V_{OUT}

V_{OUT} (V)	R_{FB1} (kΩ)	R_{FB2} (kΩ)
1	64	256
1.8	320	256
2.5	544	256
3	704	256
3.3	800	256
3.8	960	256
5	1344	256

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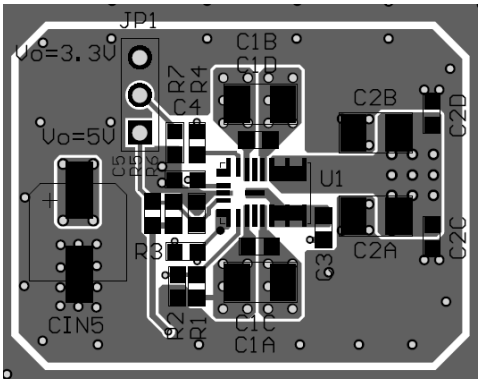
PCB Layout Guidelines [13]

Efficient PCB layout, especially for input capacitor placement, is critical for stable operation. A 4-layer layout is strongly recommended to improve thermal performance. For the best results, refer to Figure 11 and follow the guidelines below:

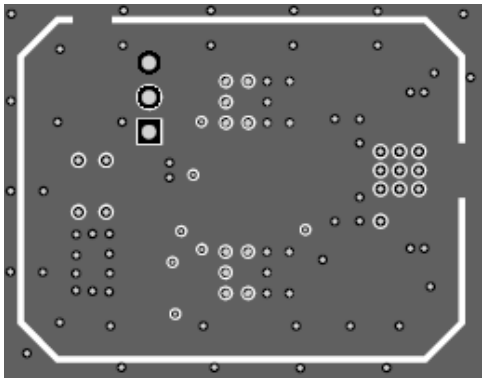
1. Place the symmetric input capacitors as close to VIN and PGND as possible.
2. Connect a large ground plane directly to PGND.
3. If the bottom layer is a ground plane, add vias near PGND.
4. Ensure that the high-current paths at PGND and VIN have short, direct, and wide traces.
5. Place the ceramic input capacitor, especially the small package size (0603) input bypass capacitor, as close to VIN and PGND as possible to minimize high-frequency noise.
6. Keep the connection between the input capacitor and VIN as short and wide as possible.
7. Place the VCC capacitor as close to VCC and AGND as possible.
8. Route SW and VBOOT away from sensitive analog areas, such as FB.
9. Place the feedback resistors close to the chip to ensure the trace that connects to FB is as short as possible.
10. Use multiple vias to connect the power planes to the internal layers.

Note:

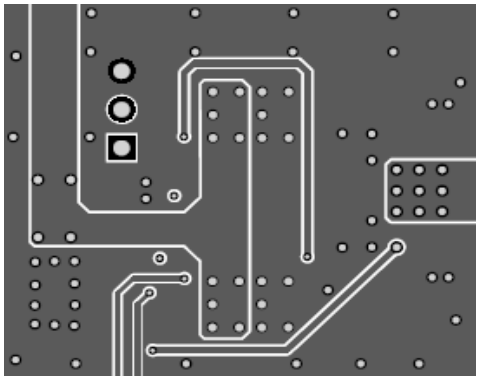
13) The recommended PCB layout is based on Figure 7 on page 25.



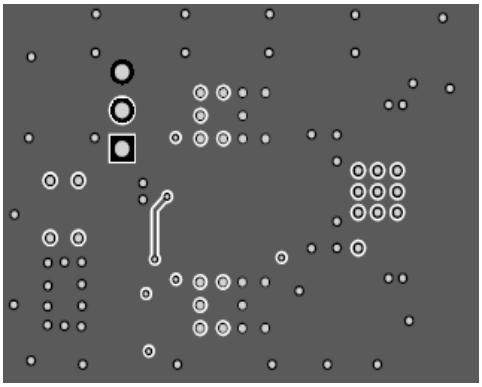
Top Layer and Top Silk



Mid-Layer 1



Mid-Layer 2



Bottom Layer and Bottom Silk

Figure 11: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUITS

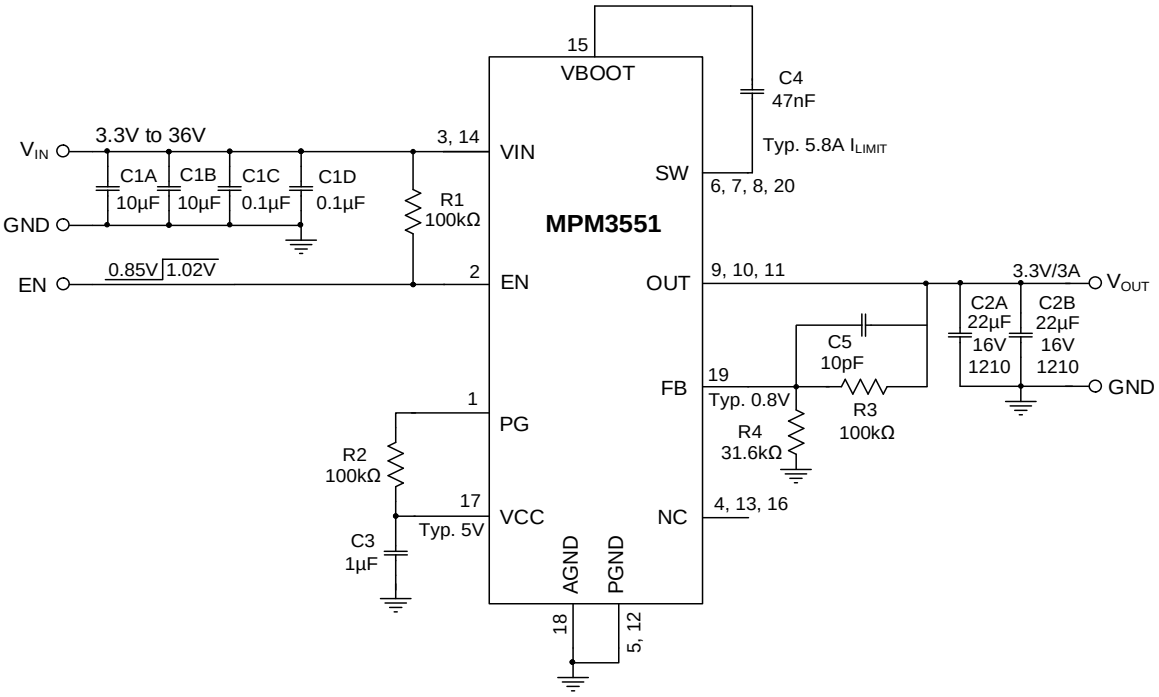


Figure 12: Typical Application Circuit (V_{OUT} = 3.3V, Internal f_{SW} = 2.2MHz)

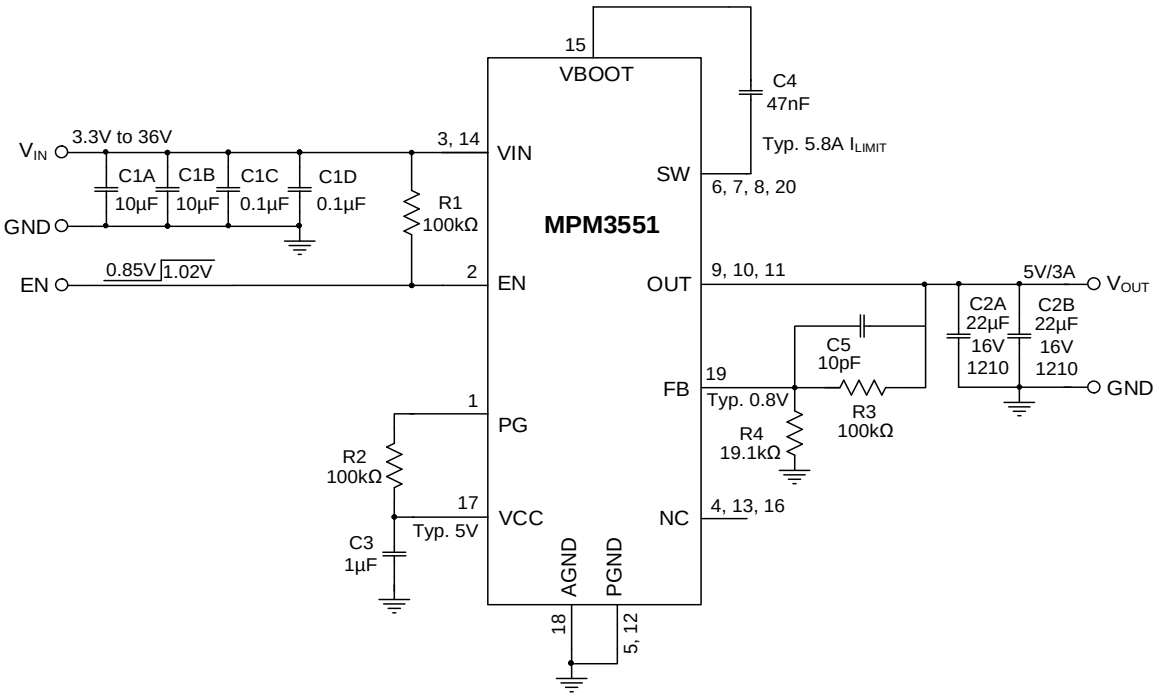


Figure 13: Typical Application Circuit (V_{OUT} = 5V, Internal f_{SW} = 2.2MHz)

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TYPICAL APPLICATION CIRCUITS *(continued)*

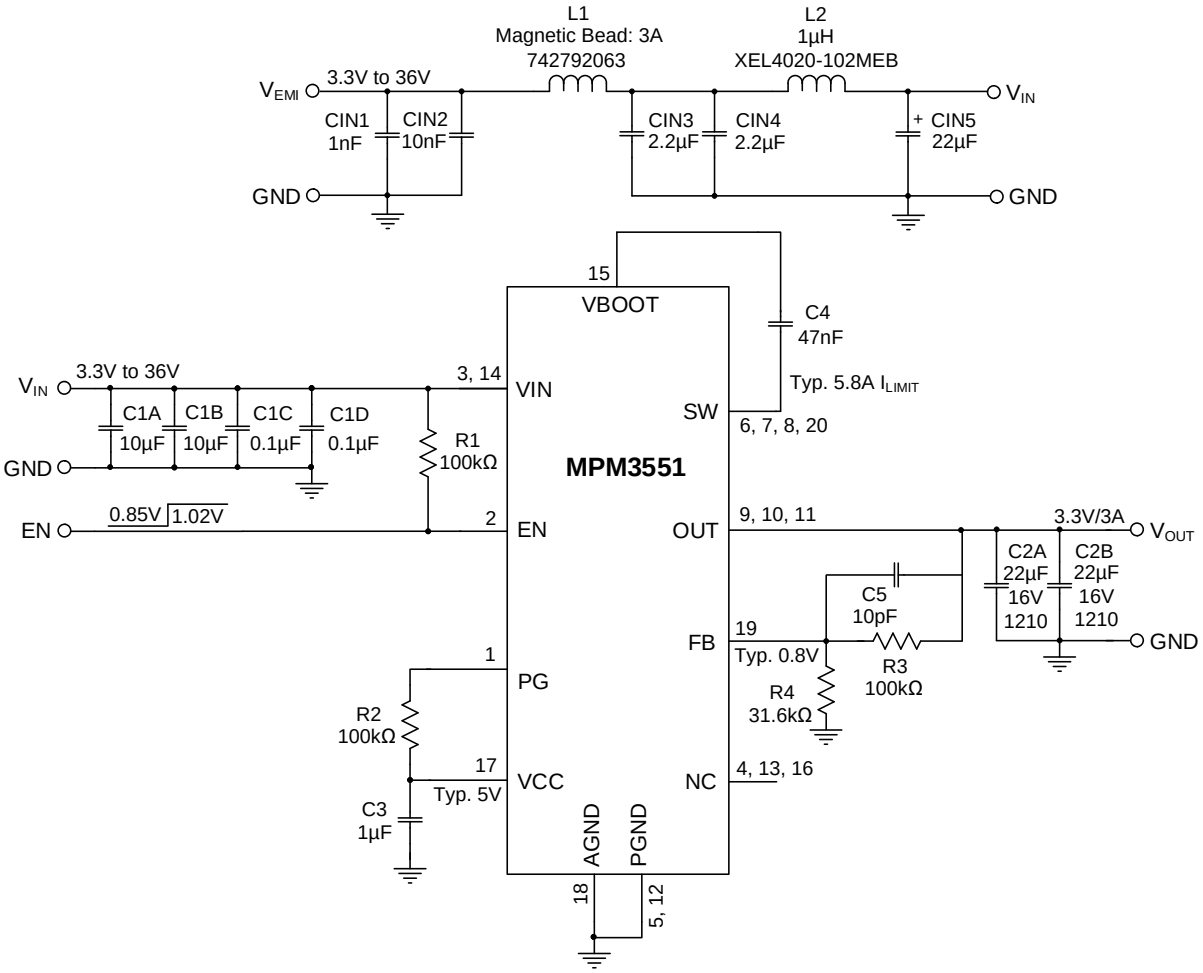


Figure 14: Typical Application Circuit (V_{OUT} = 3.3V, Internal f_{SW} = 2.2MHz with EMI Filters)

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TYPICAL APPLICATION CIRCUITS *(continued)*

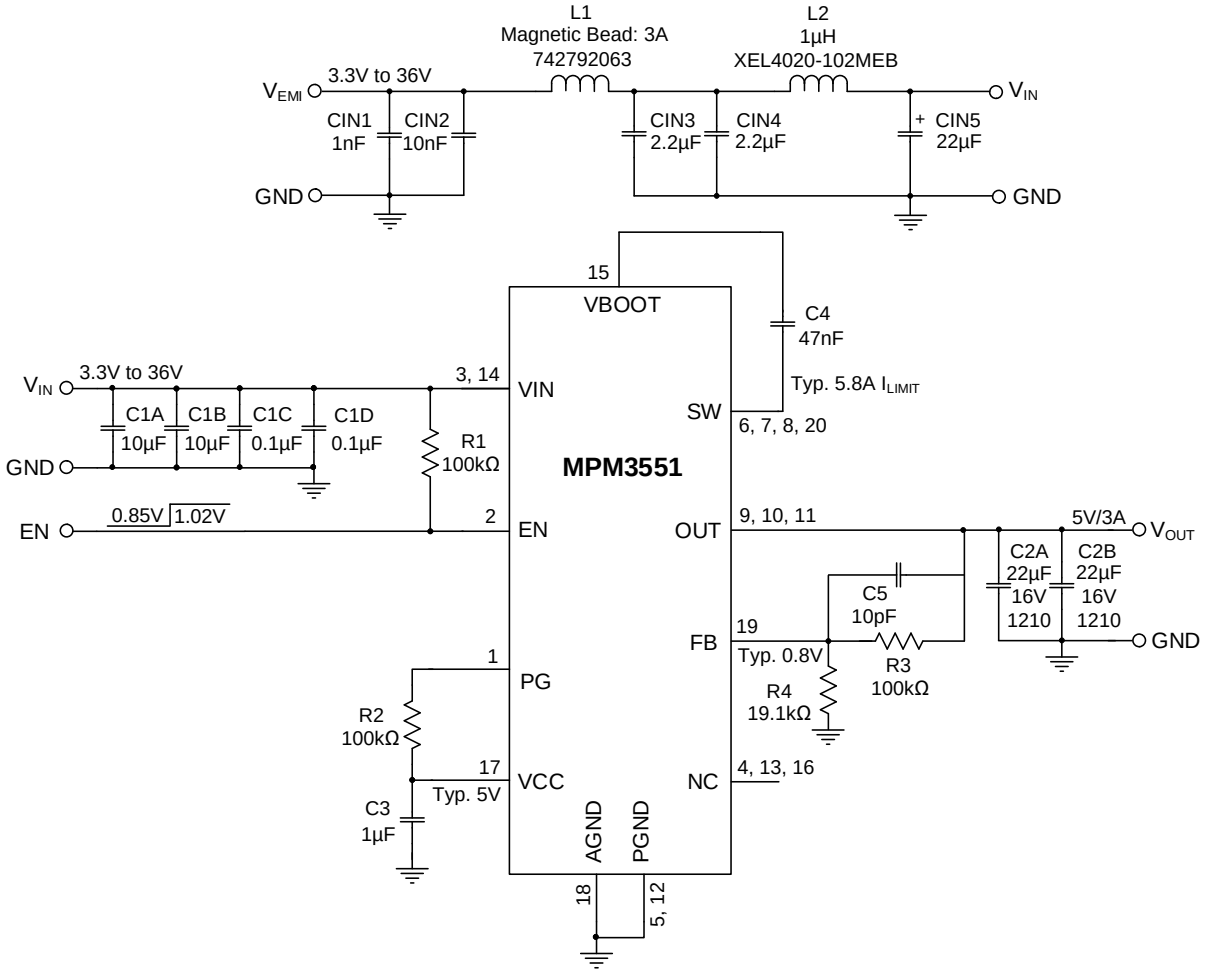
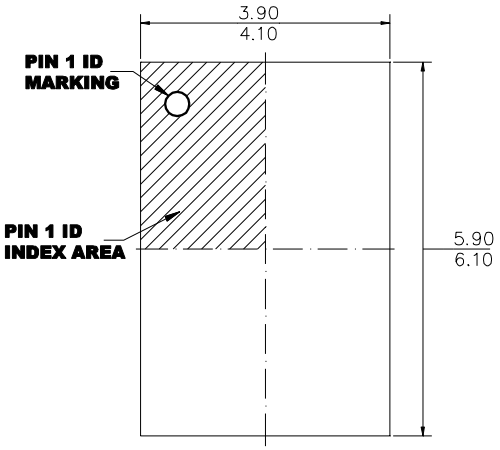


Figure 15: Typical Application Circuit (V_{OUT} = 5V, Internal f_{SW} = 2.2MHz with EMI Filters)

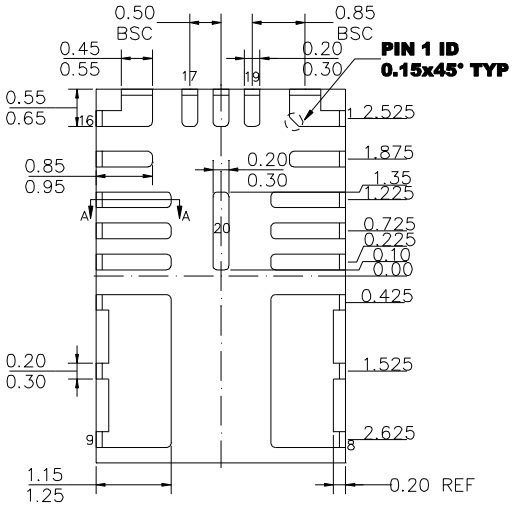
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PACKAGE INFORMATION

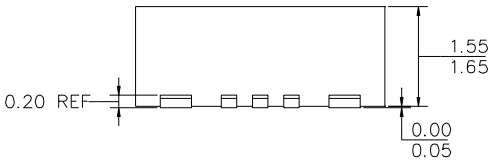
QFN-20 (4mmx6mm)
Wettable Flank



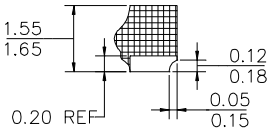
TOP VIEW



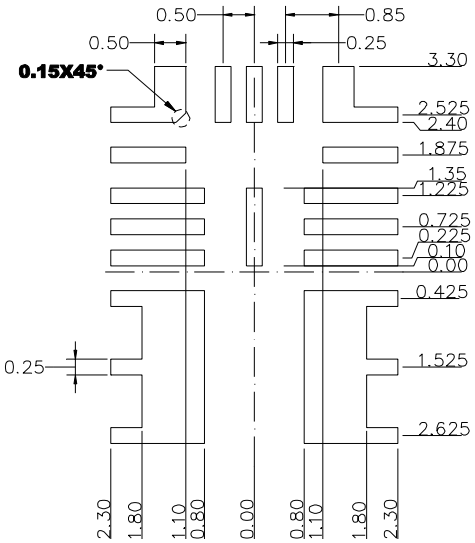
BOTTOM VIEW



SIDE VIEW



SECTION A-A



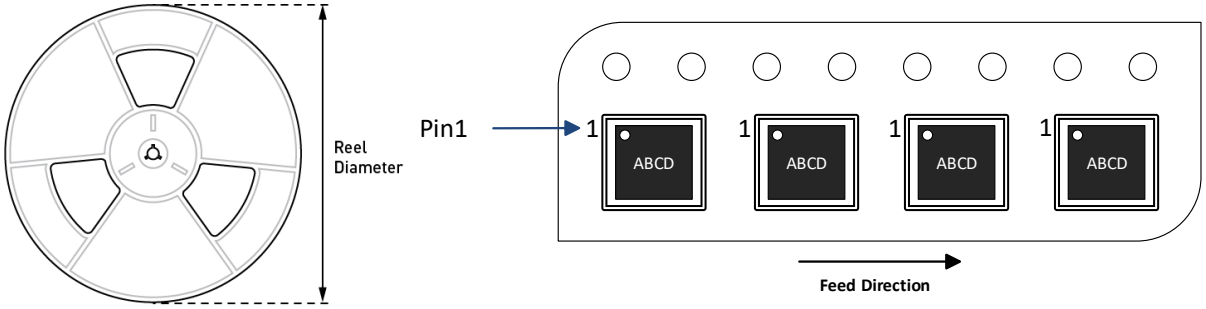
RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPM3551GQWE-Z	QFN-20 (4mmx6mm)	5000	N/A	N/A	13in	12mm	8mm
MPM3551GQWE-AEC1-Z	QFN-20 (4mmx6mm)	5000	N/A	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	7/24/2023	Initial Release	-

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