MPQ4241

65W, Fully Intergrated USB PD Solution with 36V Tolerant Input Buck and PD3.1 DFP Controller, AEC-Q100 Qualified

DESCRIPTION

The MPQ4241 is a fully integrated solution for USB Type-C ports. The device integrates a buck converter with integrated power switches and a USB power delivery (PD) controller. It achieves 65W of continuous output power (P_{OUT}) across a wide input voltage (V_{IN}) supply range with excellent load and line regulation.

The MPQ4241 provides CC over-current protection (OCP) with high accuracy. The USB port is designed for USB Type-C ports, and it is also compatible with legacy USB Type-A ports. The USB Type-C port supports USB PD Revision 3.1 with programmable power supply (PPS) and is backwards compatible with dedicated charging port (DCP) schemes for battery charging specification (BC1.2), 3A divider mode, and 1.2V/1.2V mode without the need for outside user interaction. It supports QC4+ and Huawei FCP modes as well.

The MPQ4241 provides a configurable USB power delivery power (PDP) management state machine when the battery voltage (V_{BATT}) is low, or when an over-temperature condition occurs. When two MPQ4241 devices are used in dual PD ports, the internal power sharing logic can intelligently distribute the total power.

Fault condition protections includes fixed power delivery object (PDO) OCP, DP/DM/CCx over-voltage protection (OVP), output OVP, and thermal shutdown.

The MPQ4241 requires a minimal number of readily available, standard external components. It is available in a QFN-21 (3mmx4mm) package with wettable flanks, and is available in AEC-Q100 Grade 1.

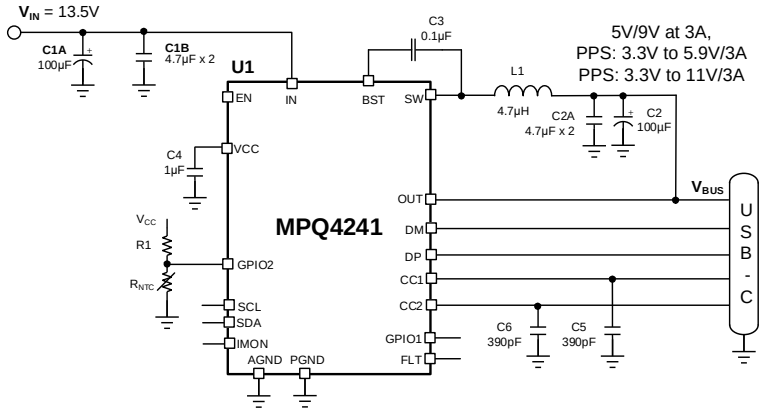
FEATURES

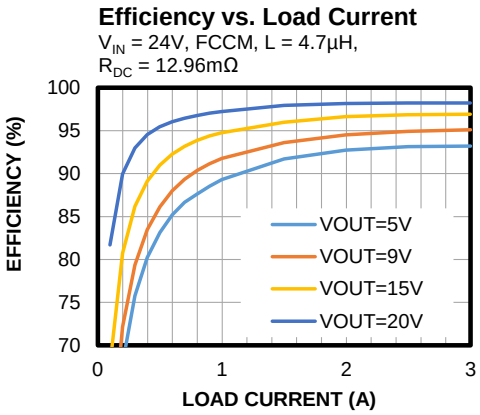
- Integrated, High-Efficiency Buck Converter and Provider-Only PD Controller
- Wide 4.5V to 24V Operating Input Range
- 36V Tolerant Input Voltage (V_{IN})
- 3.3V to 21V Output Voltage (V_{OUT}) Range
- Up to 21V/65W Output Power (P_{OUT})
- Accurate Internal Output CC Current Limit
- Integrated Buck Converter with Internal 30mΩ/18mΩ Low On Resistance ($R_{DS(ON)}$) MOSFETs
- Supports Low-Dropout (LDO) Mode with 99.6% Duty Cycle
- Low Quiescent Current (I_Q) When USB Type-C is Detached
- 250k/420k/2.2MHz Switching Frequency (f_{SW}) with Dithering
- Supports f_{SW} Synchronization
- Supports USB Type-C V2.1
- Supports USB PD R3.1 and PPS
- Supports QC4+ Specification, Huawei FCP
- Supports USB 3.1 Hub Applications
- Supports DCP Schemes for BC1.2, 3A Divider Mode, and 1.2V/1.2V Mode
- CC/DP/DM Short to VBUS (14V) Protection
- I^2C Interface
- Integrated 1W VCONN Switch
- Output Line-Drop Compensation
- Output Over-Voltage Protection (OVP)
- FCCM or Auto PFM/PWM Operation
- Automatic Power Derating during High Temperatures
- Automatic Power Derating at Low Battery Voltage (V_{BATT})
- Available in a QFN-21(3mmx4mm) Package with Wettable Flanks
- Available in AEC-Q100 Grade 1

APPLICATIONS

- USB Power Supplies
- USB PD Ports

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPQ4241GLE-0000-AEC1***	QFN-21 (3mmx4mm)	*See Below*	1
MPQ4241GLE-0001-AEC1****			
MPQ4241GLE-xxxx-AEC1**			
EVKT-MPQ4241	-	-	-

* For Tape & Reel, add suffix -Z (e.g. MPQ4241GLE-xxxx-AEC1-Z).

** “xxxx” is the configuration code identifier for the register setting stored in the OTP. Each “x” can be a hexadecimal value between 0 and F. Work with an MPS FAE to create this unique number.

*** The MPQ4241GLE-0000-AEC1 is the default version, which can be configured via the OTP by the user one time.

**** The MPQ4241GLE-0001-AEC1 is the reference design version for 27W USB PD applications, which cannot be configured via the OTP by the user.

TOP MARKING

MPYW
4241
LLL
E

MP: MPS prefix
Y: Year code
W: Week code
4241: First four digits of the part number
LLL: Lot number
E: Package code

EVALUATION KIT (EVKT-MPQ4241)

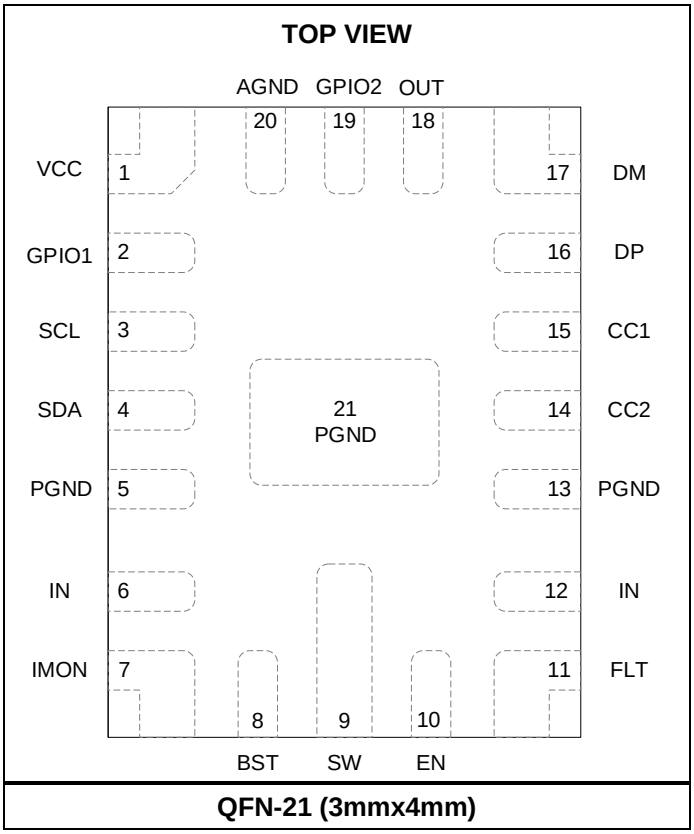
EVKT-MPQ4241 kit contents (items below can be ordered separately):

#	Part Number	Item	Quantity
1	EVQ4241-LE-00A	The MPQ4241 evaluation board	1
2	EVKT-USBI2C-02	Includes one USB-to-I^{2}C communication interface device, one USB cable, and one ribbon cable	1
3	MPQ4241GLE-0000-AEC1	The MPQ4241 IC, which can be used for OTP configurations one time	2
4	Online resources	Includes GUI and supplemental files	-

Order directly from MonolithicPower.com or our distributors.

Figure 1: EVKT-MPQ4241 Evaluation Kit Set-Up

PACKAGE REFERENCE



QFN-21 (3mmx4mm)

PIN FUNCTIONS

<table>
<tr><th>Pin #</th><th>Name</th><th colspan="2">Description</th></tr>
<tr><td>1</td><td>VCC</td><td colspan="2">Internal 5V LDO regulator output. Decouple the VCC pin with a 1µF capacitor.</td></tr>
<tr><td rowspan="8">2</td><td rowspan="8">GPIO1</td><td>NTC_CNT</td><td>NTC thermal sense input for Type-C connector. In QC4, MPQ4241 reports connector temperature via this pin.</td></tr>
<tr><td>ALT</td><td>USB Type-C attach or fault status indication. The ALT pin is an open-drain structure. When a sink is attached or detached, the ALT pin asserts a low pulse for 12µs. If a fault event is triggered, the ALT pin is always pulled low.
<table>
<tr><td>Attach Rising or Falling Edge</td><td>0</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>Fault Event</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>GPIO1_ALT_OUTPUT</td><td>Open drain</td><td>12µs pull-down pulse</td><td>Low</td><td>Low</td></tr>
</table></td></tr>
<tr><td>POWER_SHARE</td><td>Input pin. Apply a low voltage to this pin to force the chip to enter power-sharing.</td></tr>
<tr><td>FAULT</td><td>Fault output. Indicates if the following protections occur: USB over-current protection (OCP; FAULT is not pulled down when the sink device requests an augmented power data object (APDO) during constant current limit (CC) entry), DP/DM/CCx over-voltage protection (OVP), and thermal shutdown (TSD). FAULT is an open drain under normal conditions and pulled low if a fault occurs. This function is enabled when V_{BUS} is present.</td></tr>
<tr><td>POL</td><td>USB Type-C plug polarity indicator. The POL pin is an open-drain output. When CC1 is selected as the CC line, the POL pin pulls low. When CC2 is selected as the CC line or detached, the POL pin is an open drain.</td></tr>
<tr><td>NTC2</td><td>Second NTC thermal-sense input.</td></tr>
<tr><td>I2C_ADD</td><td>Input pin to set different I²C slave addresses.</td></tr>
<tr><td>SYNC_IN</td><td>External CLK sync input. Accepts ±20% of the internal base frequency setting while the external CLK input duty cycle is between 10% and 90%.</td></tr>
<tr><td>3</td><td>SCL</td><td colspan="2">I²C clock signal input.</td></tr>
<tr><td>4</td><td>SDA</td><td colspan="2">I²C data line.</td></tr>
<tr><td>5, 13, 21</td><td>PGND</td><td colspan="2">Power ground. The PGND node should be placed outside of the C_{IN} ground path to prevent switching current spikes from inducing voltage noise into the part.</td></tr>
<tr><td>6, 12</td><td>IN</td><td colspan="2">Supply voltage. The MPQ4241 operates from a 4.5V to 24V unregulated input, and supports a 36V tolerant voltage. An input capacitor (C_{IN}) is needed to prevent large voltage spikes from appearing at the input. Place C_{IN} as close to the IC as possible. It is the drain of the internal power device and power supply for the whole chip. Pin 6 and pin 12 are not connected to each other internally; short them via the PCB trace.</td></tr>
<tr><td>7</td><td>IMON</td><td colspan="2">Output current monitor output. The IMON pin outputs a voltage proportional to the output current. It is recommended to connect a 4.7kΩ + 4.7nF RC filter to the IMON pin.</td></tr>
<tr><td>8</td><td>BST</td><td colspan="2">Bootstrap. A 0.1µF capacitor is connected between SW and BST to form a floating supply across the high-side switch driver.</td></tr>
<tr><td>9</td><td>SW</td><td colspan="2">Switch output. Use a wide PCB trace to make the connection.</td></tr>
<tr><td>10</td><td>EN</td><td colspan="2">Enable control pin. Apply a logic high voltage on the EN pin to enable the IC; pull EN to logic low to disable the IC. The EN pin has an internal 6µA pull-up current.</td></tr>
<tr><td>11</td><td>FLT</td><td colspan="2">Fault indicator. The FLT pin indicates whether the following protections occur: USB over-current protection (OCP; FAULT is not pulled down when the sink device requests APDO during CC entry), DP/DM/CCx OVP, and TSD. FLT is an open drain under normal conditions and pulled low if a fault occurs. The fault function is enabled when V_{BUS} is present.</td></tr>
</table>

PIN FUNCTIONS *(continued)*

Pin #	Name	Description	
14	CC2	**Configuration channel (CC).** The CC2 pin is used in the discovery, configuration, and management of connections across a USB Type-C cable.	
15	CC1	**Configuration channel (CC).** The CC1 pin is used in the discovery, configuration, and management of connections across a USB Type-C cable.	
16	DP	**D+ data line to USB connector.** The DP pin is an input/output used for hand-shaking with portable devices.	
17	DM	**D- data line to USB connector.** The DM pin is an input/output used for hand-shaking with portable devices.	
18	OUT	**Buck output feedback.**	
19	GPIO2	POL	**USB Type-C polarity indication.** The POL pin is an open-drain output. When CC1 is selected as the CC line, the POL pin pulls low. When CC2 is selected as the CC line or detached, the POL pin is an open drain.
		NTC	**NTC thermal-sense input.**
		VCONN_IN	**1W VCONN power supply input.**
		LED_PWM	**Output a PWM driver to LED.**
		ATTACH	**Output to indicate whether a device is attached.** This pin is an open-drain output. If the USB Type-C is attached, this pin pulls low.
		POWER_SHARE	**Input pin.** Apply a low voltage to this pin to force the chip to enter power sharing.
		NTC_CNT	**NTC thermal sense input for USB Type-C connector.** In QC4, the MPQ4241 reports connector temperature via this pin.
		FAULT	**Fault output.** The FAULT pin indicates whether the following protections occur: USB over-current protection (OCP; FAULT is not pulled down when the sink device requests APDO during CC entry), DP/DM/CCx OVP, and TSD. FAULT is an open drain under normal conditions and pulled low if a fault occurs. The fault function is enabled when V_{BUS} is present.
		POWER_SHARE_HIGH_ACTIVE	**Input pin.** Apply a high voltage to this pin to force the chip to enter power-sharing.
20	AGND	**Analog Ground**. Connect AGND to PGND with the shortest possible loop.	

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) .....-0.3V to +40V
V_{EN} .....-0.3V to +40V
V_{OUT}.....-0.3V to +26V
V_{SW}..... -0.3V (-5V for <10ns) to +29V
V_{BST} ..... V_{SW} + 6.5V
$V_{CC/DP/DM}$ .....-0.3V to +16V
All other pins .....-0.3V to +5.5V
Continuous power dissipation (T_A = 25°C) (2)
QFN-21 (3mmx4mm)..... 5.89W
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to +150°C

ESD Ratings (3)

Human body model (HBM) ..... ±2kV
Charged-device model (CDM)..... ±750V

Recommended Operating Conditions (4)

Supply voltage (V_{IN}) .....4.5V to 24V
Tolerant V_{IN} ..... 36V max
Output voltage (V_{OUT}).....3.3V to 21V
Output current.....5A or 65W
Operating junction temp (T_J).... -40°C to +150°C

Thermal Resistance (4) θ_{JA} θ_{JC}

EVQ4241-LE-00A (5) ……...21.2……3.6..°C/W
QFN-21 (3mmx5mm) (6) ……..44……..9... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the device may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) HBM, per JEDEC specification JESD22-A114; CDM, per JEDEC specification JESD22-C101, AEC specification AECQ100-011. JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on a MPQ4241 test board, 43mmx50mm, 4-layer PCB.
6) Measured on a JESD51-7, 4-layer PCB. The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7 and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = floating, T_J = -40°C to +150°C, Typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (shutdown)	I_{IN}	EN = 0V		10	80	μA
Supply current (standby)	I_{Q_STB}	No device attached, I²C EN = 1, T_J = 25°C		150	200	μA
Supply current (quiescent)	I_{Q_BB}	Buck non-switching		4		mA
EN rising threshold	V_{EN_RISING}		-4%	1.32	+4%	V
EN hysteresis	V_{EN_HYS}			140		mV
EN pull-up current	I_{EN}	V_{EN} = 2V		6		μA
Thermal shutdown (7)	T_{TSD}	This can be selected via the I²C		170		°C
Thermal hysteresis (7)	T_{TSD_HYS}			20		°C
V_{IN} under-voltage lockout (UVLO) threshold rising	V_{INUV_R}		-4%	4.1	+4%	V
V_{IN} UVLO hysteresis	V_{INUV_HYS}			300		mV
V_{IN} over-voltage protection (OVP) rising	V_{INOV_RISING}		25.4	26.2	27	V
V_{IN} OVP falling	$V_{INOV\_FALLING}$		24.4	25.2	26	V
VCC regulator	V_{CC}		4.85	5.1	5.35	V
VCC load regulation	V_{CC_REG}	I_{CC} = 70mA,T_J = 25°C		3		%
VBUS_UV falling threshold 1	V_{BUS_UV1}	This can be selected via the I²C	-5%	3	+5%	V
			-5%	4.5	+5%	V
Buck Converter						
High-side (HS) switch on resistance	R_{DSON_HS}			30		mΩ
Low-side (LS) switch on resistance	R_{DSON_LS}			18		mΩ
Output voltage	V_{OUT0}		-3%	3.3	+3%	V
	V_{OUT1}	T_J = 25°C	-1.5%	5.0	+1.5%	V
		T_J = -40°C to +125°C	-2.5%	5.0	-2.5%	V
	V_{OUT2}		-2%	9.0	+2%	V
	V_{OUT3}	V_{IN} = 24V	-2%	20.0	+2%	V
Output over-voltage protection (OVP) rising threshold	V_{OVP_RISING}			117		%
OVP recovery hysteresis	V_{OVP_HYS}			10		%
Output absolute OVP	V_{OVP_ABS}		22.5	23.5	24.5	V
Absolute OVP recovery hysteresis	V_{OVP_HYS}			1		V
Line-drop compensation	V_{LDC}	I²C settings: LINE_DROP_COMP = 01b, ADDITIONAL_LINE_DROP_COMPENSATION = 0b, V_{OUT} = 5V, I_{OUT} = 3A		150		mV
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 25V			80	μA

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = floating, T_J = -40°C to +150°C. Typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Output CC current limit	I_{OC1}	OC threshold = 1A	0.85	1	1.15	A
	I_{OC2}	OC threshold = 3A, T_J = 0°C to 85°C	-5%	3	+5%	A
High-side peak current limit	I_{LIMIT1}	This can be changed via the I²C	-20%	12	+20%	A
Low-side valley limit	I_{LIMIT2}			11.2		A
Over-current protection (OCP) hiccup under-voltage (UV) falling threshold	OCP_{UV}	Set V_{OUT} = 5V	-5%	2.5	+5%	V
Frequency dithering span	f_{DITH_SPAN}			±6		%
Oscillator frequency	f_{SW1}	Set via the I²C	-20%	250	+20%	kHz
	f_{SW2}	Set via the I²C	-20%	420	+20%	kHz
	f_{SW3}	Set via the I²C	-20%	2200	+20%	kHz
Minimum on time (7)	t_{ON_MIN}			110		ns
Minimum off time (7)	t_{OFF_MIN}			50		ns
Maximum on time (7)	t_{MAX_ON}			14		µs
Soft-start time	t_{SS}	5V output from 10% to 90%		1		ms
Output discharge resistance	R_{DIS_OUT}			115		Ω
Negative Temperature Coefficient (NTC, NTC2)						
External thermal sense trip voltage	V_{NTC_ETY}	R_P = 43.2kΩ, R_{NTC} = 4.79kΩ (100°C)	8	10	12	% of V_{CC}
External thermal sense recovery voltage 1	V_{NTC_RCY1}	80°C recovery		20		% of V_{CC}
External thermal sense recovery voltage 2	V_{NTC_RCY2}	I²C setting: NTC_HYSTERESIS = 01b		30		% of V_{CC}
General-Purpose Input/Output (GPIO1)						
Power-sharing input high	V_{IH_PS}		2			V
Power-sharing input low	V_{IL_PS}				0.8	V
Power-sharing pull-up resistor	R_{PS}	Pull up to V_{CC}		1		MΩ
Fault pull-down	R_{PD_FAULT}				30	Ω
Fault leakage	I_{LKG_FAULT}				1	µA
POL pin pull-down	R_{POL_FAULT}	CC1 to GND with 5.1kΩ			30	Ω
POL pin leakage	I_{LKG_POL}	CC2 to GND with 5.1kΩ			1	µA
Attach output	V_{ATTO}	Sink 1mA			0.4	V
GPIO2						
POL pull-down	R_{PD_FAULT2}	CC1 to GND with 5.1kΩ			30	Ω
POL leakage	I_{LKG_FAULT2}	CC2 to GND with 5.1kΩ			5	µA
LED PWM output FREQ	f_{LED}			25		kHz
LED_PWM output duty	D_{LED}			50%		
Attach output	V_{ATTO2}	USB Type-C attached, 1mA sink current			0.4	V
Fault pull-down	R_{PD_FAULT2}				30	Ω

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = Float, T_J = -40°C to +150°C. Typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power-sharing input high	V_{IH_PS2}		2			V
Power-sharing input low	V_{IL_PS2}				0.8	V
VCONN_IN output power	V_{CON_1W}	GPIO2 with 5V supply	1			W
IMON voltage	V_{IMON}	LS source 1A, T_J = 25°C	-10%	270	+10%	mV
Power Good (PG) Indication						
PG rising	V_{PG_RISING}		-3.5%	91.5	+3.5%	% of V_{REF}
PG falling	$V_{PG\_FALLING}$			85		% of V_{REF}
USB CHARGING MODE IDENTIFICATION						
BC1.2 Dedicated Charging Port (DCP) Mode						
DP and DM short resistance	$R_{DP\_DM\_SHORT}$	V_{DP} = 0.8V, I_{DM} = 1mA			40	Ω
Divider Mode						
DP output voltage	$V_{DIVIDER\_DP}$	V_{OUT} = 5V	2.6	2.7	2.8	V
DM output voltage	$V_{DIVIDER\_DM}$	V_{OUT} = 5V	3.15	3.3	3.45	V
DP output impedance	$R_{DIVIDER}$			22		kΩ
DM output impedance	$R_{DIVIDER}$			17.1		kΩ
1.2V/1.2V Mode						
DP/DM output voltage	$V_{DP\_DM\_1.2V}$	V_{OUT} = 5V	1.15	1.25	1.35	V
DP/DM output impedance	$R_{DP\_DM\_1.2V}$		35	75	120	kΩ
Quick Charge (QC) 3.0 Mode						
DP/DM low voltage	V_{QC_LOW}		0.2	0.3	0.4	V
DP/DM high voltage	V_{QC_HIGH}		1.8	2	2.2	V
QC mode entry voltage glitch time (QC identify) (7)	t_{QC_GLITCH}		1000			ms
DP output impendence	R_{DP_QC}			350		kΩ
DM output impendence	R_{DM_QC}			20		kΩ
Request voltage time (7)	$t_{V\_NEW\_REQUEST}$		200			ms
Output voltage change glitch time (7)	$t_{GLITCH\_V\_CHANGE}$		20		60	ms
Unplug V_{BUS} discharge time (7)	$t_{VBUS\_DISC\_QC}$				500	ms
FCP Mode						
DM Tx high voltage (7)	V_{FCPT_H}	R_{LOAD} = 15kΩ	2.55		5	V
DM Tx low voltage (7)	V_{FCPT_L}	R_{LOAD} = 15kΩ			0.4	V
DM Rx high voltage	V_{FCPR_H}		1.5		5	V
DM Rx low voltage	V_{FCPR_L}				1	V
DM pull-low resistance	R_{LD_D-}			20		kΩ
Unit interval for PHY (7)	t_{UI_FCP}		144	160	176	μs
USB Type-C (CC1 and CC2 Pins)						
CC pull-up current 1	I_{RP1}	V_{BUS} = 5V at 3A, T_J = 25°C	-8%	330	+8%	μA

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = floating, T_J = -40°C to +150°C. Typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
CC pull-up current 2	I_{RP2}	V_{BUS} = 5V at 1.5A, T_J = 25°C	-8%	180	+8%	µA
CC voltage to enable V_{CONN} for 3A USB Type-C mode	V_{RA1}				0.75	V
USB Type-C (CC1 and CC2 Pins)						
CC voltage to enable V_{BUS} for 3A USB Type-C mode	V_{RD1}		0.85		2.45	V
CC detach threshold for 3A USB Type-C mode	V_{OPEN1}		2.75			V
CC voltage to enable V_{CONN} for 1.5A USB Type-C mode	V_{RA2}				0.35	V
CC voltage to enable V_{BUS} for 1.5A USB Type-C mode	V_{RD2}		0.45		1.5	V
CC detach threshold for 1.5A USB Type-C mode	V_{OPEN2}		1.7			V
CC voltage falling de-bounce timer	$t_{CC\_DEBOUNCE}$	V_{BUS} enable deglitch	100	150	200	ms
CC voltage rising de-bounce timer	$t_{PD\_DEBOUNCE}$	V_{BUS} disable deglitch	5	10	20	ms
V_{CONN} output power	P_{VCONN}	Default	100			mW
USB PD						
tUnitInterval (7)	t_{UI_PD}		3.03		3.7	µs
Transmitter						
tEndDriveBMC (7)	$t_{END\_DRIVE\_BMC}$				23	µs
Falling time (7)	t_{FALL}		300	400		ns
Rising time (7)	t_{RISE}		300	400		ns
tHoldLowBMC (7)	$t_{HOLD\_LOW\_BMC}$		1			µs
Logic high voltage	V_{LH}		1.05		1.2	V
Logic low voltage	V_{LL}				70	mV
Output impedance	Z_{TX}			34		Ω
Receiver (7)						
CC receiver capacitance	$C_{RECEIVER}$				600	pF
Transitions for signal detection	$N_{TRANSITION}$		3			Edges
Rx bandwidth limiting filter	t_{RX_FILTER}		100			ns
Time window for detecting non-idle	$t_{TRANSITION\_WINDOW}$		12		20	µs
Receiver input impedance	Z_{BMC_RX}		1			MΩ
I^2C Interface Specifications (7)						
Input logic high	V_{IH}	I^2C pull-up voltage from 1.8V to 3.3V	1.26			V
Input logic low	V_{IL}				0.54	V
Output voltage logic low	V_{OUT_L}				0.45	V
SCL clock frequency	f_{SCL}			400		kHz
SCL high time	t_{HIGH}		60			ns

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = floating, T_J = -40°C to +150°C. Typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
SCL low time	t_{LOW}		160			ns
Data set-up time	t_{SU_DAT}		10			ns
Data hold time	t_{HD_DAT}			70		ns
Set-up time for repeated start	t_{SU_STA}		160			ns
Hold time for (repeated) start	t_{HD_STA}		160			ns
Bus free time between a start and a stop command	t_{BUF}		160			ns
Set-up time for stop command	t_{SU_STO}		160			ns
Rising time of SCL and SDA	t_R		10		300	ns
Falling time of SCL and SDA	t_F		10		300	ns
Pulse width of suppressed spike	t_{SP}		0		50	ns
Capacitance bus for each bus line	C_B				400	pF
SCL low time	t_{LOW}		160			ns

Note:

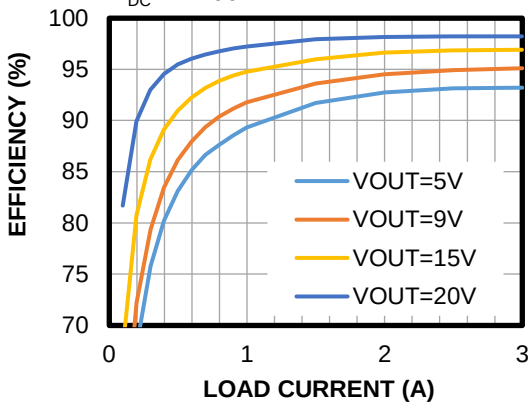
7) Guaranteed by characterization sample test.

TYPICAL CHARACTERISTICS

V_{IN} = 24V, V_{BUS} = 5V, L = 4.7µH, f_{SW} = 420kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

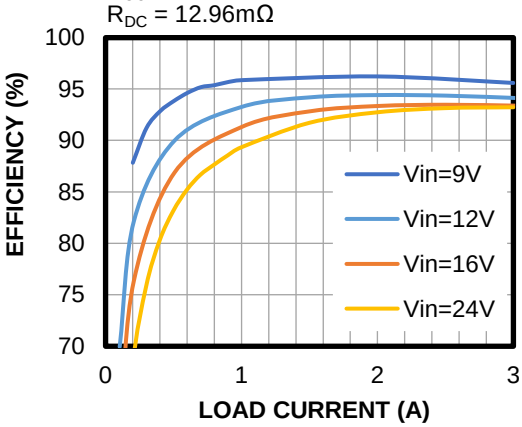
Efficiency vs. Load Current

V_{IN} = 24V, FCCM, L = 4.7µH, R_{DC} = 12.96mΩ



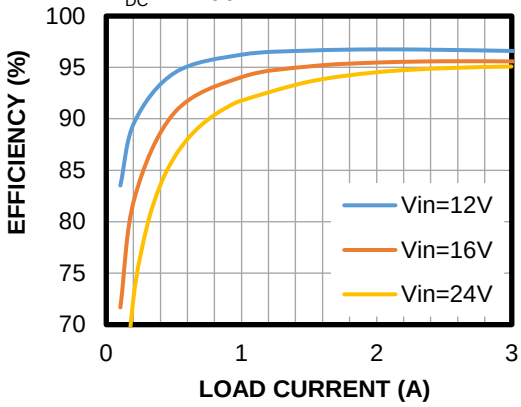
Efficiency vs. Load Current

V_{OUT} = 5V, FCCM, L = 4.7µH, R_{DC} = 12.96mΩ

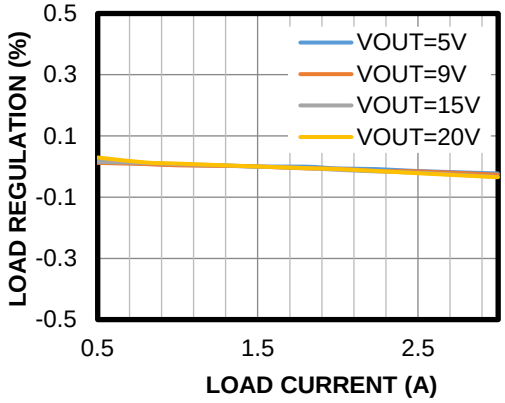


Efficiency vs. Load Current

V_{OUT} = 9V, FCCM, L = 4.7µH, R_{DC} = 12.96mΩ

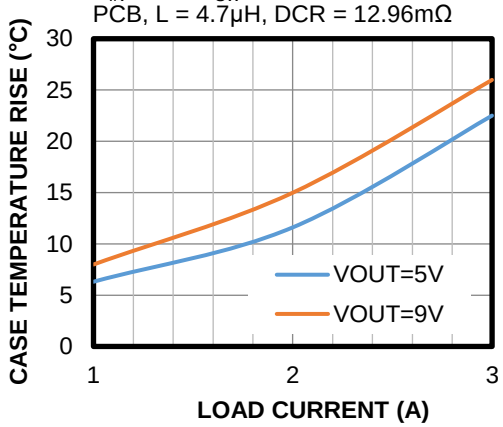


Load Regulation



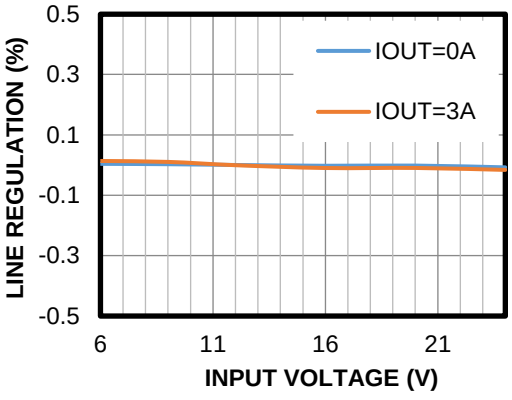
Case Temperature Rise

V_{IN} = 12V, f_{SW} = 420kHz, 4.3cmx5cm PCB, L = 4.7µH, DCR = 12.96mΩ



Line Regulation

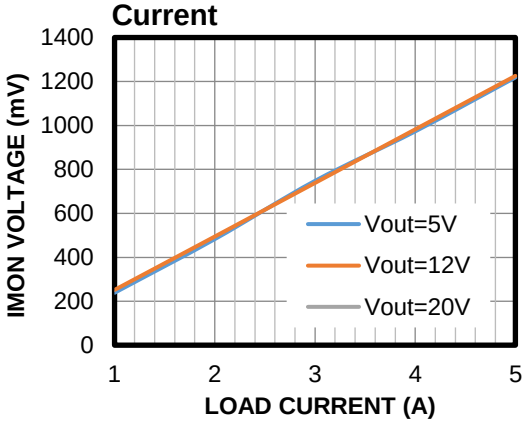
V_{OUT} = 5V, measured between VOUT and PGND



TYPICAL CHARACTERISTICS *(continued)*

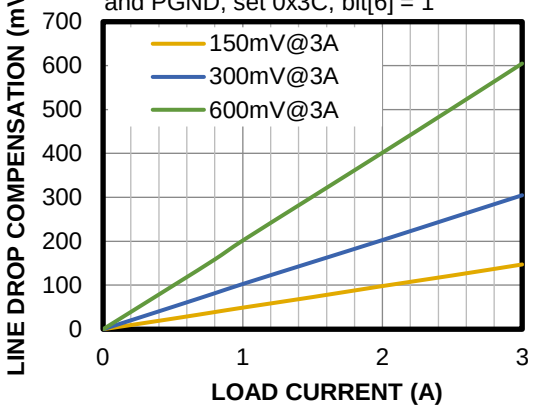
V_{IN} = 24V, V_{BUS} = 5V, L = 4.7µH, f_{SW} = 420kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

IMON Voltage vs. Load Current



Line Drop Compensaton vs. Load Current

V_{OUT} = 5V, measured between VOUT and PGND, set 0x3C, bit[6] = 1

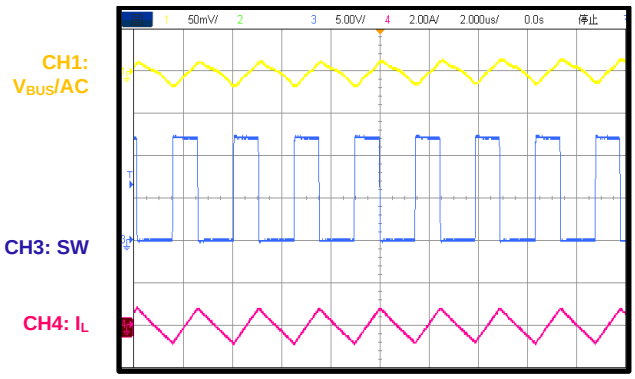


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{BUS} = 5V, L = 4.7µH, f_{SW} = 420kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

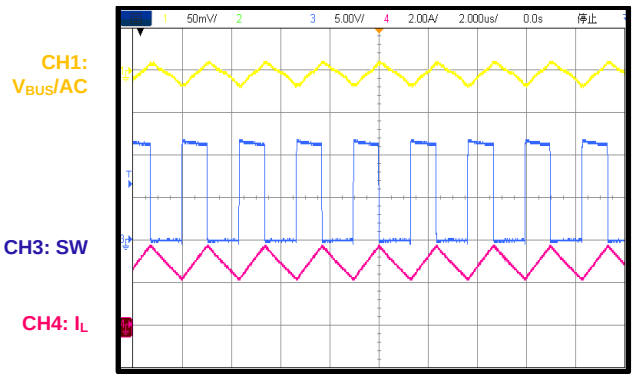
Output Voltage Ripple

V_{BUS} = 5V, load = 0A



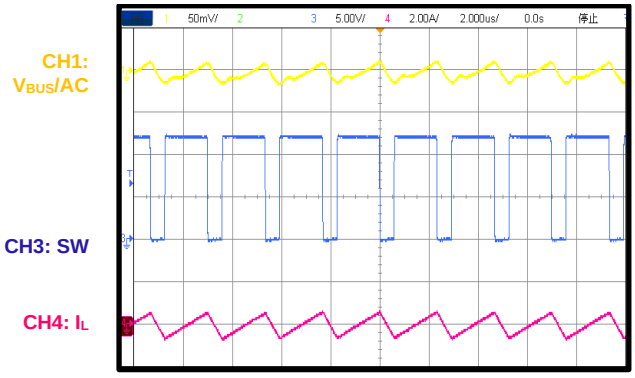
Output Voltage Ripple

V_{BUS} = 5V, load = 3A



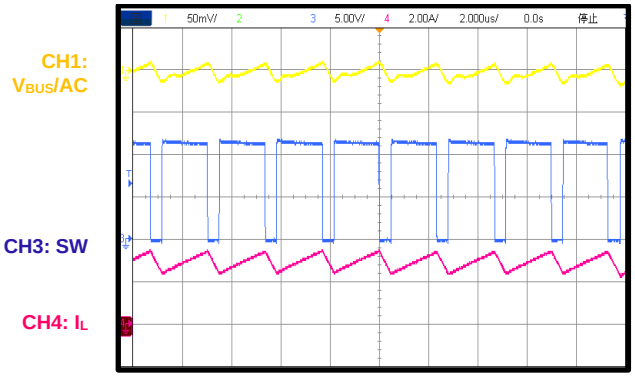
Output Voltage Ripple

V_{BUS} = 9V, load = 0A



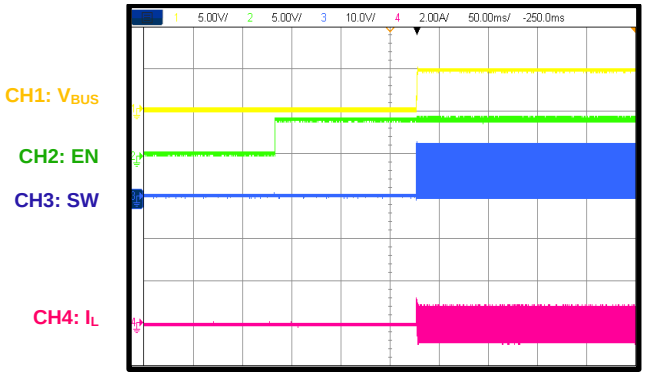
Output Voltage Ripple

V_{BUS} = 9V, load = 3A



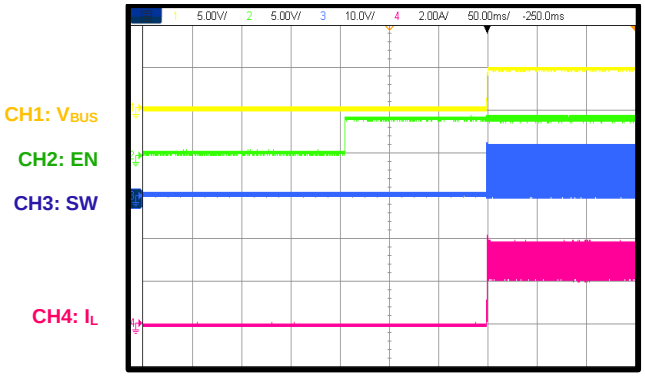
EN Pin Enabled

Load = 0A, CC1 with 5.1kΩ R_D resistor



EN Pin Enabled

Load = 3A, CC1 with 5.1kΩ R_D resistor

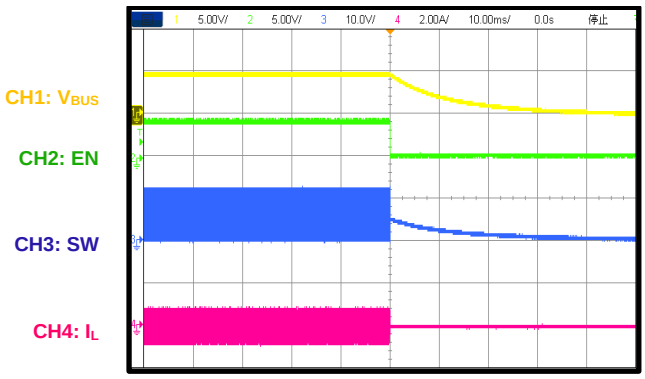


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{BUS} = 5V, L = 4.7µH, f_{SW} = 420kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

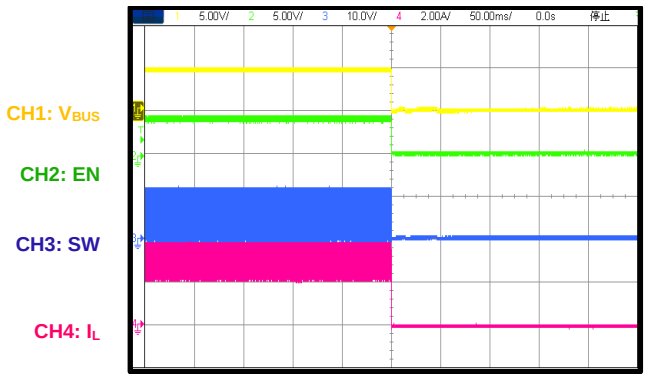
EN Pin Disabled

Load = 0A, CC1 with 5.1kΩ R_D resistor



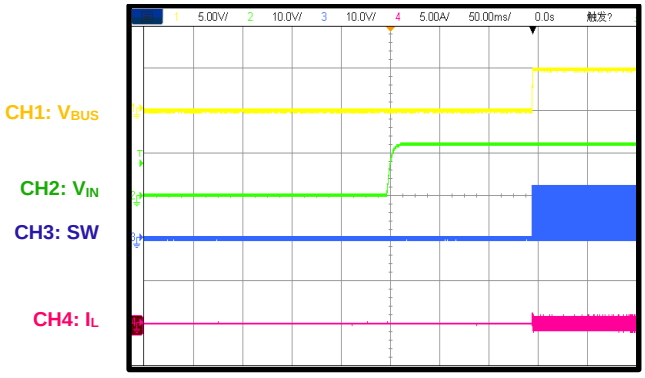
EN Pin Disabled

Load = 3A, CC1 with 5.1kΩ R_D resistor



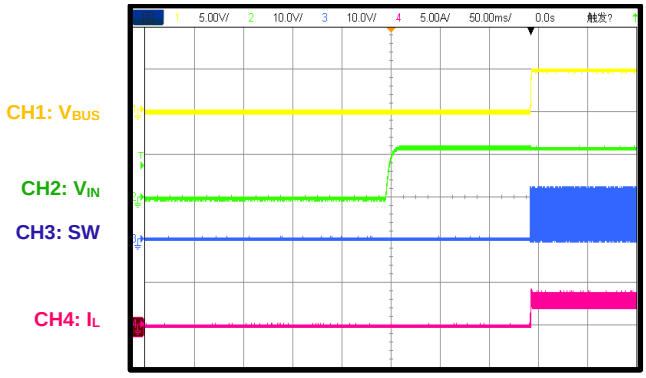
Input Start-Up

Load = 0A, CC1 with 5.1kΩ R_D resistor



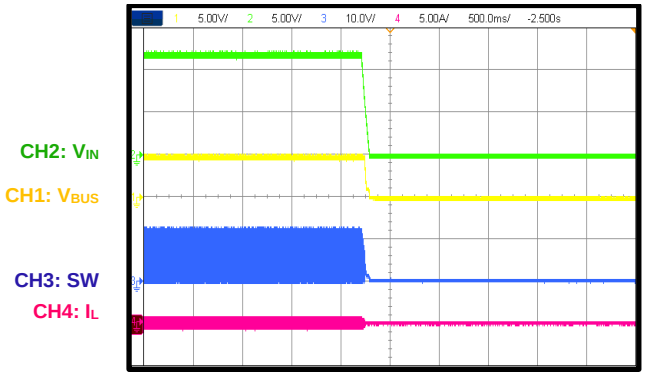
Input Start-Up

Load = 3A, CC1 with 5.1kΩ R_D resistor



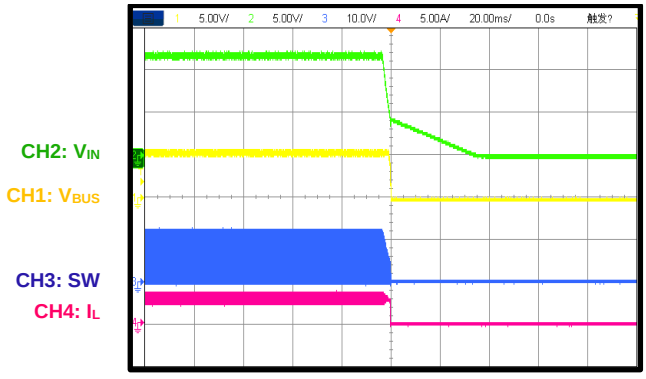
Input Shutdown

Load = 0A



Input Shutdown

Load = 3A

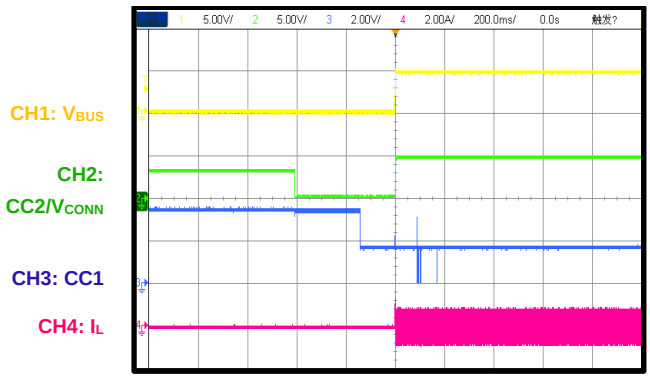


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{BUS} = 5V, L = 4.7µH, f_{SW} = 420kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

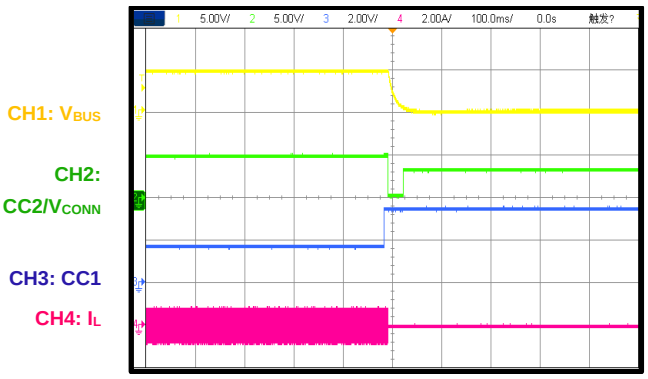
CC1 Attached R_D to Enable VBUS

I_{OUT} = 0A, CC2 with 1kΩ R_A resistor



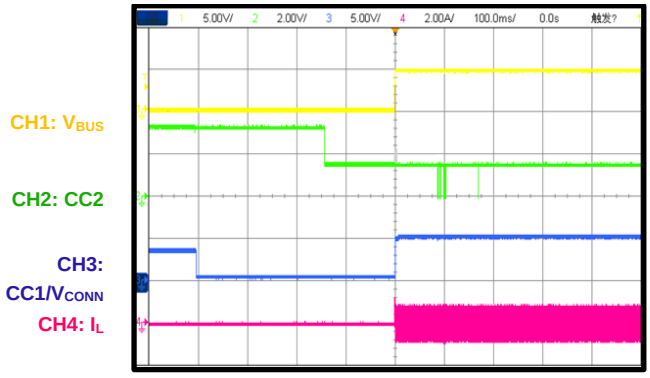
CC1 Detached R_D to Disable VBUS

I_{OUT} = 0A, CC2 with 1kΩ R_A resistor



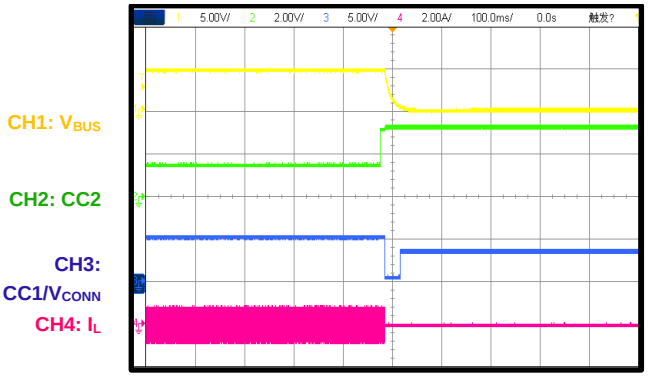
CC2 Attached R_D to Enable VBUS

I_{OUT} = 0A, CC1 with 1kΩ R_A resistor



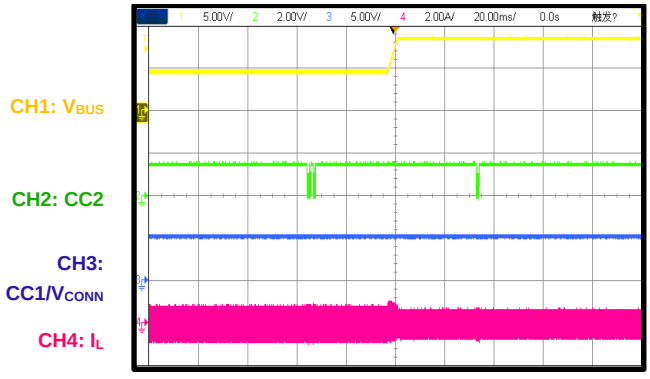
CC2 Detached R_D to Disable VBUS

I_{OUT} = 0A, CC1 with 1kΩ R_A resistor



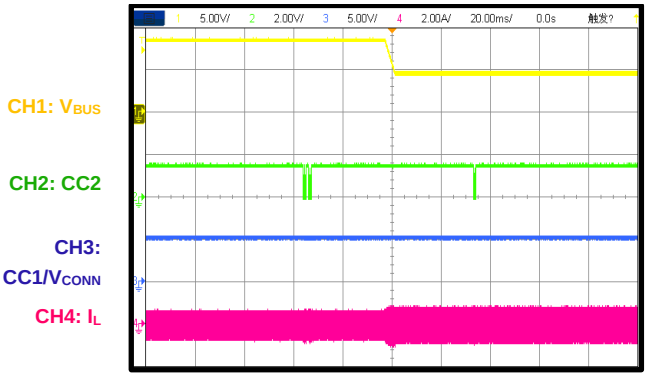
PDO Transition

5V PDO to 9V PDO



PDO Transition

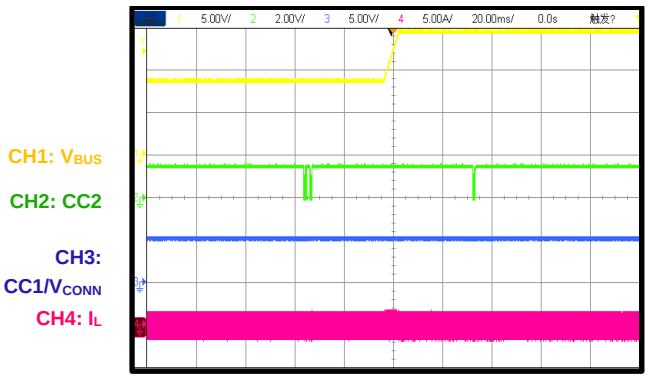
9V PDO to 5V PDO



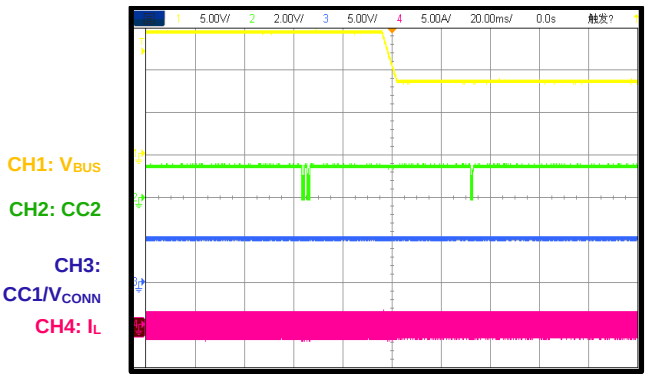
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{BUS} = 5V, L = 4.7µH, f_{SW} = 420kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

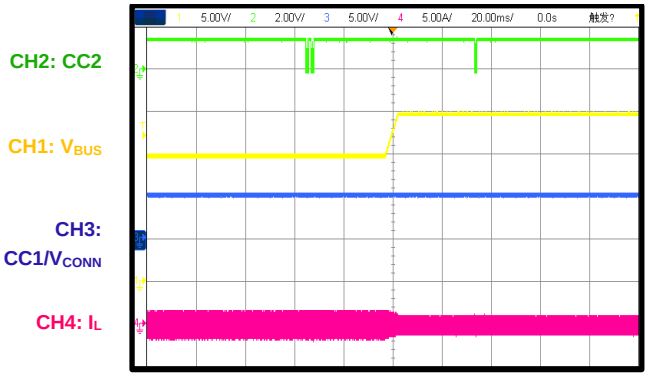
PDO Transition
V_{IN} = 24V, 9V PDO to 15V PDO



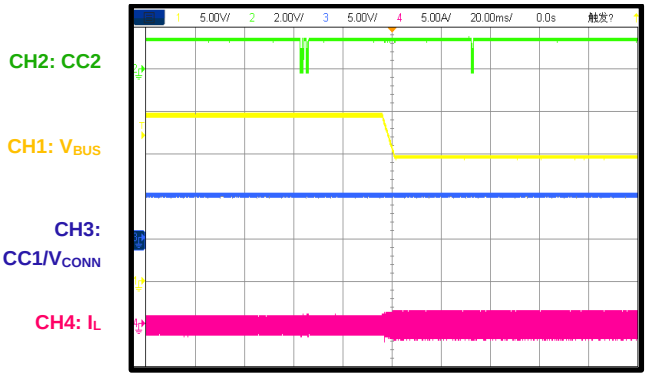
PDO Transition
V_{IN} = 24V, 15V PDO to 9V PDO



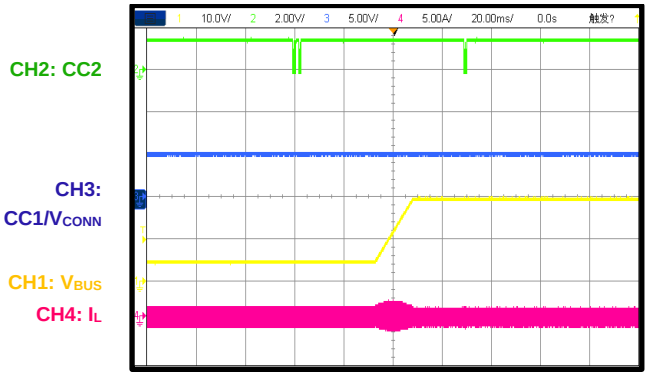
PDO Transition
15V PDO to 20V PDO



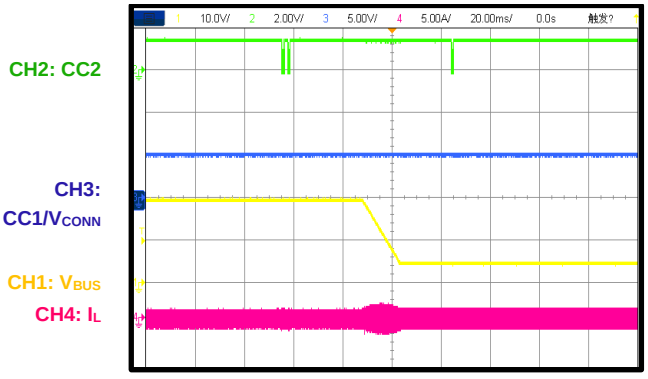
PDO Transition
20V PDO to 15V PDO



PDO Transition
5V PDO to 20V PDO



PDO Transition
20V PDO to 5V PDO

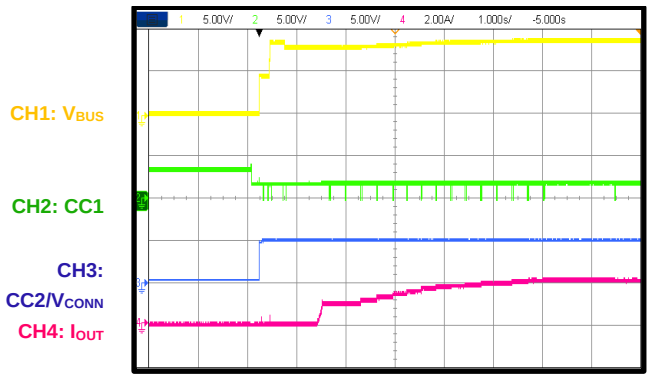


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{BUS} = 5V, L = 4.7µH, f_{SW} = 420kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

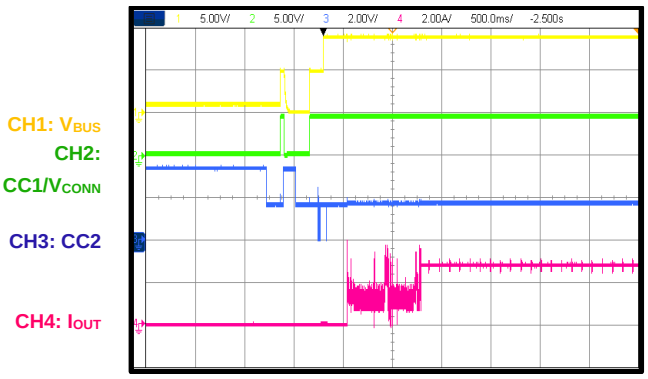
Mobile Phone Charging Test

V_{IN} = 12V, phone requests 9V PPS



Laptop Charging Test

V_{IN} = 12V, laptop requests 9V PDO



FUNCTIONAL BLOCK DIAGRAM

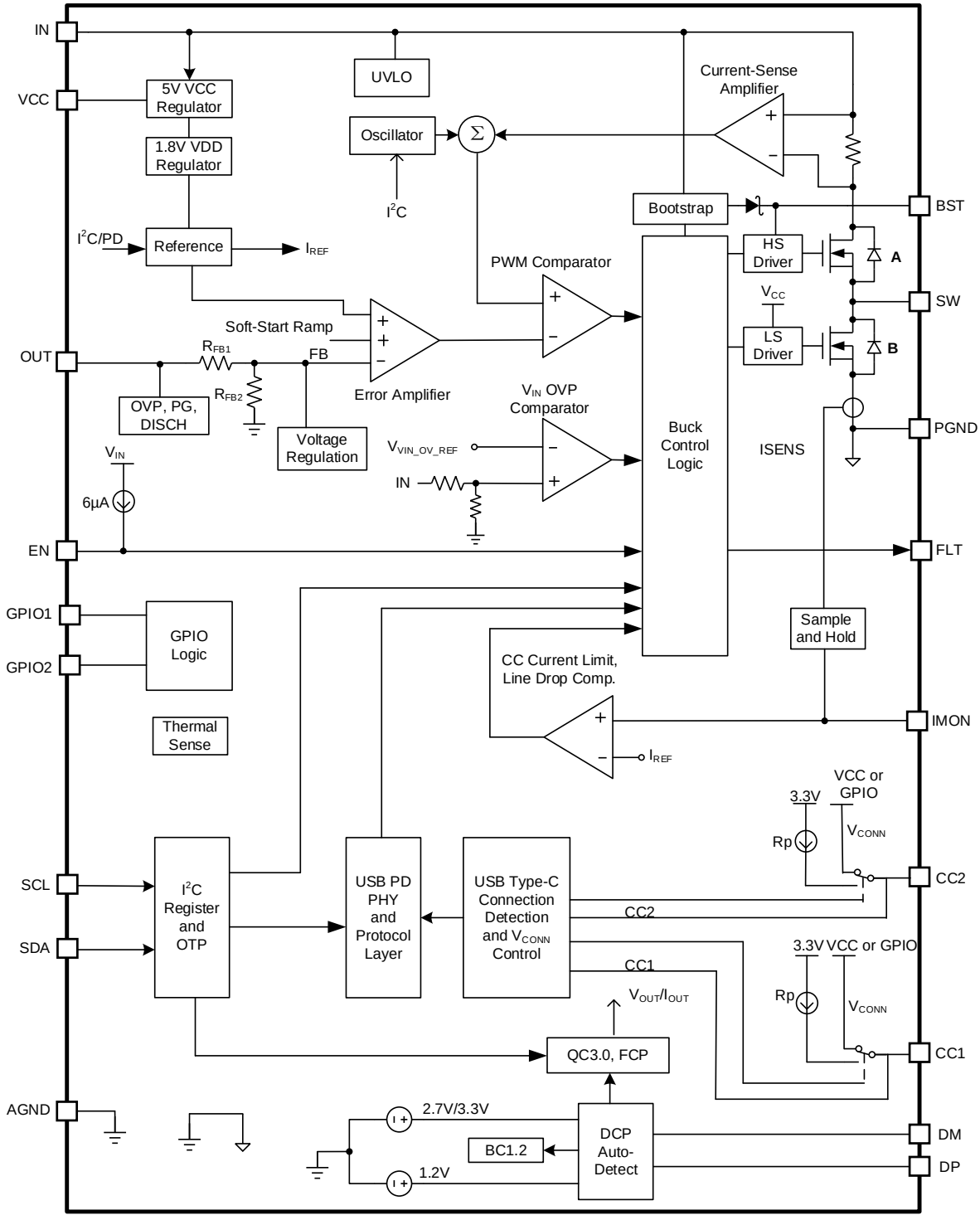


Figure 2: Functional Block Diagram

OPERATION

The MPQ4241 integrates a buck converter with integrated USB charging protocols. The buck converter works in current mode, which provides fast transient response. Figure 2 on page 20 shows the internal block diagram, and the sections below describe the device's functions in detail.

Pulse-Width Modulation (PWM) Operation

The MPQ4241 operates in a fixed-frequency, peak current mode control to regulate the output voltage (V_{OUT}). The internal clock initiates the pulse-width modulation (PWM) cycle, turning on the related power switch. The switch remains on until its current reaches the value set by the COMP voltage (V_{COMP}). When the power switch is off, it remains off until the next clock cycle starts. The user can configure the switching frequency (f_{SW}) to 250kHz, 420kHz, or 2200kHz via the I^2C.

The high-side MOSFET (HS-FET) works with the peak current mode control logic, and the low-side MOSFET (LS-FET) turns on as a complement to the HS-FET. In each cycle, the HS-FET turns on to charge the inductor current (I_L). The current-sense output voltage (V_{IL}) is proportional to I_L. When V_{IL} reaches V_{COMP}, the HS-FET turns off and the LS-FET turns on. The LS-FET stays on until the next clock comes, then the HS-FET turns on and the process repeats. The COMP signal is the output of the internal error amplifier (EA). Figure 3 shows the buck converter's operation waveform.

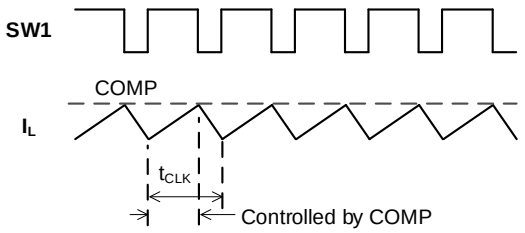


Figure 3: Buck Waveform

Low-Dropout Mode

If the input voltage (V_{IN}) drops close to V_{OUT}, the MPQ4241 enters low-dropout mode. The MPQ4241 starts extending its on time (t_{ON}) when the minimum off time is triggered, and the maximum t_{ON} is limited to 14µs. In low-dropout mode, V_{OUT} is equal to V_{IN} multiplied by the maximum duty cycle.

This function is disabled by default. Low-Dropout mode can be enabled via the factory OTP trim.

5V Internal VCC Regulator

The 5V internal regulator powers the CC pin's pull-up, the 100mW VCONN, and most of the internal logic circuitries. The regulator takes the VIN input and operates across the full V_{IN} range. When V_{IN} exceeds 5V, the regulator's output is in full regulation. If V_{IN} is below 5V, the output decreases with V_{IN}.

The VCC pin can support 0.1W of output power (P_{OUT}). The VCC pin requires a 1µF ceramic decoupling capacitor.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The MPQ4241's UVLO comparator monitors V_{IN}.

Internal Soft Start (SS)

Soft start prevents the converter's V_{OUT} from overshooting during start-up. When the chip starts, the internal circuitry generates a soft-start voltage (V_{SS}) that ramps up from 0V to 5V. When SS is below the reference voltage (V_{REF}), the error amplifier uses V_{SS} as the reference. When V_{SS} exceeds V_{REF}, the error amplifier uses V_{REF} as the reference. The SS time is internally set to 1ms for a 5V V_{OUT}.

If the output of the MPQ4241 is pre-biased to a certain voltage during start-up, the IC disables the switching of both the HS-FET and LS-FET until the voltage on the internal soft-start capacitor exceeds the internal feedback voltage.

Constant Current (CC) Mode Over-Current-Protection (OCP)

The MPQ4241 integrates a high-accuracy current limit. If the output current (I_{OUT}) exceeds the set current-limit threshold, the MPQ4241 enters constant current (CC) limit mode. In this mode, the current amplitude is limited.

If the MPQ4241 works in fixed power data object (PDO) mode, it sends a hard reset message once I_{OUT} exceeds the constant current limit. If the MPQ4241 works in augmented power data object (APDO) mode and continues to reduce the load resistance, V_{OUT} drops until it reaches

the under-voltage (UV) threshold, which is typically 3V falling (or 4.5V falling, as determined via the I²C). Once a UV condition is triggered, the MPQ4241 sends a hard reset message. If I_{OUT} still exceeds the OCP threshold, the MPQ4241 enters hiccup mode to periodically restart the part.

This protection mode is especially useful when the output is dead-shorted to ground. This operation greatly reduces the average short-circuit current, alleviates thermal issues, and protects the regulator. The MPQ4241 exits hiccup mode once the OC condition is removed.

The current limit threshold can be set from 1A to 6.35A (with a 50mA resolution) via the I²C.

Output Over-Voltage Protection (OVP)

The MPQ4241 has output over-voltage protection (OVP). If V_{OUT} exceeds 117% of V_{REF}, both the HS-FET and LS-FET turn off. The resistor discharge path connected from the OUT pin to ground turns on. When V_{OUT} drops to 107% of V_{REF}, the chip returns to normal operation.

The absolute output OVP threshold is about 23.5V. The discharge resistor turns on when absolute OVP is triggered.

Input Over-Voltage Protection (V_{IN} OVP)

The MPQ4241 has V_{IN} OVP. If V_{IN} exceeds the V_{IN} OVP rising threshold (typically 26.2V rising), the HS-FET and LS-FET turn off. The chip returns to normal operation when V_{IN} drops to the V_{IN} OVP falling threshold (typically 25.2V).

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection. The UVLO rising threshold is 2.2V with a hysteresis of 150mV. The BST capacitor voltage is regulated internally by VCC through D2, M1, and C4 (see Figure 4).

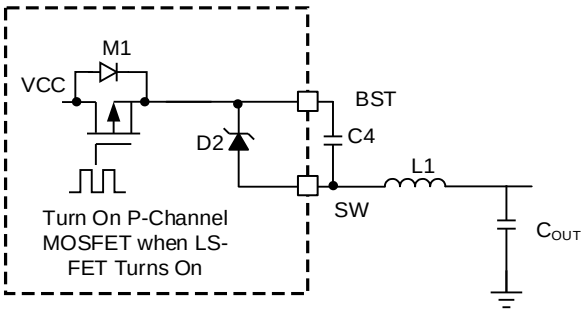


Figure 4: Internal Bootstrap Charging Circuit

Output Line Drop Compensation

The MPQ4241 is capable of compensating for a V_{OUT} drop.

If I_{OUT} is 0A, there is no compensation. If I_{OUT} is 3A and V_{OUT} exceeds 3V, the line drop compensation voltage is 150mV. For example, if the USB output current exceeds 3A, the line drop compensation voltage stays at 150mV and does not rise further. The line drop compensation value can be set to 150mV, 300mV, or 600mV via 0x18, bits[2:1]. Set 0x3C, bit[6] = 1 to enable an additional compensation voltage. Then the line drop compensation value can be set to 350mV, 500mV, or 800mV when the load is 3A.

Line drop compensation can be configured via the I²C or OTP. The compensated voltage is the same for all voltages.

For a default IC, line drop compensation is disabled once entering APDO mode. Line drop compensation can be enabled when the sink device requests APDO by setting 0x1F, bit[1].

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures.

When the silicon die temperature exceeds 170°C (which is set via the I²C), the whole chip shutdown. When the temperature falls below its lower threshold (typically 150°C), the chip is enabled again.

CHARGING MODE AUTO-DETECTION

Legacy USB 2.0 Mode

The MPQ4241 integrates the USB-dedicated charging port auto detect function that recognizes most mainstream portable devices. The device supports the following charging schemes:

- USB battery charging specification (BC1.2) / Chinese Telecommunications Industry Standard YD/T 1591-2009
- Apple 3A Divider Mode
- 1.2V/1.2V Mode
- QC 3.0
- Huawei FCP Class A

The automatic detection function is a state machine that supports all of the above DCP charging schemes. This function starts in 3A divider mode. If a device compliant to divider mode is connected, the MPQ4241 stays in divider mode. Meanwhile, 3.3V is applied to the DM pin, while 2.7V is applied to the DP pin.

If a BC 1.2 or YD/T 1591-2009 compliant device is attached, the MPQ4241 operates in 1.2V/1.2V and BC 1.2 DCP mode. DM and DP are shorted together with a resistance below 40Ω. The device then stays in this mode until the data line is released. If this occurs, the MPQ4241 returns to 3A divider mode.

When a QC 3.0 or FCP device (without PD protocol) is connected, the MPQ4241 can automatically enter high-voltage, quick charge mode.

If the USB PD contract is established after the sink is attached, the QC 3.0 and FCP functions are disabled.

USB Type-C Port (Complies to V2.1)

The USB Type-C receptacle, plug, and cable solution incorporates a configuration process to detect a downstream facing port (DFP) to upstream facing port (UFP) connection. This detection function is used for V_{BUS} management and can determine the host-to-device connection.

Initially, DFP-to-UFP attach is detected by a host (DFP) when one of the CC pins at its USB Type-C receptacle senses a specified resistance to GND. Subsequently, DFP-to-UFP detach is detected when the CC pin that was terminated at its USB Type-C receptacle is no longer terminated to GND.

Power is not applied to the USB Type-C host or hub receptacle (VBUS or VCONN) until the DFP detects the presence of a connected device (UFP) port. When a DFP-to-UFP connection is detected, the DFP is expected to enable power to the receptacle and proceed to normal USB operation with the connected device. When a DFP-to-UFP disconnect is detected, the port sourcing V_{BUS} removes power.

The MPQ4241's power supply capability is rated for 5V @ 3A by default. V_{CONN} is provided by the DFP to power cables with electronics that are plugged in. V_{CONN} is provided power over the CC pin that is not connected to the cable's CC wire. The maximum output power of V_{CONN} is 1W.

VCONN is disabled until R_A is detected. R_A is a pull-down resistor connected from the CC pin to GND. Its resistance must be below 1.2kΩ.

USB Power Delivery (PD) 3.1

In USB PD, pairs of directly connected ports negotiate the voltage, current, and/or the direction of power flow across the USB cable, using VBUS or the CC wire as the communication channel. The mechanisms used operate independently of other USB methods that negotiate power. USB Type-C connectors can support the CC wire as the communication channel (see Figure 5).

The USB PD engine can disable the clock and enter sleep mode if no PD command is detected. The input current is typically 150μA in sleep mode.

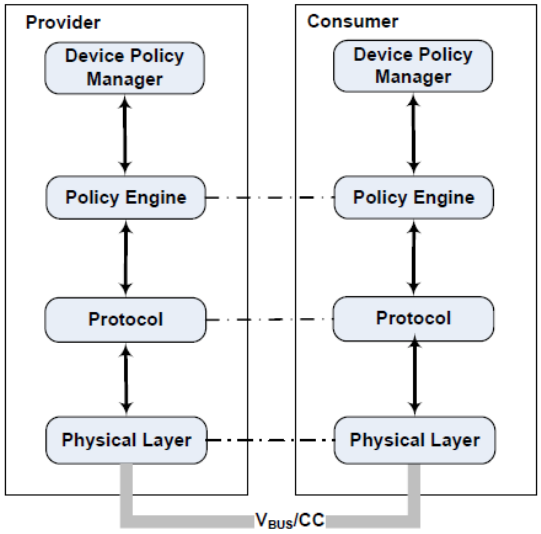


Figure 5: USB PD Communication Stack

The MPQ4241 supports certain functions and commands as a DFP (see Table 1 on page 24).

Table 1: Control Message

Transmitted Message	Received Message
ACCEPT	GET_PPS_STATUS
GET_STATUS	GET_STATUS
GOODCRC	GOODCRC
NOT_SUPPORTED	NOT_SUPPORTED
PS_RDY	REJECT
REJECT	SOFT_RESET
SOFT_RESET	HARD_RESET
HARD_RESET	VCONN_SWAP
-	GET_SOURCE_CAP
-	GET_SOURCE_CAP_ EXTENDED

Table 2 shows the data messages.

Table 2: Data Message

Transmitted Message	Received Message
SOURCE_CAPABILITIES	SINK_CAPABILITIES
BIST	REQUEST
ALERT	BIST
	ALERT

Table 3 shows the extended messages.

Table 3: Extended Message

Transmitted Message	Received Message
STATUS	-
PPS_STATUS	-
SOURCE_CAPABILITIES_ EXTENDED	-

Figure 6 shows the MPQ4241's device policy manager function block.

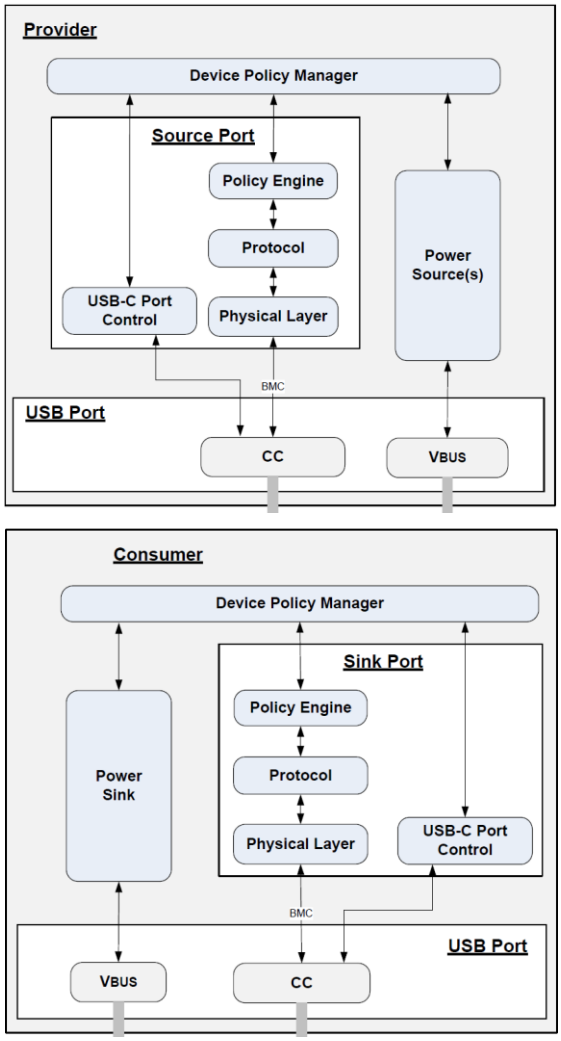


Figure 6: Device Policy Manager

Figure 7 shows a MPQ4241 PD contract handshake sequence.

#	CH	OS	Power	Data	Cable Plug	Type
0	CC2	SOP'			UFP or DFP	Vendor_Defined
1	CC2	SOP'			Cable Plug	GoodCRC
2	CC2	SOP'			Cable Plug	Vendor_Defined
3	CC2	SOP'			UFP or DFP	GoodCRC
4	CC2	SOP	Source	DFP		Source_Capabilities
5	CC2	SOP	Sink	UFP		GoodCRC
6	CC2	SOP	Sink	UFP		Request
7	CC2	SOP	Source	DFP		GoodCRC
8	CC2	SOP	Source	DFP		Accept
9	CC2	SOP	Sink	UFP		GoodCRC
10	CC2	SOP	Source	DFP		PS_RDY
11	CC2	SOP	Sink	UFP		GoodCRC

Figure 7: PD Contract Handshake

VCONN Power Supply

The integrated maximum VCONN power supply is 100mW. There is a power switch connected from VCC to VCONN with current limit.

During a VCONN short-to-ground event, the MPQ4241 turns off VCONN and all other functions continue to operate normally. For 1W VCONN applications, the external VCONN supply should be applied to GPIO2.

LED PWM Driver

The GPIO2 pin can be configured to be a PWM output or to drive an LED. By default, it is a 25kHz, 50% duty cycle PWM with a maximum 15mA capability.

The user can change the PWM duty cycle via the I^2C. It can be set from 5% to 100% with 1% resolution.

EN Off Timer

The MPQ4241 has a configurable EN off timer. When the EN pin is pulled low, the device operates with full functionality until the timer elapses. The maximum EN off delay is 120 minutes. If the EN pin is pulled high within the off timer, the counter is reset.

Current Monitor Output

The MPQ4241 senses the average load current through the internal-sense resistor, and it outputs one voltage signal on the IMON pin, which is a signal that is proportional to the load current. A 4.7nF + 4.7kΩ filter connected to the IMON pin is recommended (see Figure 8). The recommended minimum load that the IMON pin can recognize is 1A.

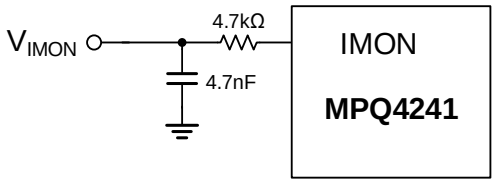


Figure 8: IMON Connection

The relationship between the IMON voltage and load current can be calculated with Equation (1):

$$V_{IMON} = Gain \times I_{OUT} \quad (1)$$

Where Gain is 260mV/A.

With a pulse-frequency modulation (PFM)/pulse-width modulation (PWM) mode set-up, the IMON pin can only work normally when the device enters continuous conduction mode (CCM).

NTC Function

When the GPIO2 pin is set to the NTC function, the device compares the NTC voltage to the internal reference. If the NTC voltage is below this threshold, the MPQ4241 enters thermal shutdown protection mode, or it reduces the PD power instead of shutting down (configurable via NTC_MODE).

If NTC_MODE = 1, then OTW2_NTC_PDP determines the value to which the PD power should be reduced. OTW2_NTC_PDO_SELECT sets which PDO voltage is enabled after entering NTC mode. Table 4 on page 27 shows the OTW2_NTC_PDO_SELECT function.

The device recovers to a normal state when the NTC exceeds the recovery threshold. The I^2C can set two different NTC recovery hysteresis values.

NTC2 Function

If GPIO1 is set to the NTC2 function, the device compares the NTC2 voltage to the internal reference. If the NTC2 voltage is below this threshold, the MPQ4241 triggers power sharing. If the power-sharing function is triggered, the PD power rating is reduced to the PS_PDP_THD setting. The PDO/APDO voltage and current are determined by Table 4 on page 27. The MPQ4241 exits the power-sharing status if the NTC2 voltage exceeds the recovery threshold. NTC_HYSTERESIS sets the hysteresis (it shares the same hysteresis as GPIO2 NTC).

The NTC_MODE, OTW2_NTC_PDO_SELECT, and OTW2_NTC_PDP bits do not control NTC2 behavior.

If the GPIO2 pin is set for the power-sharing function while GPIO1 is set for the NTC2 function, the MPQ4241 enters power-sharing mode when either NTC2 or GPIO2_POWER_SHARE is triggered.

Over-Temperature Warning (OTW) Function

The MPQ4241 senses its die temperature internally. If the chip temperature exceeds the over-temperature warning (OTW1) threshold, the MPQ4241 enters a state where it reduces the PD power state to the value set by OTW1_PDP. OTW1_PDO_SELECT sets which PDO voltage is enabled after entering OTW1 mode. Table 4 on page 27 shows the OTW_PDO_SELECT function.

If the die temperature continues increasing and triggers the second threshold (set via OTW2), the MPQ4241 reduces the PD power to the level set via OTW2_NTC_PDP. OTW2_NTC_PDO_SELECT sets which PDO voltage is enabled.

The IC recovers to a normal PD rating once it exits the OTW status.

NTC Sense for USB Type-C Connector (NTC_CNT)

When the GPIO1 or GPIO2 pin is set to the NTC_CNT function, the MPQ4241 senses the connector's temperature and reports it to the PD controller. In this scenario, it is recommended to use a 20kΩ pull-up resistor connected to VCC and a 100kΩ NTC resistor (NTCG064EF104FTDSX) when a coefficient of B = 4308. If the NTC_CNT temperature exceeds 145°C, the chip shuts down. The device recovers when the temperature falls below 125°C.

This function can be disabled via NTC_CNT_DISABLE (0x2D), bit[0] or the OTP.

SYNC_IN

When the GPIO1 pin is set to the SYNC_IN function, this pin accepts external clock in. The clock's frequency should be within ±20% of the base f_{SW} setting with a 10% to 90% duty cycle. To use external frequency synchronization on the GPIO1 pin, the external clock should match the internal f_{SW}; otherwise, f_{SW} may be abnormal. The SYNC_IN rising threshold is 1.7V, and the SYNC_IN signal should be below 5V.

Low Battery Operation

During the first V_{IN} start-up, the MPQ4241 is delayed for 1s before detecting V_{IN}.

If the MPQ4241 detects that the battery voltage (its VIN voltage) is below the VBATT_LOW_THLD1 falling threshold for the VBATT_LOW_BLK deglitch time, it reduces the PD power rating according to the set value. Meanwhile, VBATT_LOW1_FLAG is set. If there is a PD contract, the PD engine resends the updated PDO with a reduced PDP. The PDO list is determined by VBATT_L1_PDO_SELECT.

If the MPQ4241 detects that the battery voltage (its VIN voltage) is below the VBATT_LOW_THLD2 falling threshold for the VBATT_LOW_BLK deglitch time, it reduces the PD power rating according to the set value. Meanwhile, VBATT_LOW2_FLAG is set.

If there is a PD contract, the PD engine resends the updated PDO with a reduced PDP. The PDO list is determined by VBATT_L2_PDO_SELECT.

If the MPQ4241 detects that the battery voltage (its VIN voltage) is below the VBATT_LOW_THLD3 falling threshold for the VBATT_LOW_BLK deglitch time, the device shuts down.

When the battery voltage recovers and exceeds the VBATT_LOW_THLD rising threshold with a 1s digital deglitch time, the PDO recovers to a normal PDP.

If VBATT_LOW_THLD1 and VBATT_LOW_THLD2 events occur simultaneously, VBATT_LOW2 has a higher priority to set the PDO list.

There are three VBATT_LOW thresholds: VBATT_LOW_THLD1, VBATT_LOW_THLD2, and VBATT_LOW_THLD3. Accordingly, VBATT_LOW1_PDP and VBATT_LOW2_PDP define the PDP level to which the MPQ4241 should be reduced. During the MPQ4241's first start-up, the internal VBATT_LOW_FLAG default state is 0. The VBATT_LOW detection circuitry starts to work when the USB Type-C port is attached and reset by IC UVLO or EN shutdown.

POWER SHARE FUNCTION

GPIO1_POWER_SHARE

The GPIO1_POWER_SHARE pin can accept an external input voltage. If the second MPQ4241 (MPQ4241-B) detects that a valid sink is attached, the first MPQ4241's (MPQ4241-A) GPIO1_POWER_SHARE pin is pulled down by the MPQ4241-B's GPIO2_ATTACH pin (see Figure 9).

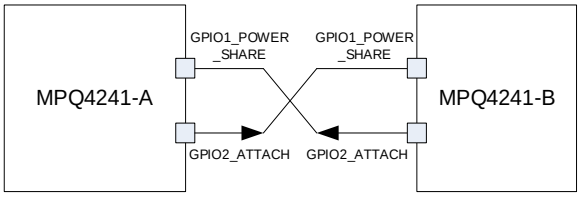


Figure 9: Power Share Connection between Two MPQ4241 Devices (e.g. Cut Total Power to 50%/50%)

When the power-sharing function is triggered, the PDO list and current are determined by PS_PDP_THD and PS_PDP_THD_PDO_SELECT.

Table 4 shows one example. For example, when in 3.3V to 21V APDO mode, the current rating is 45W/20V = 2.25A.

Table 4: PDO Voltage and Current Set Table Based on PS_PDP_THD and PS_PDP_THD_PDO_SEL

PDO List	5V Fixed	9V Fixed	12V Fixed	15V Fixed	20V Fixed	5V Prog.	9V Prog.	15V Prog.	20V Prog.
Output Current	PDP / 5 (8)	PDP / 9	PDP / 12	PDP / 15	PDP / 20 (9)	PDP / 5	PDP / 9	PDP / 11	PDP / 20 (9)
PS_PDP_THD_PDO_SEL Register Selection Bit (12)	-	1	0	1	1	1	1	0	0
Example: PS_PDP_THD = 22.5W	5V, 3A (10)	9V, 2.5A	-	15V, 1.5A	20V, 1.13A	3.3V to 5.9V, 3A (11)	3.3V to 11V, 2.5A	-	-

Notes:

8) 5V Fixed PDO is always enabled after entering power-sharing mode.
9) Fixed PDO's current equals to PDP/Voltage. The maximum current is 3A for <20V fixed PDOs. The maximum current can be 5A for APDOs.
10) The minimum PDP is 5V x 1.5A = 7.5W. R_P changes to 5V/1.5A when PDP < 15W.
11) The PPS current is calculated with PDP / 5V for 5V PPS, PDP / 9V for 9V PPS, PDP / 15V for 15V PPS, and PDP / 20V for 20V PPS.
12) PS_PDP_THD, PS_PDO_SELECT, VBATT_L1_PDO_SELECT, VBATT_L2_PDO_SELECT, OTW1_PDO_SELECT, and OTW2_NTC_PDO_SELECT share the same format. The gray cells are set by 8-bit register values.

GPIO2_POWER_SHARE_HIGH_ACTIVE

The GPIO2_POWER_SHARE_HIGH_ACTIVE threshold is V_{TH_PS} (1.2V in typical). When the GPIO2 pin is set to the GPIO2_POWER_SHARE_HIGH_ACTIVE function, and the MPQ4241-A detects that its GPIO2 voltage exceeds V_{TH_PS}, the power-sharing function is triggered. When the power-sharing function is triggered, the PDO list and current are determined by PS_PDP_THD and PS_PDP_THD_PDO_SELECT. Table 5 shows one example on this scenario; the notes in this table are the same as the notes for Table 4 above.

Table 5: PDO Voltage and Current Set Table Based on PS_PDP_THD and PS_PDP_THD_PDO_SEL

PDO List	5V Fixed	9V Fixed	12V Fixed	15V Fixed	20V Fixed	5V Prog.	9V Prog.	15V Prog.	20V Prog.
Output Current	PDP / 5 (8)	PDP / 9	PDP / 12	PDP / 15	PDP / 20 (9)	PDP / 5.9	PDP / 11	PDP / 16	PDP / 21 (9)
PS_PDP_THD_PDO_SEL Register Selection Bit (12)	-	1	0	0	0	1	1	0	0
For Example: PS_PDP_THD = 15W	5V, 3A (10)	9V, 1.6A	-	-	-	3.3V to 5.9V, 3A (11)	3.3V to 11V, 1.35A	-	-

The MPQ4241 exits the power-sharing status after the GPIO2 voltage drops below V_{TH_PS}. Figure 10 shows the GPIO2_POWER_SHARE_HIGH_ACTIVE connection block. When V_{BUS} > 11.2V, the power-sharing function is triggered. Table 6 on page 28 shows the PDP of the MPQ4241-A and MPQ4241-B in the GPIO2_POWER_SHARE_HIGH_ACTIVE function.

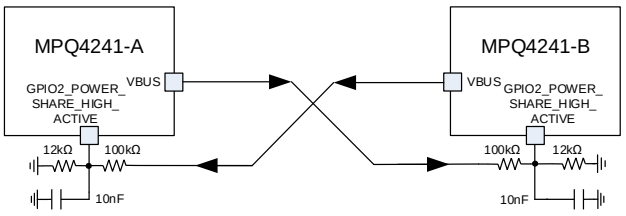


Figure 10: GPIO2 Power Share High Active Connection between Two MPQ4241 Devices

Table 6: GPIO2 Power Share PDP Management in Dual-Channel Application (13)

Column Format: <PD Contract W> (<Advertised Power W>)
Total Shared Power: 60W (14)
Each Port PDP: 45W

Condition	USB Type-C Port 1	USB Type-C Port 2	Total Power
1	-- (45W)	-- (45W)	--
2	15W (45W)	-- (45W)	15W
3	27W (45W)	-- (45W)	27W
4	45W (45W)	15W (15W)	60W
5	27W (45W)	15W (45W)	42W
6	27W (45W)	27W (45W)	54W
7	15W (15W)	45W (45W)	60W
8	-- (15W)	45W (45W)	45W
9	-- (45W)	27W (45W)	27W

Notes:

13) The PDP table is based on the GPIO2_POWER_SHARE set-up in Figure 10 on page 27.
14) Triggers power-sharing when the MPQ4241-B's V_{BUS} > 11.2V.

Figure 11 shows the PDP state machine.

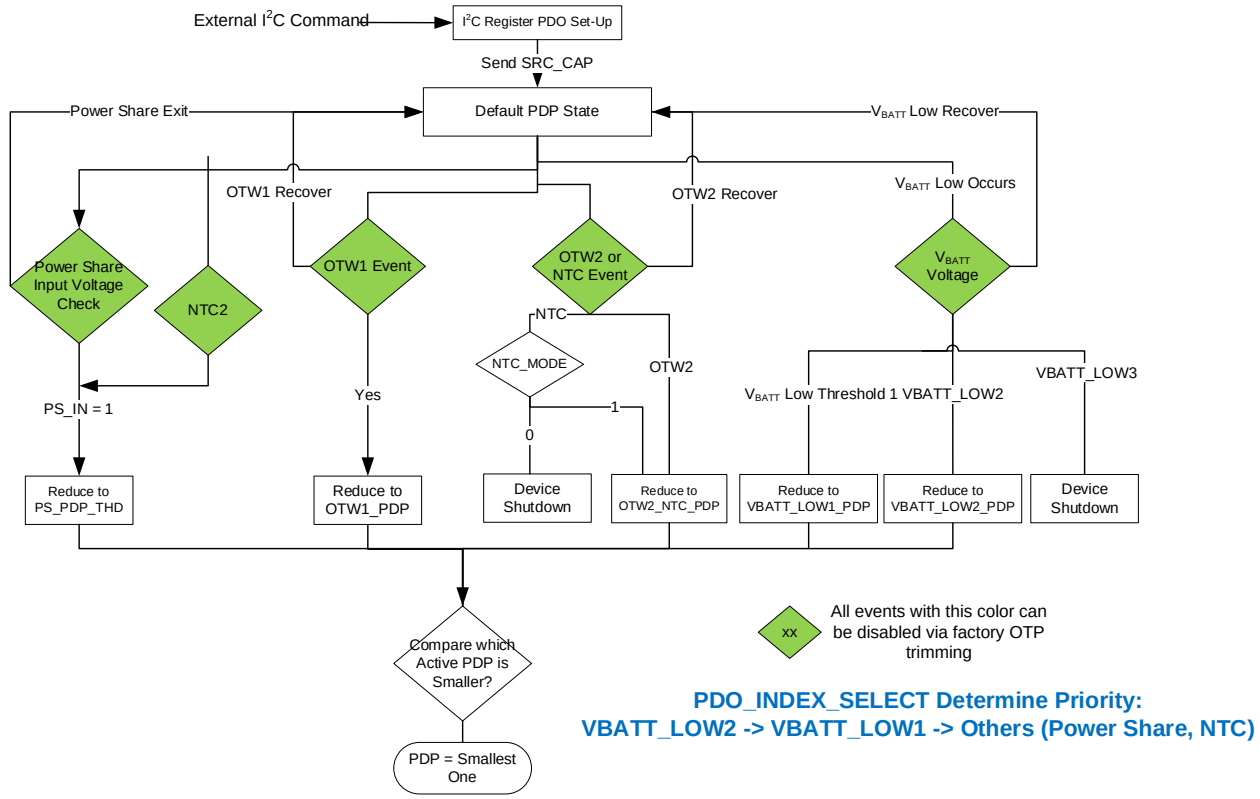


Figure 11: PDP State Machine (I²C Still Alive when NTC Shuts Down) (15)

Note:

15) If V_{BATT} is low and other PDP-decreasing events (e.g. NTC, power share, or OT warning) occur at the same time, the low V_{BATT} condition has a higher priority to determine the PDO_INDEX, but the PDP should be the minimum of {PS_PDP_THD, OTW1_PDP, OTW2_PDP, OTW2_NTC_PDP, VBATT_LOW1_PDP, VBATT_LOW2_PDP}.

Figure 12 on page 29 shows the PDP foldback scheme.

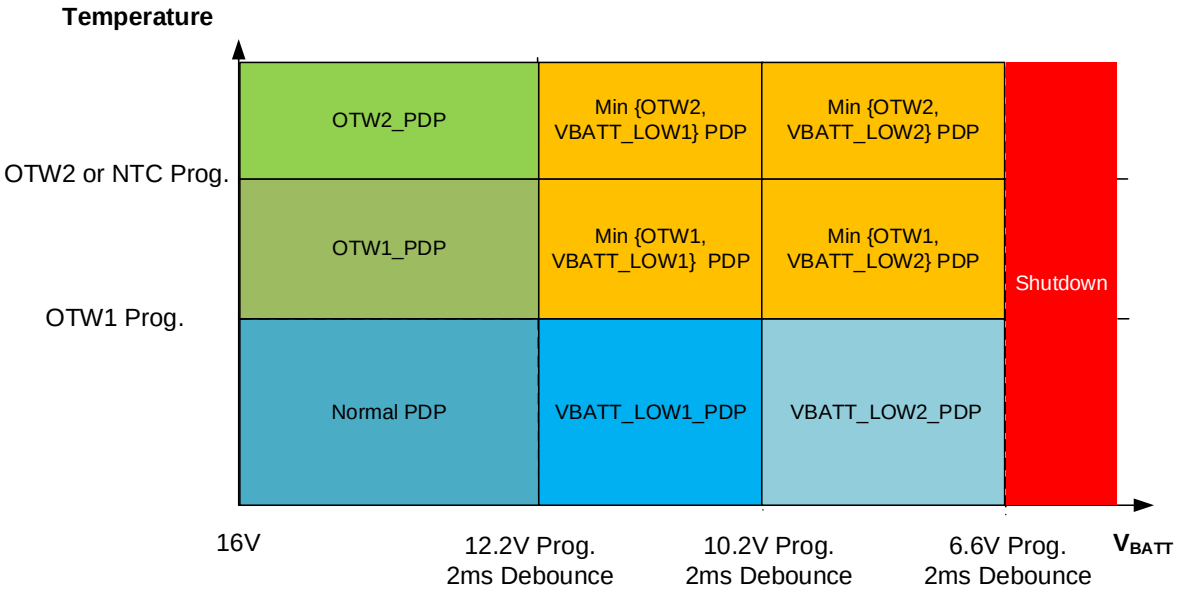


Figure 12: PDP Foldback Scheme

I²C INTERFACE

I²C Serial Interface Description

The I²C is a two-wire, bidirectional serial interface, consisting of a data line (SDA) and a clock line (SCL). The lines are externally pulled to a bus voltage when they are idle. Connecting to the line, a master device generates the SCL signal and device address and arranges the communication sequence.

The MPQ4241 interface is an I²C slave, which supports fast mode (400kHz). The I²C interface adds flexibility to the power supply solution. The output voltage, transition slew rate, or other parameters can be instantaneously controlled via the I²C interface. When the master sends the address as an 8-bit value, the 7-bit address should be followed by 0 or 1 to indicate a write or read operation, respectively.

Start and Stop Commands

The start and stop commands are signaled by the master device, which signifies the beginning and the end of the I²C transfer. The start command is defined as the SDA signal transitioning from high to low while the SCL is high. The stop command is defined as the SDA signal transitioning from low to high while the SCL is high (see Figure 13).

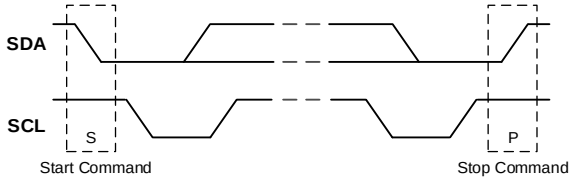


Figure 13: Start and Stop Commands

The master then generates the SCL clocks, and transmits the device address and the read/write (R/W) direction bit on the SDA line.

Data Transfer

Data is transferred in 8-bit bytes by the SDA line. Each byte of data must be followed by an acknowledge (ACK) bit.

I²C Update Sequence

The MPQ4241 requires a start command, a valid I²C address, a register address byte, and a data byte for a single data update. After receiving each byte, the MPQ4241 acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the MPQ4241. The MPQ4241 performs an update on the falling edge of the least significant bit (LSB) byte. Figure 14 shows a single register I²C write example. Figure 15 shows a multi-register I²C write example. Figure 16 on page 31 shows a single-register I²C read example.

I²C Start-Up Timing

The I²C function is enabled once V_{IN} > UVLO threshold, and EN is active.

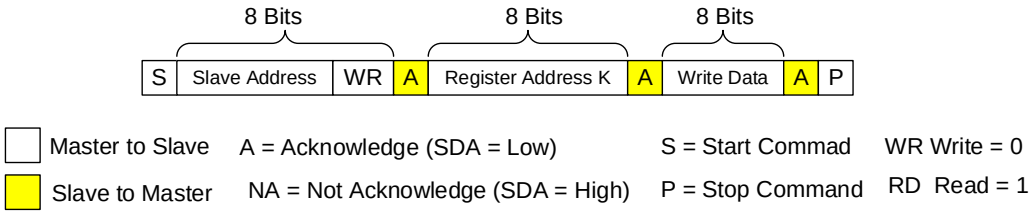


Figure 14: I²C Write Example (Write Single Register)

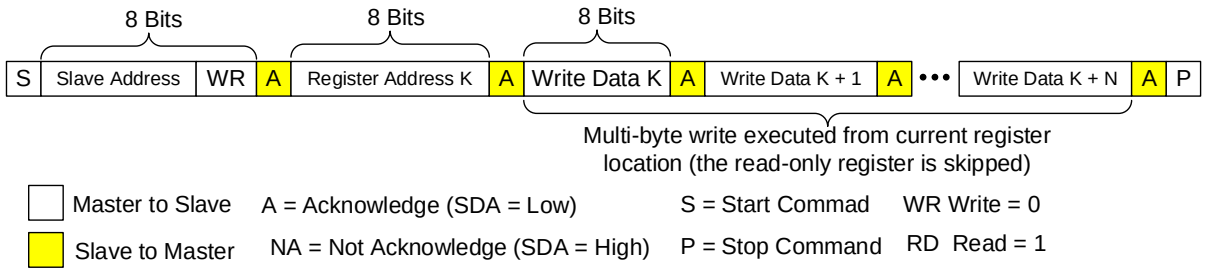


Figure 15: I²C Write Example (Write Multi-Register)

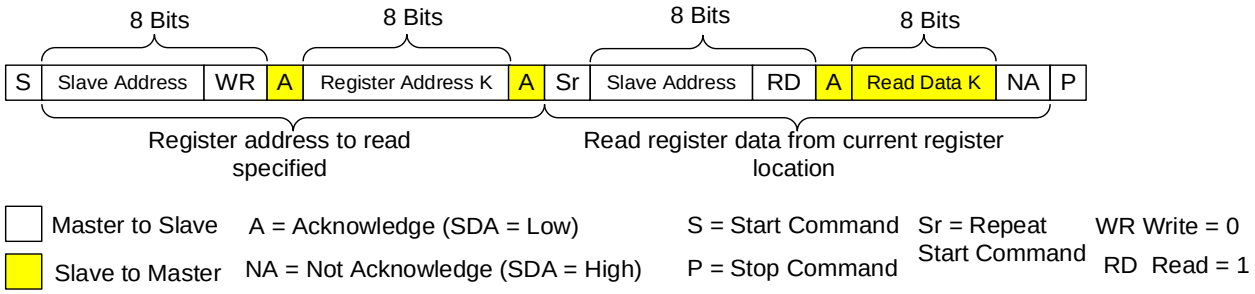


Figure 16: I²C Read Example (Read Single Register)

I²C REGISTER MAP

Add. (Hex)	Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
00	PDO_SET1	R/W	RESERVED	RESERVED	PDO7_EN (16)	PDO6_EN (16)	PDO5_EN (16)	PDO4_EN (16)	PDO3_EN (16)	PDO2_EN (16)
01	PDO_SET2	R/W	RESERVED	RESERVED	PDO7_TYPE (16)	PDO6_TYPE (16)	PDO5_TYPE (16)	PDO4_TYPE (16)	PDO3_TYPE (16)	PDO2_TYPE (16)
02	HOST_SET	R/W	COMMUNICA_CAPAB_HOST (16)	PRODUCT_TYPE_DFP (16)		HOST_CAPABILITY (000b) (16)			PORT_NUMBER (16)	
03	PDO_I1	R/W	PDO1_CURRENT_SETTING (16) (3A Default)							
04	PDO_V2_L	R/W	PDO2_VOLTAGE_SETTING_LOW_BYTE (16) (9V Default)							
05	PDO_V2_H	R/W	PDO2_VOLTAGE_SETTING_HIGH_BYTE (16) (0x00)							
06	PDO_I2	R/W	PDO2_CURRENT_SETTING (16) (3A Default)							
07	PDO_V3_L	R/W	PDO3_VOLTAGE_SETTING_LOW_BYTE (16) (15V Default)							
08	PDO_V3_H	R/W	PDO3_VOLTAGE_SETTING_HIGH_BYTE (16) (0x00)							
09	PDO_I3	R/W	PDO3_CURRENT_SETTING (16) (3A)							
0A	PDO_V4_L	R/W	PDO4_VOLTAGE_SETTING_LOW_BYTE (16) (20V Default)							
0B	PDO_V4_H	R/W	PDO4_VOLTAGE_SETTING_HIGH_BYTE (16) (0x00)							
0C	PDO_I4	R/W	PDO4_CURRENT_SETTING (16) (3A)							
0D	PDO_V5_L	R/W	PDO5 VOLTAGE SETTING LOW BYTE (16) (3.3V)							
0E	PDO_V5_H	R/W	PDO5 VOLTAGE SETTING HIGH BYTE (16) (11V)							
0F	PDO_I5	R/W	PDO5_CURRENT_SETTING (16) (3A)							
10	PDO_V6_L	R/W	PDO6_VOLTAGE_SETTING_LOW_BYTE (16) (3.3V)							
11	PDO_V6_H	R/W	PDO6_VOLTAGE_SETTING_HIGH_BYTE (16) (16V)							
12	PDO_I6	R/W	PDO6_CURRENT_SETTING (16) (3A)							
13	PDO_V7_L	R/W	PDO7_VOLTAGE_SETTING_LOW_BYTE (16) (3.3V)							
14	PDO_V7_H	R/W	PDO7 VOLTAGE SETTING_HIGH_BYTE (16) (21V)							
15	PDO_I7	R/W	PDO7_CURRENT_SETTING (16) (3A)							
16	PD_CTL1	R/W	TYPE_C_1P5 (16)	LEGACY_CHARGING_MODE_SEL (16)		USBCOMMUNICATE (16)	NTC_CTL_RP (16)	TOUCH_TEMP (16)		I2C_CTL_VOUT_EN (16)
17	PD_CTL2	R/W	HDRST	USBSUSPEND (16)	TOUCH_CURRENT (16)			COMPLIANCE (16)		
18	PWR_CLT1	R/W	EN (16)	MODE (16)	FREQ (16)		DITHER (16)	LINE_DROP_COMP (16)		SLEW_RATE (16)
19	PWR_CLT2	R/W	EN_VBUS (16)	PPS_MIN_SEL (16)	OTW1_THRESHOLD (16)			TSD_THRESHOLD (16)		
1A	VOUT_L	R/W	RESERVED ALL “0”					VOUT_L bits[2:0] (16)		
1B	VOUT_H	R/W	VOUT_H bits[10:3] (16) (use this as the default DAC V_{REF})							
1C	IOUT_LIM	R/W	GO_BIT	OUTPUT_CURRENT_LIMIT_THRESHOLD (1A to 6.35A/50mA step) (16)						
1D	CTL_SYS0	R/W	PDO_CURRENT_PLUS10MA (for fixed PDO only) (16)							
1E	CTL_SYS1	R/W	SEND_SRC_CAP	EN_OFF_TIMER (16)			I2C_SLAVE_ADDRESS (A4:A1) (16)			
1F	CTL_SYS2	R/W	GPIO1 (16)			GPIO2 (16)				LDC_EN_PPS (16)
20	CTL_SYS3	R/W	PS_PDP_THD (16) (PDP reduced after power-sharing)							
21	CTL_SYS4	R/W	PS_PDP_THD_PDO_SELECT (16)							
22	CTL_SYS5	R/W	RESERVED	PPS_3A_5A (16)	CC_BLANK_TIMER (16)		RESERVED		PD_CAP_PEAK_CURRENT (16)	
23	CTL_SYS6	R/W	VBATT_LOW1_PDP (16)							
24	CTL_SYS7	R/W	VBATT_L1_PDO_SELECT (16)							
25	CTL_SYS8	R/W	VBATT_LOW2_PDP (16)							
26	CTL_SYS9	R/W	VBATT_L2_PDO_SELECT (16)							

I²C REGISTER MAP *(continued)*

Add. (Hex)	Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
27	CTL_SYS10	R/W	OTW1_PDP (16)							
28	CTL_SYS11	R/W	OTW1_PDO_SELECT (16)							
29	CTL_SYS12	R/W	OTW2_NTC_PDP (16)							
2A	CTL_SYS13	R/W	OTW2_NTC_PDO_SELECT (16)							
2B	CTL_SYS14	R/W	VBATT_LOW_THLD1 (16)	VBATT_LOW_THLD2 (16)						
2C	CTL_SYS15	R/W	VBATT_LOW_THLD3 (16)	VBATT_LOW_BLK (16)		RESERVED				
2D	CTL_SYS16	R/W	SLOW_SW (16)		RESERVED	OTW_HYSTERESIS (16)	OTW2_THRESHOLD*			NTC_CNT_DISABLE (16)
2E	CTL_SYS17	R/W	PEAK_CL (16)		RESERVED	NTC_HYSTERESIS (16)	NTC_MODE (16)	RESERVED	VBUS_VOLTAGE (16)	
2F	CTL_SYS18	R/W	OTP_PROGRAM	LED_PWM_DUTY (16)						
30	STATUS1	R	ATTACHED	NTC2_ENTER	PG	SHORT_VBATT	TSD	OTP_PAGE	CC_CV	NTC_ENTER
31	STATUS2	R	VBATT_LOW1_FLAG	VBATT_LOW2_FLAG	OTW1	OTW2	SELECTED_PDO_INDEX			PDO_TYPE
32	STATUS3	R	POL	FAULT	PD_VALID	QC_VALID	RESERVED			OUT_OVP
33	STATUS4	R	CONTRACT_POWER (CP)							
34	ID1	R	OTP_SUFFIX_CODE (OTP configure code, where “0x00” means the standard MPQ4241-0000, and “0x01” means the MPQ4241-0001 part number (16))							
35	ID2	R	OTP_SOFTWARE_REVISION_NO (16)							
36	FW_REV	R	MISMATCH	GIVEBACK_FLAG	CABLE_CAP	FIRMWARE_REVISION				
37	MAX_REQ_CUR	R	MAX_REQ_CUR (Maximum requested operation current where MISMATCH = 1 in 20mA unit, only valid when GIVEBACK flag = 0. Fixed PDO.)							
38	MFR_ID	R	MANUFACTURER_ID (where “0000 1001b” (16))							
39	DEV_ID	R	DEVICE_ID (where “0101 1000b” (16))							
3B	CLK_ON	W	CLOCK_ON (Write “1b” to enable clock, write “0b” to disable clock.)							
3C	CTL_SYS19	W	CTR_VCONN (16)	ADDITIONAL_LINE_DROP_COMPENSATION (16)	RESERVED					

Note:

16) This register can be configured via the one-time programmable (OTP) memory.

REGISTER DESCRIPTION

The default register value is based on MPQ4241-0000.

PDO_SET1 (00h)

Format: Unsigned binary

The PDO_SET1 command enables PDOx (where *x* = 2–7). PDO1 is fixed as a 5V power data object (PDO), and it is always enabled. Its voltage can be changed via VBUS_VOLTAGE.

Bits	Access	Bit Name	Default	Description
D[5]	R/W	PDO7_EN	1'b 1	Enables the PDO7's power object setting. 1'b 0: Disabled 1'b 1: Enabled
D[4]	R/W	PDO6_EN	1'b 1	Enables the PDO6's power object setting. 1'b 0: Disabled 1'b 1: Enabled
D[3]	R/W	PDO5_EN	1'b 1	Enables the PDO5's power object setting. 1'b 0: Disabled 1'b 1: Enabled
D[2]	R/W	PDO4_EN	1'b 1	Enables the PDO4's power object setting. 1'b 0: Disabled 1'b 1: Enabled
D[1]	R/W	PDO3_EN	1'b 1	Enables the PDO3's power object setting. 1'b 0: Disabled 1'b 1: Enabled
D[0]	R/W	PDO2_EN	1'b 1	Enables the PDO2's power object setting. 1'b 0: Disabled 1'b 1: Enabled

PDO_SET2 (01h)

Format: Unsigned binary

The PDO_SET2 command configures PDOx (where *x* = 2–7) to be fixed PDO or APDO.

Bits	Access	Bit Name	Default	Description
D[5]	R/W	PDO7_TYPE	1'b 1	Sets the PDO7's power object. 1'b 0: Fixed PDO 1'b 1: APDO
D[4]	R/W	PDO6_TYPE	1'b 1	Sets the PDO6's power object. 1'b 0: Fixed PDO 1'b 1: APDO
D[3]	R/W	PDO5_TYPE	1'b 1	Sets the PDO5's power object. 1'b 0: Fixed PDO 1'b 1: APDO
D[2]	R/W	PDO4_TYPE	1'b 0	Sets the PDO4's power object. 1'b 0: Fixed PDO 1'b 1: APDO

D[1]	R/W	PDO3_TYPE	1’b 0	Sets the PDO3’s power object. 1’b 0: Fixed PDO 1’b 1: APDO
D[0]	R/W	PDO2_TYPE	1’b 0	Sets the PDO2’s power object. 1’b 0: Fixed PDO 1’b 1: APDO

HOST_SET (02h)

Format: Unsigned binary

The HOST_SET command controls certain functions.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	COMMUNICA_ CAPAB _HOST	1’b 0	Sets the USB communication capabilities for the USB host. The default is 0b. 0b: Other 1b: The product can enumerate USB devices
D[6:5]	R/W	PRODUCT_TYPE_ DFP	2’b 11	Sets the product type (DFP). 00b: Undefined 01b: PDUSB hub 10b: PDUSB host 11b: Power brick
D[4:2]	R/W	HOST_CAPABILITY	3’b 000	Sets the DFP VDO message’s B26…24 content. The default is 000b. 000b: USB2.0 host capable 010b: USB3.2 host capable 100b: USB4 host capable
D[1:0]	R/W	PORT_NUMBER	2’b 01	Sets the unique port number to identify a specific port on a multi-port device. The default is 01b.

PDO_I1 (03h)

Format: Unsigned binary

The PDO_I1 command sets PDO1’s maximum output current.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	PDO1_CURRENT_ SETTING	8’b 10010110	Sets PDO1’s maximum output current setting in 20mA units. The default is 8’b 10010110, which is equal to 0x96 (3A). When these bits are set to exceed 3A, the MPQ4241 checks the cable current rating first. If it is 5A, then send the >3A setting; if the cable is 3A, only send a 3A maximum current capability.

PDO_V2_L (04h)

Format: Unsigned binary

If the PDO2_TYPE is set to 0b (fixed PDO), the PDO_V2_L command sets PDO2’s output voltage. The default for PDO2_TYPE is 0b.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	PDO2_VOLTAGE_ SETTING	8’b 01011010	Sets PDO2’s output voltage in 100mV units. The default is 8’b 01011010, which is equal to 0x5A (9V). The maximum voltage that can be set is 22.97V.

If PDO2_TYPE is set to 1b (APDO), the PDO_V2_L command sets PDO2's minimum output voltage.

Bits	Access	Bit Name	Description
D[7:0]	R/W	PDO2_MINIMUM	Sets PDO2's minimum voltage in 100mV increments. This function is not enabled with the MPQ4241-0000 code.

PDO_V2_H (05h)

Format: Unsigned binary

If PDO2_TYPE is set to 1b (APDO), the PDO_V2_H command sets PDO2's maximum output voltage.

Bits	Access	Bit Name	Description
D[7:0]	R/W	PDO2_MAXIMUM	Sets PDO2's maximum voltage in 100mV increments. This function is not enabled with the MPQ4241-0000 code.

PDO_I2 (06h)

Format: Unsigned binary

The PDO_I2 command sets PDO2's maximum output current.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	PDO2_CURRENT_ SETTING	8'b 10010110	Sets PDO2's maximum output current setting in 20mA units for fixed PDO, or 50mA units for APDO (PPS). The default is 8'b 10010110, which is equal 0x96 (3A and fixed PDO). When these bits are set to exceed 3A, the MPQ4241 checks the cable current rating first. If it is 5A, then send the >3A setting; if the cable is 3A, only send a 3A maximum current capability.

PDO_V3_L (07h)

Format: Unsigned binary

If PDO3_TYPE is set to 0b (fixed PDO), the PDO_V3_L command sets PDO3's output voltage. The default for PDO3_TYPE is 0b.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	PDO3_VOLTAGE_ SETTING	8'b 10010110	Sets PDO3's output voltage in 100mV units. The default is 8'b 10010110, which is equal to 0x96 (15V). The maximum voltage that can be set is 22.97V.

If PDO3_TYPE is set to 1b (APDO), the PDO_V3_L command sets PDO3's minimum output voltage

Bits	Access	Bit Name	Description
D[7:0]	R/W	PDO3_MINIMUM_ VOLTAGE	Sets PDO3's minimum voltage in 100mV increments. This function is not enabled with the MPQ4241-0000 code.

PDO_V3_H (08h)

Format: Unsigned binary

If PDO3_TYPE is set to 1b (APDO), the PDO_V3_H command sets PDO3's maximum output voltage.

Bits	Access	Bit Name	Description
D[7:0]	R/W	PDO3_MAXIMUM_ VOLTAGE	Sets PDO3's maximum voltage in 100mV increments. This function is not enabled with the MPQ4241-0000 code.

PDO_I3 (09h)

Format: Unsigned binary

The PDO_I3 command sets PDO3's maximum output current.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	PDO3_CURRENT_ SETTING	8'b 10010110	Sets PDO3's maximum output current setting in 20mA units for fixed PDO, or 50mA units for APDO (PPS). The default is 8'b 10010110, which is equal to 0x96 (3A). When these bits are set to exceed 3A, the MPQ4241 checks the cable current rating first. If it is 5A, then send the >3A setting; if the cable is 3A, only send a 3A maximum current capability.

PDO_V4_L (0Ah)

Format: Unsigned binary

If PDO4_TYPE is set to 0b (fixed PDO), the PDO_V4_L command sets PDO4's output voltage. The default for PDO4_TYPE is 0b.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	PDO4_VOLTAGE_ SETTING	8'b 11001000	Sets PDO4's output voltage in 100mV units. The default is 8'b 11001000, which is equal to 0xC8 (20V). The maximum voltage that can be set is 22.97V.

If PDO4_TYPE is set to 1b (APDO), the PDO_V4_L command sets PDO4's minimum output voltage.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	PDO4_MINIMUM_ VOLTAGE	N/A	Sets PDO4's minimum voltage in 100mV increments. This function is not enabled with the MPQ4241-0000 code.

PDO_V4_H (0Bh)

Format: Unsigned binary

If PDO4_TYPE is set to 1b (APDO), the PDO_V4_H command sets PDO4's maximum output voltage.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	PDO4_MAXIMUM_ VOLTAGE	N/A	Sets PDO4's maximum voltage in 100mV increments. This function is not enabled with the MPQ4241-0000 code.

PDO_I4 (0Ch)

Format: Unsigned binary

The PDO_I4 command sets PDO4's maximum output current.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	PDO4_CURRENT_ SETTING	8'b 10010110	Sets PDO4's maximum output current setting in 20mA units for fixed PDO, or 50mA units for APDO (PPS). The default is 8'b 10010110, which is equal to 0x96 (3A). When these bits are set to exceed 3A, the MPQ4241 checks the cable current rating first. If it is 5A, then send the >3A setting; if the cable is 3A, only send a 3A maximum current capability.

PDO_V5_L (0Dh)

Format: Unsigned binary

If PDO5_TYPE is set to 0b (fixed PDO), the PDO_V5_L command sets PDO5's output voltage. The default for PDO5_TYPE is 1b.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	PDO5_VOLTAGE_ SETTING	N/A	Sets PDO5's output voltage in 100mV units. This function is not enabled with the MPQ4241-0000 code.

If PDO5_TYPE is set to 1b (APDO), the PDO_V5_L command sets PDO5's minimum output voltage.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	PDO5_MINIMUM_ VOLTAGE	8'b 00100001	Sets PDO5's minimum voltage in 100mV increments. The default is 8'b 00100001, which is equal to 0x21 (3.3V).

PDO_V5_H (0Eh)

Format: Unsigned binary

If PDO5_TYPE is set to 1b (APDO), the PDO_V5_H command sets PDO5's maximum output voltage.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	PDO5_MAXIMUM_ VOLTAGE	8'b 01101110	Sets PDO5's maximum voltage in 100mV increments. The default is 8'b 01101110, which is equal to 0x6E (11V).

PDO_I5 (0Fh)

Format: Unsigned binary

The PDO_I5 command sets PDO5's maximum output current.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	PDO5_CURRENT_ SETTING	8'b 00111100	Sets PDO5's maximum output current setting in 20mA units for fixed PDO, or 50mA units for APDO (PPS). The default is 8'b 00111100, which is equal to 0x3C (3A). When these bits are set to exceed 3A, the MPQ4241 checks the cable current rating first. If it is 5A, then send the >3A setting; if the cable is 3A, only send a 3A maximum current capability.

PDO_V6_L (10h)

Format: Unsigned binary

If PDO6_TYPE is set to 0b (fixed PDO), the PDO_V6_L command sets PDO6's output voltage. The default for PDO6_TYPE is 1b.

Bit	Access	Bit Name	Default	Description
D[7:0]	R/W	PDO6_VOLTAGE_ SETTING	N/A	Sets PDO6's output voltage in 100mV units. This function is not enabled with the MPQ4241-0000 code.

If PDO6_TYPE is set to 1b (APDO), the PDO_V6_L command sets PDO6's minimum output voltage.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	PDO6_MINIMUM_ VOLTAGE	8'b 00100001	Sets PDO6's minimum voltage in 100mV increments. The default is 8'b 00100001, which is equal to 0x21 (3.3V).

PDO_V6_H (11h)

Format: Unsigned binary

If PDO6_TYPE is set to 1b (APDO), the PDO_V6_H command sets PDO6's maximum output voltage.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	PDO6_MAXIMUM_ VOLTAGE	8'b 10100000	Sets PDO6's maximum voltage in 100mV increments. The default is 8'b 10100000, which is equal to 0xA0 (16V).

PDO_I6 (12h)

Format: Unsigned binary

The PDO_I6 command sets PDO6's maximum output current.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	PDO6_CURRENT_ SETTING	8'b 00111100	Sets PDO6's maximum output current setting in 20mA units for fixed PDO, or 50mA units for APDO (PPS). The default is 8'b 00111100, which is equal to 3A at APDO. When these bits are set to exceed 3A, the MPQ4241 checks the cable current rating first. If it is 5A, then send the >3A setting; if the cable is 3A, only send a 3A maximum current capability.

PDO_V7_L (13h)

Format: Unsigned binary

If PDO7_TYPE is set to 0b (fixed PDO), the PDO_V7_L command sets PDO7's output voltage. The default for PDO7_TYPE is 1b.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	PDO7_VOLTAGE_ SETTING	N/A	Sets the PDO7's output voltage in 100mV units. This function is not enabled with the MPQ4241-0000 code.

If PDO7_TYPE is set to 1b (APDO), the PDO_V7_L command sets PDO7's minimum output voltage.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	PDO7_MINIMUM_ VOLTAGE	8'b 00100001	Sets PDO7's minimum voltage in 100mV increments. The default is 8'b 00100001, which is equal to 0x21 (3.3V).

PDO_V7_H (14h)

Format: Unsigned binary

If PDO7_TYPE is set to 1b (APDO), the PDO_V7_H command sets PDO7's maximum output voltage.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	PDO7_MAXIMUM_ VOLTAGE	8'b 11010010	Sets PDO7's maximum voltage in 100mV increments. The default is 8'b 00100001, which is equal to 0xD2 (21V).

PDO_I7 (15h)

Format: Unsigned binary

The PDO_I7 command sets PDO7's maximum output current.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	PDO7_CURRENT_ SETTING	8'b 00111100	Sets PDO7's maximum output current setting in 20mA units for fixed PDO, or 50mA units for APDO (PPS). The default is 8'b 00111100, which is equal to 3A at APDO. When these bits are set to exceed 3A, the MPQ4241 checks the cable current rating first. If it is 5A, then send the >3A setting; if the cable is 3A, only send a 3A maximum current capability.

PD_CTL1 (16h)

Format: Unsigned binary

The PD_CTL1 command controls certain functions.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	TYPE_C_1P5	1’b 0	Selects 3A or 1.5A USB Type-C mode. In 5V @ 3A USB Type-C mode, the R_P pull-up current is 330μA, and the R_D detection range is between 0.85V and 2.45V 1’b 0: 3A USB Type-C mode 1’b 1: 1.5A USB Type-C mode
D[6:5]	R/W	LEGACY_ CHARGING_MODE_ SEL	2’b 00	Selects the legacy charging mode. 2b 00: All DCP modes are active 2b 01: Apple mode and BC 1.2 mode are active 2b 11/10: Only BC 1.2 is active. No Apple mode or QC
D[4]	R/W	USBCOMMUNICATE	1’b 0	Sets whether USB communication is supported. 1’b 0: USB communication is not supported. This is the default 1’b 1: USB communication is supported
D[3]	R/W	NTC_CTL_RP	1’b 0	Selects whether NTC and over-temperature warning (OTW1/2) events trigger USB Type-C 3A or 1.5A mode. The default is 1’b 0. In 5V @ 3A USB Type-C mode, the R_P pull-up current is 330μA, and the R_D detection range is between 0.85V and 2.45V. 1’b 0: R_P = 1.5A when PDP < 15W; Otherwise R_P = 3A 1’b 1: Enter 1.5A USB Type-C mode if an NTC or OTW1/OTW2 event occurs
D[2:1]	R/W	TOUCH_TEMP	2’b 00	Sets the touch temperature default value to 0 or 1. For more details, refer to the “Source_Capabilities_Extended Message,” byte 20 in the USB PD specification. 2’b 00: 0 2’b 01: 1
D[0]	R/W	I2C_CTL_VOUT_EN	1’b 0	Enables controlling the I^2C registers 0x1A, 0x1B, and 0x1C. 1’b 0: V_{OUT} is controlled by the USB PD engine. The V_{OUT} and I_{OUT} limits do not change, even after sending commands to VOUT_L, VOUT_H, GO_BIT, and ILIMIT 1’b 1: V_{OUT} changes based on the VOUT/IOUT_CC register setting

PD_CTL2 (17h)

Format: Unsigned binary

The PD_CTL2 command controls certain functions.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	HDRST	1’b 0	Sends a hard reset command. 1’b 0: Normal state. This is the default 1’b 1: Send a hard reset command to the sink. After the HDRST message is sent, this bit automatically resets to 0b
D[6]	R/W	USB_SUSPEND	1’b 0	Sets whether the USB suspend function is supported. 1’b 0: Not supported. This is the default 1’b 1: Supported

D[5:3]	R/W	TOUCH_CURRENT	3’b 000	Sets the values for bits[2:0] of the touch current, defined in SOURCE_CAPABILITIES_EXTENDED. Message byte 13, bits[2:0]. Bit[5] of this command sets the touch current value for bit[2]. The default is 000b.
D[2:0]	R/W	COMPLIANCE	3’b 101	Sets the compliance values for bits[2:0], defined in SOURCE_CAPABILITIES_EXTENDED message byte 12, bits[2:0]. Bit D[2] of this command sets the compliance value for bit[2].

PWR_CTL1 (18h)

Format: Unsigned binary

The PWR_CTL1 command controls certain functions.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	EN	1’b 1	Determines whether I^2C control turns the part on or off. When the external EN pin is low, the converter is off, and the I^2C shuts down. When the EN pin is high, the EN bit takes over. The default is 1’b 1. 1’b 0: The device is off but the I^2C register does not reset. When EN = 0, the USB Type-C logic is off and the system clock is also off to save I_Q 1’b 1: The USB Type-C is disconnected; the system clock remains off to save I_Q
D[6]	R/W	MODE	1’b 1	Sets the MPQ4241’s switching mode. 1’b 0: Enables automatic PFM/PWM mode 1’b 1: Forced PWM mode
D[5:4]	R/W	FREQ	2’b 01	Sets the switching frequency (f_{SW}). 2’b 00: 250kHz 2’b 01: 420kHz 2’b 10: 2200kHz 2’b 11: Reserved
D[3]	R/W	DITHER	1’b 0	Enables the frequency spread spectrum (FSS) function. 1’b 0: Disabled 1’b 1: Enabled
D[2:1]	R/W	LINE_DROP_COMP	2’b 00	Sets the output voltage compensation vs. the load feature. The compensation amplitude is fixed for any output voltage. Set 0x3C, bit[6] = 1 to enable an additional compensation voltage. Line drop compensation is only enabled for applications where V_{OUT} ≥ 3V. Line drop compensation has a maximum clamp at 800mV, regardless of the output current. Line drop compensation is disabled once the default MPQ4241 enters PPS PDO mode. Line drop compensation can be enabled in PPS mode via 0x1F, bit[1]. 2’b 00: No compensation 2’b 01: V_{OUT} compensates 150mV at 3A I_{OUT} 2’b 10: V_{OUT} compensates 300mV at 3A I_{OUT} 2’b 11: V_{OUT} compensates 600mV at 3A I_{OUT}

D[0]	R/W	SLEW_RATE	1'b 1	Sets the output slew rate to adjust V_{OUT}. The slew rate can be calculated with the following equation: V_{OUT} Slew Rate = V_{REF} Slew Rate x Feedback Resistor Ratio (12.5) 1'b 0: 0.4mV/µs V_{REF} rising slew rate; 0.08mV/µs V_{REF} falling slew rate 1'b 1: 0.08mV/µs V_{REF} rising slew rate; 0.08mV/µs V_{REF} falling slew rate

PWR_CTL2 (19h)

Format: Unsigned binary

The PWR_CTL2 command controls certain functions.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	EN_VBUS	1'b 0	Enables the power converter's output directly, even if there is no attached USB Type-C sink device. 1'b 0: The power converter's on/off status is controlled by the USB Type-C controller. This is the default 1'b 1: The power converter is enabled
D[6]	R/W	PPS_MIN_SEL	1'b 1	Sets the V_{BUS} under-voltage (UV) threshold. This bit also controls the 3.3V or 5V minimum PPS voltage. 1'b 0: The V_{BUS} UV falling threshold is 4.5V, with 5% accuracy for 5V minimum PPS voltage applications 1'b 1: The V_{BUS} UV falling threshold is 3V (3.135V maximum), with 4.5% accuracy for 3.3V minimum PPS voltage applications
D[5:3]	R/W	OTW1_THRESHOLD	3'b 100	Sets the over-temperature warning (OTW) threshold. The OTW threshold has a hysteresis for recovery (20°C by default; set via 0x2D, bit[4]). The default value is 3'b 100. 3'b 000: Disable the OTW function 3'b 001: 100°C 3'b 010: 110°C 3'b 011: 120°C 3'b 100: 130°C 3'b 101: 140°C 3'b 110: 150°C 3'b 111: 160°C
D[2:0]	R/W	OTPTSD_ THRESHOLD	3'b 010	Sets the OT thermal shutdown threshold. The default value is 010. There is a 20°C hysteresis for recovery. 3'b 000: 150°C 3'b 001: 160°C 3'b 010: 170°C 3'b 011: 180°C 3'b 100~111: Reserved

VOUT_L (1Ah) and VOUT_H (1Bh)

Format: Linear

The VOUT_L and VOUT_H registers set V_{OUT} following an 11-bit direct format.

Name	VOUT															
Format	Direct, Unsigned Binary Integer															
Register Name	N/A					VOUT_H D[7:0]								VOUT_L D[2:0]		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	N/A					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	N/A					Data Bit High			Data Bit Low							
Default Value (5V)	N/A					250 Integer										

The real-world V_{OUT} (in V) can be calculated with Equation (2):

$$V_{OUT}\ (V) = V / 100 + 2.5 \quad (2)$$

Where *V* is an 11-bit, unsigned binary integer from VOUT[10:0] (ranging between 0 and 2047). The V_{OUT} resolution (or minimum step) is 10mV. The MPQ4241 has a feedback network from the OUT pin to the internal FB reference voltage. The feedback resistor ratio is V_{OUT} / V_{REF} = 12.5.

See the GO_BIT bit section below for more details on how to implement output voltage changes.

IOUT_LIM (1Ch)

Format: Unsigned binary

The IOUT_LIM command controls certain functions.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	GO_BIT	1’b 0	Controls when the MPQ4241 starts to change V_{OUT}. Set GO_BIT to 1 to start changing V_{OUT} based on the VOUT register. When V_{OUT} is done changing (the internal V_{REF} steps to the target V_{REF}), GO_BIT auto-resets to 0. This prevents false operation of the V_{OUT} scale. 1’b 0: V_{OUT} does not change 1’b 1: V_{OUT} changes based on the VOUT register setting; after V_{OUT} finishes scaling, this bit resets to 0 automatically
D[6:0]	R/W	IOUT_LIM	7’b 01001000	Sets the buck output’s CC current limit in 50mA units. The default is 7’b 01001000, which is equal to 0x48 (3.6A). When changing IOUT_LIM, the internal I_{REF} should have slew rate control. The ramping slew rate is 1mA/µs.

CTL_SYS0 (1Dh)

Format: Unsigned binary

The CTL_SYS0 command controls certain functions.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	PDO_CURRENT_ PLUS10MA	7’b 00000000	Sets an additional 10mA for PDO1 to PDO7’s output current. These bits are only valid for fixed PDO. D[6]: Control PDO7 D[5]: Controls PDO6 D[4]: Controls PDO5 D[3]: Controls PDO4 D[2]: Controls PDO3 D[1]: Controls PDO2 D[0]: Controls PDO1

CTL_SYS1 (1Eh)

Format: Unsigned binary

The CTL_SYS1 command controls certain functions.

<table>
<tr><th>Bits</th><th>Access</th><th>Bit Name</th><th>Default</th><th>Description</th></tr>
<tr><td>D[7]</td><td>R/W</td><td>SEND_SRC_CAP</td><td>1’b 0</td><td>Sends the source capability message. The default is 0b.

1’b 0: No action
1’b 1: Write 1 to this bit to force the MPQ4241 to send a SRC_CAP message; this bit automatically resets to “0” after the SRC_CAP message is sent out</td></tr>
<tr><td>D[6:4]</td><td>R/W</td><td>EN_OFF_TIMER</td><td>3’b 000</td><td>Sets a different EN off timer. When pulling down the EN pin, the chip is delayed based on the timer then shuts down. If EN is pulled high before the timer expires, then the counter is reset.

3’b 000: No delay
3’b 001: 10 minutes
3’b 010: 20 minutes
3’b 011: 40 minutes
3’b 100: 80 minutes
3’b 101: 120minutes</td></tr>
<tr><td>D[3:0]</td><td>R/W</td><td>I2C_SLAVE_ ADDRESS</td><td>4’b 0001</td><td>Sets the I²C slave address bits A4:A1. The slave address is 7 bits followed by an 8th data direction bit (read or write). The A5:A1 bits can be configured via the I²C or OTP.

When GPIO1 is selected as I2C_ADD, it can set different I²C slave addresses. It is an input pin and accepts a logic high or logic low input. A5 is controlled via the I2C_ADD pin. If I2C_ADD = high, A5 = 1; if I2C_ADD = low or floating, A5 = 0.

<table><tr><th></th><th>A7</th><th>A6</th><th>A5</th><th>A4</th><th>A3</th><th>A2</th><th>A1</th></tr><tr><td>Setting Value</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td></tr></table>
The A4:A1 values are set via the I2C_SLAVE_ADDRESS, bits D[3:0].

<table><tr><th colspan="3">I²C Address A7:A1 (D[3:0] = 0001)</th></tr><tr><td>I2C_ADD GPIO Status</td><td>Binary</td><td>Hex</td></tr><tr><td>I2C_ADD = Logic Low (or this GPIO is Not Selected)</td><td>1100 001 (Default)</td><td>61h</td></tr><tr><td>I2C_ADD = Logic High</td><td>1110 001</td><td>71h</td></tr></table></td></tr>
</table>

CTL_SYS2 (1Fh)

Format: Unsigned binary

The CTL_SYS2 command controls certain functions.

Bits	Access	Bit Name	Default	Description
D[7:5]	R/W	GPIO1	3’b 000	Sets the GPIO1 pin’s function. 3’b 000: POWER_SHARE. See the Power Share Function section on page 26 for more details 3’b 001: POL. This pin indicates the USB Type-C plug’s polarity. Open-drain output. When CC1 is selected as the CC line, the POL pin pulls low; when CC2 is selected as the CC line or detached, the POL pin is an open drain 3’b 010: FAULT. See the Pin Functions section on page 5 for the FAULT description. The TSD means that if thermal shutdown occurs, this pin pulls low 3’b 011: NTC2. When this function is selected, the power share input is controlled by NTC2. NTC_MODE does not control the NTC2 behavior. NTC_HYSTERESIS sets the hysteresis 3’b 100: ALT. This pin indicates a USB Type-C attach or fault event status; open-drain structure. When the sink is attached, the ALT pin inserts a 12μs low pulse; if a fault event is triggered, the ALT pin pulls low until the fault event is removed. See the Pin Functions section on page 5 for the ALT description 3’b 101: I2C_ADD. See the CTL_SYS1 (1Eh) section on page 44 for more details 3’b 110: NTC_CNT. This pin is the NTC thermal sense input for the USB Type-C connector 3’b 111: FREQ SYNC input. See the SYNC_IN section on page 26 for more details
D[4:1]	R/W	GPIO2	4’b 0000	Sets the GPIO2 pin’s function. 4’b 0000: Reserved 4’b 0001: POL. This pin indicates the USB Type-C plug’s polarity. Open-drain output. When CC1 is selected as the CC line, the POL pin pulls low; when CC2 is selected as the CC line or detached, the POL pin is an open drain 4’b 0010: NTC_CNT. This pin is the NTC thermal sense input for the USB Type-C connector (it cannot be used with GPIO1_NTC_CNT at the same time) 4’b 0011: VCONN_IN. Apply a 5V/1.5W power supply on this pin 4’b 0100: LED_PWM output. This has a 25kHz PWM signal output with an adjustable duty cycle. See the LED_PWM_DUTY bit section on page 52 for more details 4’b 0101: ATTACH. This pin indicates whether the USB Type-C port is attached or unattached. It has two states: low and open drain. When a USB Type-C port is attached, ATTACH pulls low; otherwise it is an open drain. 4’b 0110: FAULT. See the Pin Functions section on page 5 for the FAULT description 4’b 0111: POWER_SHARE. See the Power Share Function section on page 26 for more details 4’b 1000: NTC function. It is an input pin to sense external thermal conditions. See the NTC Function section on page 25 for more details 4’b 1001: POWER_SHARE_HIGH_ACTIVE. V_{GPIO2} exceeding 1.2V triggers power-sharing. See the GPIO2_POWER_SHARE section on page 27 for more details

D[0]	R/W	LDC_EN_PPS	1’b 0	Enables line drop compensation in a PPS status setting. 1’b 0: Line drop is disabled in a PPS PDO status 1’b 1: Line drop is enabled even in PPS mode

CTL_SYS3 (20h)

Format: Unsigned binary

The CTL_SYS3 command controls certain functions.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	PS_PDP_THD	8’b 01011010	Sets the threshold to which the PDO power rating is reduced. When the GPIOx pin (if GPIOx is set to the POWER_SHARE function) is pulled low, the MPQ4241’s PD power is reduced to the value set by PS_PDP_THD. The default value is 45W. 0x01: 0.5W 0xFF: 127.5W

CTL_SYS4 (21h)

Format: Unsigned binary

The CTL_SYS4 command controls certain functions.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	PS_PDP_THD_ PDO_SELECT	8’b 10111110	Selects which voltage is enabled in the PDO list (see Table 4 on page 27). The final PDO current is determined by PS_PDP_THD. The default is 5V, 9V, 15V, 20V, 3.3V to 5.9V, 3.3V to 11V, and 3.3V to 16V.

CTL_SYS5 (22h)

Format: Unsigned binary

The CTL_SYS5 command controls certain functions.

Bits	Access	Bit Name	Default	Description
D[7]	R	RESERVED	N/A	Reserved.
D[6]	R/W	PPS_3A_5A	1’b 0	Sets the maximum current for APDO after entering a power-sharing, V_{BATT} low, OTW, or NTC state. 1’b 0: 3A 1’b 1: 5A (requires 5A cable)
D[5:4]	R/W	CC_BLANK_TIMER	2’b 10	Sets the blank time when the output CC over-current condition is reached. 00b: No additional CC blank timer 2’b 01: 2ms 2’b 10: 12ms 2’b 11: 32ms
D[1:0]	R/W	PD_CAP_ PEAK_CURRENT	2’b 11	Enables the peak current 1, 2, and 3 capabilities in the SOURCE_CAP_EXTEND message. 2’b 00: Not support 2’b 01: Support peak current 1 2’b 10: Support peak current 1 and 2 2’b 11: Support peak current 1, 2, and 3

CTL_SYS6 (23h)

Format: Unsigned binary

The CTL_SYS6 command controls certain functions.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	VBATT_LOW1_PDP	8’b 01011010	Sets the maximum power rating when V_{BATT} is below the first threshold. PDP is reduced to this setting. The default value is 45W. 0x01: 0.5W 0xFF: 127.5W

CTL_SYS7 (24h)

Format: Unsigned binary

The CTL_SYS7 command controls certain functions.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	VBATT_L1_PDO_ SELECT	8’b 1011 1110	Selects which voltage is enabled in the PDO list (see Table 4 on page 27)p. The final PDO current is determined by PDP_L. The default is 5V, 9V, 15V, 20V, 3.3V to 5.9V, 3.3V to 11V, and 3.3V to 16V.

CTL_SYS8 (25h)

Format: Unsigned binary

The CTL_SYS8 command controls certain functions.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	VBATT_LOW2_PDP	8’b 00011110	Sets the maximum power rating when V_{BATT} is below the second threshold. PDP is reduced to this setting. The default value is 15W. 0x01: 0.5W 0xFF: 127.5W

CTL_SYS9 (26h)

Format: Unsigned binary

The CTL_SYS9 command controls certain functions.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	VBATT_L2_PDO_ SELECT	8’b 10111110	Selects which voltage is enabled in the PDO list (see Table 4 on page 27). The final PDO current is determined by PDP_L. The default is 5V, 9V, 15V, 20V, 3.3V to 5.9V, 3.3V to 11V, and 3.3V to 16V.

CTL_SYS10 (27h)

Format: Unsigned binary

The CTL_SYS10 command controls certain functions.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	OTW1_PDP	8’b 01011010	Sets the maximum power rating when the die temperature exceeds the threshold. PDP is reduced to this setting. The default value is 45W. 0x01: 0.5W 0xFF: 127.5W

CTL_SYS11 (28h)

Format: Unsigned binary

The CTL_SYS11 command controls certain functions.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	OTW1_PDO_ SELECT	8’b 10111110	Selects which voltage is enabled in the PDO list (see Table 4 on page 27). The final PDO current is determined by PDP_L. The default is 5V, 9V, 15V, 20V, 3.3V to 5.9V, 3.3V to 11V, and 3.3V to 16V.

CTL_SYS12 (29h)

Format: Unsigned binary

The CTL_SYS12 command controls certain functions.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	OTW2_NTC_PDP	8’b 00111100	Sets the maximum power rating when the die temperature exceeds the OTW2_NTC threshold. The PDP is reduced to this setting. The default value is 30W. 0x01: 0.5W 0xFF: 127.5W

CTL_SYS13 (2Ah)

Format: Unsigned binary

The CTL_SYS13 command controls certain functions.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	OTW2_NTC_PDO_ SELECT	8’b 10111110	Selects which voltage is enabled in the PDO list (see Table 4 on page 27). The final PDO current is determined by PDP_L. The default is 5V, 9V, 15V, 20V, 3.3V to 5.9V, 3.3V to 11V, and 3.3V to 16V.

CTL_SYS14 (2Bh)

Format: Unsigned binary

The CTL_SYS14 command controls certain functions.

<table>
<tr><th>Bits</th><th>Access</th><th>Bit Name</th><th>Default</th><th>Description</th></tr>
<tr><td>D[7:4]</td><td>R/W</td><td>VBATT_LOW_THLD1</td><td>4’b 0100</td><td>Sets the first VBATT_LOW threshold for V_{IN} detection. See the table below for more information.
<table>
<tr><th>Bits[3:0]</th><th>V_{IN} Falling</th><th>Hysteresis</th></tr>
<tr><td>0000</td><td>This function is disabled</td><td>This function is disabled</td></tr>
<tr><td>0001</td><td>12.6V</td><td rowspan="16">800mV</td></tr>
<tr><td>0010</td><td>12.2V</td></tr>
<tr><td>0011</td><td>11.8V</td></tr>
<tr><td>0100</td><td>11.4V</td></tr>
<tr><td>0101</td><td>11V</td></tr>
<tr><td>0110</td><td>10.6V</td></tr>
<tr><td>0111</td><td>10.2V</td></tr>
<tr><td>1000</td><td>9.8V</td></tr>
<tr><td>1001</td><td>9.4V</td></tr>
<tr><td>1010</td><td>9V</td></tr>
<tr><td>1011</td><td>8.6V</td></tr>
<tr><td>1100</td><td>8.2V</td></tr>
<tr><td>1101</td><td>7.8V</td></tr>
<tr><td>1110</td><td>7.4V</td></tr>
<tr><td>1111</td><td>7V</td></tr>
</table>
</td></tr>
</table>

<table>
<tr>
<td>D[3:0]</td>
<td>R/W</td>
<td>VBATT_LOW_THLD2</td>
<td>4’b 1000</td>
<td>Sets the second VBATT_LOW threshold for V_{IN} detection. See the table below for more information.
<table>
<tr><th>Bits[3:0]</th><th>V_{IN} Falling</th><th>V_{IN} Rising</th></tr>
<tr><td>0000</td><td>This function is disabled</td><td>This function is disabled</td></tr>
<tr><td>0001</td><td>11.8V</td><td rowspan="16">800mV</td></tr>
<tr><td>0010</td><td>11.4V</td></tr>
<tr><td>0011</td><td>11V</td></tr>
<tr><td>0100</td><td>10.6V</td></tr>
<tr><td>0101</td><td>10.2V</td></tr>
<tr><td>0110</td><td>9.8V</td></tr>
<tr><td>0111</td><td>9.4V</td></tr>
<tr><td>1000</td><td>9V</td></tr>
<tr><td>1001</td><td>8.6V</td></tr>
<tr><td>1010</td><td>8.2V</td></tr>
<tr><td>1011</td><td>7.8V</td></tr>
<tr><td>1100</td><td>7.4V</td></tr>
<tr><td>1101</td><td>7V</td></tr>
<tr><td>1110</td><td>6.6V</td></tr>
<tr><td>1111</td><td>6.2V</td></tr>
</table>
</td>
</tr>
</table>

CTL_SYS15 (2Ch)

Format: Unsigned binary

The CTL_SYS15 command controls certain functions.

<table>
<tr><th>Bits</th><th>Access</th><th>Bit Name</th><th>Default</th><th>Description</th></tr>
<tr>
<td>D[7:4]</td>
<td>R/W</td>
<td>VBATT_LOW_THLD3</td>
<td>4’b 1010</td>
<td>Sets the third VBATT_LOW threshold for V_{IN} detection. See the table below for more information.
<table>
<tr><th>Bits[3:0]</th><th>V_{IN} Falling</th><th>V_{IN} Rising</th></tr>
<tr><td>0000</td><td>This function is disabled</td><td>This function is disabled</td></tr>
<tr><td>0001</td><td>9.8V</td><td rowspan="16">800mV</td></tr>
<tr><td>0010</td><td>9.4V</td></tr>
<tr><td>0011</td><td>9V</td></tr>
<tr><td>0100</td><td>8.6V</td></tr>
<tr><td>0101</td><td>8.2V</td></tr>
<tr><td>0110</td><td>7.8V</td></tr>
<tr><td>0111</td><td>7.4V</td></tr>
<tr><td>1000</td><td>7V</td></tr>
<tr><td>1001</td><td>6.6V</td></tr>
<tr><td>1010</td><td>6.2V</td></tr>
<tr><td>1011</td><td>5.8V</td></tr>
<tr><td>1100</td><td>5.4V</td></tr>
<tr><td>1101</td><td>5V</td></tr>
<tr><td>1110</td><td>4.6V</td></tr>
<tr><td>1111</td><td>4.2V</td></tr>
</table>
</td>
</tr>
<tr>
<td>D[3:2]</td>
<td>R/W</td>
<td>VBATT_LOW_BLK</td>
<td>2’b 01</td>
<td>Sets the VBATTERY_LOW1, VBATTERY_LOW2, and VBATTERY_LOW3 blanking time.

00b: 2ms
2’b 01: 10ms
2’b 10: 48ms
2’b 11: 160ms</td>
</tr>
<tr>
<td>D[1:0]</td>
<td>N/A</td>
<td>RESERVED</td>
<td>N/A</td>
<td>Reserved.</td>
</tr>
</table>

CTL_SYS16 (2Dh)

Format: Unsigned binary

The CTL_SYS16 command controls certain functions.

Bits	Access	Bit Name	Default	Description
D[7:6]	R/W	SLOW_SW	2'b 00	Sets the switching speed. 2'b 00: Normal SW rising/falling speed 2'b 01: Slower SW rising/falling speed 2'b 10: Faster SW rising/falling speed
D[4]	R/W	OTW_ HYSTERESIS	1'b 0	Sets the over-temperature warning (OTW1, OTW2) recovery hysteresis. 1'b 0: 20°C 1'b 1: 40°C
D[3:1]	R/W	OTW2_THRESHOLD	3'b 110	Sets the OTW threshold. The OT warning has a 20°C or 40°C hysteresis for recovery, which is set via 2Dh, bit D[4]. 3'b 000: Disable the OTW function 3'b 001: 100°C 3'b 010: 110°C 3'b 011: 120°C 3'b 100: 130°C 3'b 101: 140°C 3'b 110: 150°C 3'b 111: 160°C
D[0]	R/W	NTC_CNT_ DISABLE	1'b 0	Enables a USB Type-C connector NTC fault to trigger a shutdown. 1'b 0: Enable the function of NTC_CNT > 145°C shutdown 1'b 1: Disable the function of NTC_CNT > 145°C shutdown

CTL_SYS17 (2Eh)

Format: Unsigned binary

The CTL_SYS17 command controls certain functions.

Bits	Access	Bit Name	Default	Description
D[7:6]	R/W	PEAK_CL	2'b 11	Sets the high-side peak current limit in buck mode. 2'b 00: 8A 2'b 01: 10A 2'b 10: 12A 2'b 11: 14A
D[4]	R/W	NTC_HYSTERESIS	1'b 1	Sets the NTC thermal recovery hysteresis. This bit controls both NTC and NTC2. 1'b 0: 10% 1'b 1: 20%
D[3]	R/W	NTC_MODE	1'b 0	Sets the behavior when the NTC function is triggered. 1'b 0: Shut down the MPQ4241 1'b 1: Reduce the PD power to the value set by OTW2_NTC_PDP
D[1:0]	R/W	VBUS_ VOLTAGE	2'b 10	Sets the default V_{BUS}. 2'b 00: 5.0V 2'b 01: 5.05V 2'b 10: 5.1V 2'b 11: 5.15V

CTL_SYS18 (2Fh)

Format: Unsigned binary

The CTL_SYS18 command controls certain functions.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	OTP_ PROGRAM	1’b 0	Configures the I²C register value into the OTP memory cell. The password is required before executing OTP configurations. The OTP can be configured once. Only the MPQ4241-0000 and OTP_PAGE = 0 can be used for OTP configurations. Apply a 12V V_{IN} during the OTP configurations. 1’b 0: No action 1’b 1: Write 1 to implement OTP configurations. After the OTP finishes configuring, this bit automatically reset to 0
D[6:0]	R/W	LED_PWM_DUTY	7’b 0110 010	Sets the LED_PWM output duty cycle. The minimum value is 5%, and the maximum is 100%. 0x05: 5% 0x64: 100%

STATUS1 (30h)

Format: Unsigned binary

The STATUS1 command latches off, then is cleared when it is read.

Bits	Access	Bit Name	Description
D[7]	R	ATTACHED	Indicates whether the sink device is attached. 1’b 0: Detached 1’b 1: Attached
D[6]	R	NTC2_ENTER	Indicates whether an NTC2 state has been entered. 1’b 0: Not entered 1’b 1: Entered
D[5]	R	PG	Indicates the output power good status. 1’b 0: Power is not good 1’b 1: Power is good
D[4]	R	SHORT_VBATT	Indicates the output bus voltage status. 1’b 0: Normal state 1’b 1: DP/DM/CC1/CC2 is shorted with the battery voltage
D[3]	R	TSD	1’b 0: The IC is not in a thermal shutdown state 1’b 1: The IC is in a thermal shutdown (TSD) protection state; includes both die senses (TSD and NTC both sense TSD events)
D[2]	R	OTP_PAGE	Indicate the current OTP page index. 1’b 0: Page 0, no OTP programmed 1’b 1: Page 1
D[1]	R	CC_CV	Indicates the output power status. 1’b 0: CV state 1’b 1: The output is in a CC current limit state
D[0]	R	NTC_ENTER	Indicates whether an NTC state has been entered. 1’b 0: Not entered 1’b 1: Entered

STATUS2 (31h)

Format: Unsigned binary

The STATUS2 command latches off, then is cleared when it is read.

Bits	Access	Bit Name	Description
D[7]	R	VBATT_LOW1_FLAG	Indicates whether V_{IN} is below VBATT_LOW_THRESHOLD1. 1'b 0: V_{IN} is not below the threshold 1'b 1: V_{IN} is below the threshold
D[6]	R	VBATT_LOW2_FLAG	Indicates whether V_{IN} is below VBATT_LOW_THRESHOLD2. 1'b 0: V_{IN} is not below the threshold 1'b 1: V_{IN} is below the threshold
D[5]	R	OTW1	Indicates whether the device is in the first over-temperature warning (OTW1) state. 1'b 0: No OTW1 state has been detected 1'b 1: The device is in an OTW1 state
D[4]	R	OTW2	Indicates whether the device is in the second over-temperature warning (OTW2) state. 1'b 0: No OTW2 state has been detected 1'b 1: The device is in an OTW2 state
D[3:1]	R	SELECTED_PDO_ INDEX	Returns the sink's selected PDO index. 4'b 0000: No PD contract 4'b 0001: PDO 1~7 is selected
D[0]	R	PDO_TYPE	Indicates whether the sink's selected PDO is fixed PDO or APDO (PPS). 1'b 0: Fixed PDO 1'b 1: APDO

STATUS3 (32h)

Format: Unsigned binary

The STATUS3 command indicates live statuses. It is a non-latch register.

Bits	Access	Bit Name	Description
D[7]	R	POL	Indicates the USB Type-C plug polarity. 1'b 0: CC1 is attached to R_D 1'b 1: CC2 is attached to R_D
D[6]	R	FAULT	Selects how the FAULT function indicates whether a fault has occurred when pulling low. The fault condition includes over-current protection (OCP) (it does not indicate when the sink requests APDO and enters constant current limit mode) TSD, DP/DM/CCx short-to-battery, and V_{OUT} absolute over-voltage protection (OVP). Open-drain output. 1'b 0: The IC is not in a fault state 1'b 1: The IC has entered a fault state
D[5]	R	PD_VALID	1'b 0: There is no valid PD contract 1'b 1: A PD contract is established
D[4]	R	QC_VALID	1'b 0: QC 3.0 or FCP mode is not entered 1'b 1: The IC has entered QC 3.0 or FCP mode
D[0]	R	OUT_OVP	1'b 0: The output is not in an over-voltage protection (OVP) state 1'b 1: The output is in an OVP state

STATUS4 (33h)

Format: Unsigned binary

The STATUS4 command indicates live statuses. It is a non-latch register.

Bits	Access	Bit Name	Description
D[7:0]	R	CONTRACT POWER	Returns the PD contracted power in 0.5W units. Calculate the fixed PDO value with the following equation: Fixed PDO = Voltage x Maximum Current Calculate the PPS with the following equation: PPS = Max Voltage x Max Current If there is no PD contract, the value is 7.5W or 15W, depending on R_P.

ID1 (34h)

Format: Unsigned binary

The ID1 command sets the OTP suffix code, which is defined by MPS.

Bits	Access	Bit Name	Description
D[7:0]	R	OTP_SUFFIX_CODE	“0x00” means the standard MPQ4241-0000. “0x01” means the MPQ4241-0001 part number.

ID2 (35h)

Format: Unsigned binary

The ID2 command sets the OTP software revision number, which is defined by MPS.

Bits	Access	Bit Name	Description
D[7:0]	R	OTP_SOFTWARE_ REVISION_NO	Stores the revision number. The OTP value may need to be updated from time to time.

FW_REV (36h)

Format: Unsigned binary

The FW_REV command controls certain functions.

Bit	Access	Name	Description
D[7]	R	MISMATCH	Indicates whether the sink request sets a mismatch bit. Defined in the PD specification. 1’b 0: MISMATCH bit is set to 0 1’b 1: MISMATCH bit is set to 1
D[6]	R	GIVEBACK_FLAG	This bit is set if the sink requests a GIVEBACK flag.
D[5]	R	CABLE_CAP	0’b 0: The cable can only handle 3A 1’b 1: 5A cable
D[4:0]	R	FIRMWARE_ REVISION	Returns the PD firmware revision number.

MAX_REQ_CUR (37h)

Format: Unsigned binary

The MAX_REQ_CUR command controls certain functions.

Bits	Access	Bit Name	Description
D[7:0]	R	MAX_REQ_CUR	Sets the sink-requested maximum operation current (when the MISMATCH bit = 1) in 20mA units. These bits are only valid when GIVEBACK_FLAG = 0 and a fixed PDO is selected.

MFR_ID (38h)

Format: Unsigned binary

The MFR_ID command controls certain functions.

Bits	Access	Bit Name	Description
D[7:0]	R	MANUFACTURER_ID	Returns the manufacturer ID. The default is “0000 1001b”.

DEV_ID (39h)

Format: Unsigned binary

The DEV_ID command controls certain functions.

Bits	Access	Bit Name	Description
D[7:0]	R	DEVICE_ID	Returns the device ID. The default is 0101 1000b.

CLK_ON (3Bh)

Format: Unsigned binary

The CLK_ON command enables the digital clock.

Bits	Access	Bit Name	Description
D[7:0]	W	CLOCK_ON	Enables the digital clock. Write 0x3B =0x01 to enable the digital clock, or it is enabled automatically when a USB Type-C device is connected. No I^2C registers can be modified before enabling the digital clock. This bit automatically resets to 0 after the clock is enabled. To disable the digital clock again, write 0x3B = 0, write the EN bit = 0, or pull down the EN pin or VIN pin below their UVLO thresholds.

CTL_SYS19 (3Ch)

Format: Unsigned binary

The CLT_SYS19 command controls certain functions.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	CTR_VCONN	1’b 0	Enables the VCONN function. 1’b 0: Enable VCONN 1’b 1: Disable VCONN
D[6]	R/W	ADDITIONAL_LINE_DROP_COMPENSATION	1’b 0	Enables the additional line drop compensation function. 0’b: Maintain the default line drop compensation function set via the 0x18 register 1’b: Enable additional 200mV line drop compensation based on the 0x18 register

GPIO1 and GPIO2 Options

GPIO1 Options	POWER_SHARE	POL	FAULT	NTC2	ALT	I2C_ADD	NTC_CNT	SYNC_IN	-
GPIO2 Options	POL	NTC_CNT	VCONN_IN	LED_PWM	ATTACH	FAULT	POWER_SHARE	NTC	POWER_SHARE_HIGH_ACTIVE

APPLICATION INFORMATION

COMPONENT SELECTION

Selecting the Inductor

For most applications, use an inductor with a DC current rating at least 25% higher than the maximum load current. Select an inductor with a small DC resistance for optimal efficiency. The inductance (L_1) can be calculated with Equation (3):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (3)$$

Where ΔI_L is the inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current can be estimated with Equation (4):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (4)$$

Choose L = 6.8µH to avoid a slope compensation issue when using a 250kHz switching frequency (f_{SW}). For automotive input and PD applications, choose the inductor ripple current to be approximately 30% to 50% of the maximum load current (see Table 7).

A full-shielded inductor is recommended to improve EMI.

Table 7: Recommended L (µH) for Different f_{SW} (D_{MAX} at ΔI_L = 30% to 50% I_{O_MAX})

V_{IN} = 12V, V_{OUT} = 5V to 9V	
f_{SW}	**L**
250kHz	6.8µH
420kHz	4.7µH
2.2MHz	1µH

Selecting Buck Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply the AC current while maintaining the DC input voltage. Use low-ESR capacitors for optimal performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For a 60W PD application, a 100µF electrolytic capacitor and two 4.7µF + 0.1µF ceramic capacitors are recommended.

Since the input capacitor (C_{IN}) absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be calculated with Equation (5):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (5)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, estimated with Equation (6):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (6)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using an electrolytic capacitor, place two additional, high-quality ceramic capacitors as close to IN as possible. Calculate the input voltage ripple caused by the capacitance with Equation (7):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

Selecting Output Capacitor

The device requires an output capacitor (C_{OUT}) to maintain the DC output voltage. Estimate the output voltage ripple with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESER} + \frac{1}{8 \times f_{SW} \times C2}\right) \quad (8)$$

Where L_1 is the inductance and R_{ESR} is the output capacitor's equivalent series resistance (ESR).

For an electrolytic capacitor, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be calculated with Equation (9):

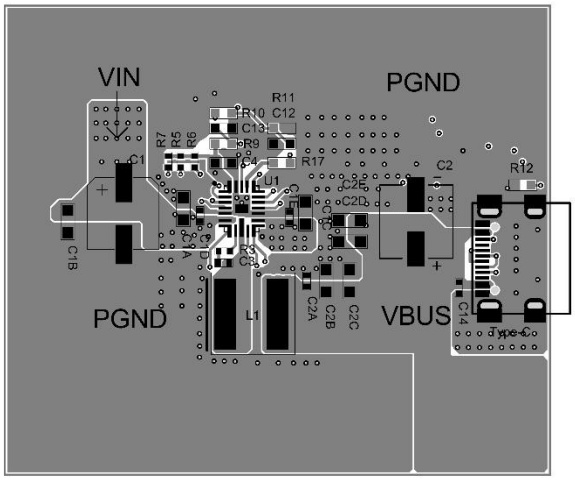
$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (9)$$

The MPQ4241's loop compensation is optimized for ceramic output capacitors. Typically, two 4.7µF ceramic output capacitors and one 100µF polymer/hybrid capacitor are recommended for excellent loop stability and transient response.

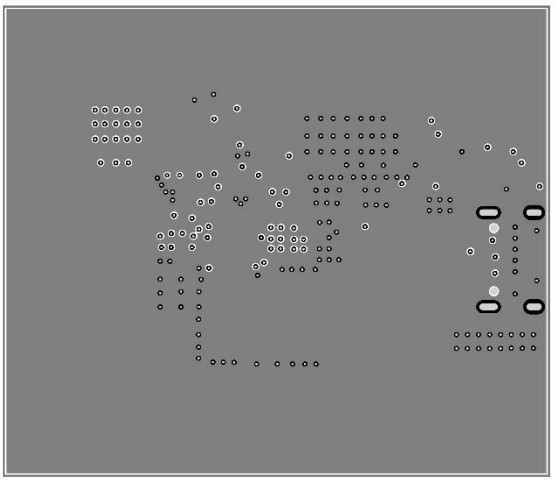
PCB Layout Guidelines

Efficient PCB layout is critical for standard operation and thermal dissipation. For the best guidelines, refer to Figure 17 and follow the guidelines below:

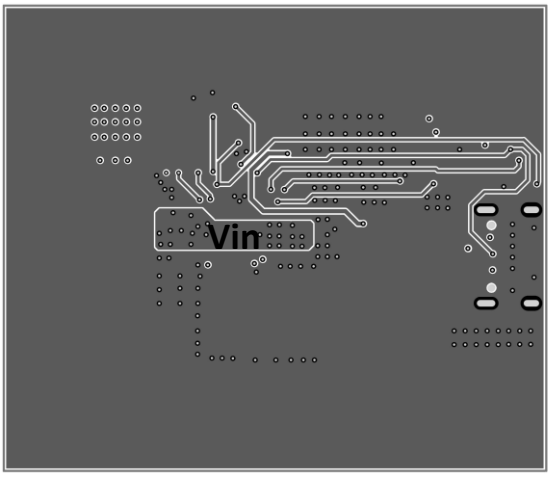
1. Use short, direct, and wide traces to connect OUT.
2. Place a large copper plane for PGND.
3. Add multiple vias to improve thermal dissipation. Connect AGND to PGND.
4. Place PGND vias close to the PGND pin and under the IC's body.
5. Place the VCC decoupling capacitor as close as possible to the VCC pin.
6. Place 2 or 3 vias close to the VCC decoupling capacitor's AGND terminal.
7. Place a large copper plane for SW to improve thermal dissipation.
8. To improve EMI performance, place two ceramic input decoupling capacitors as close as possible to VIN/VOUT and PGND.
9. Both VIN pins need decoupling capacitors. It is highly recommend to place them symmetrically.
10. Place an input filter on the bottom layer to improve EMI performance.
11. Place input capacitors close to the VIN pin and use wide copper for the VIN trace to reduce the parasitic inductance of the VIN loop.



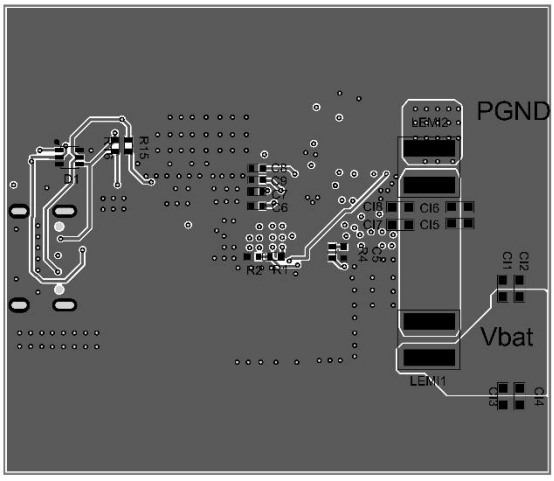
Top Layer



Mid-Layer 1



Mid-Layer 2



Bottom Layer

Figure 17: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

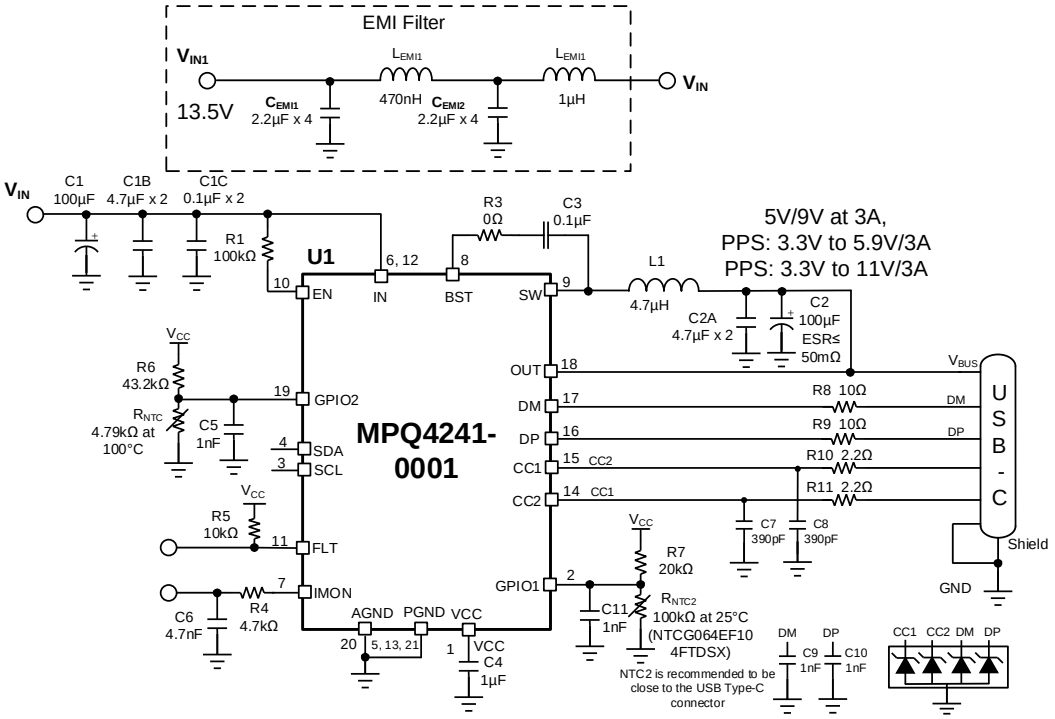


Figure 18: Typical Application Circuit (MPQ4241 27W PD Application)

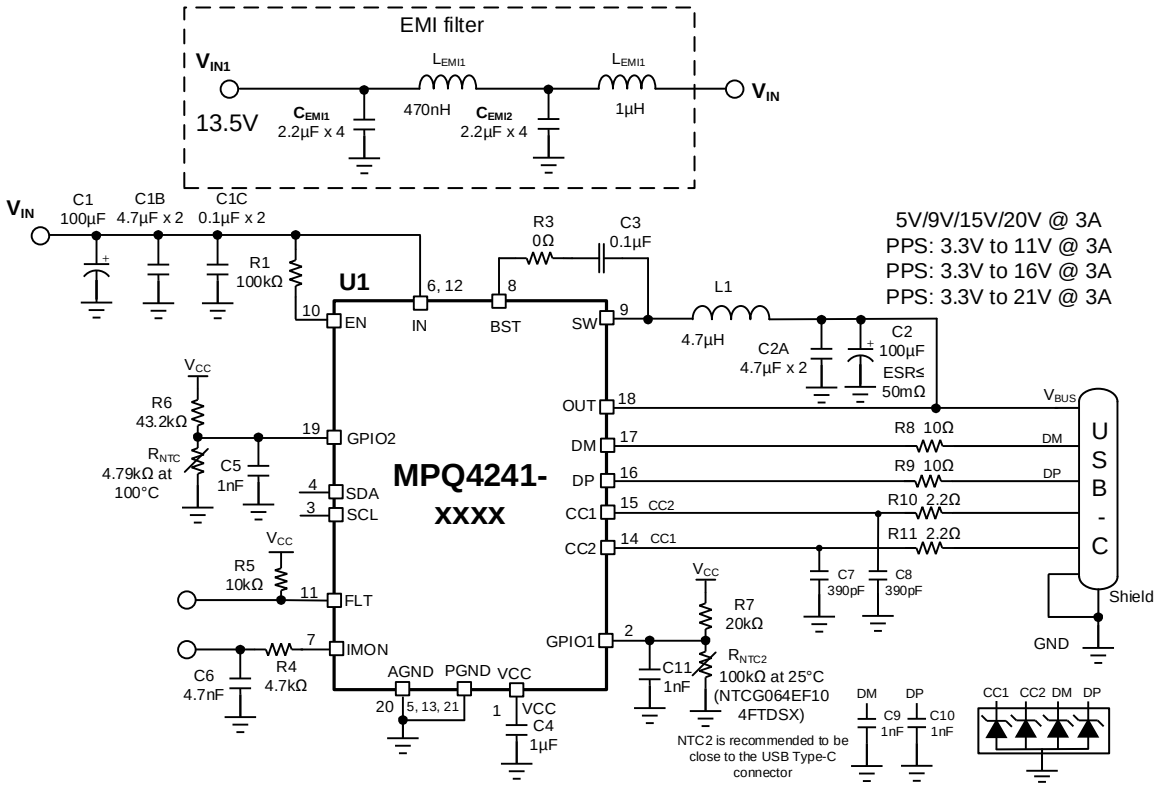


Figure 19: Typical Application Circuit (MPQ4241 60W PD Application)

MPQ4241GLE-0001 CONFIGURATION TABLES

OTP Items(PDO)	Enabled/Disabled	PDO Type	Voltage Setting	Current Setting
PDO1	Enabled	Fixed PDO	5V	3A
PDO2	1b: Enabled	0b: Fixed PDO	9V	3A
PDO3	1b: Enabled	1b: APDO	3.3V to 5.9V	3A
PDO4	1b: Enabled	1b: APDO	3.3V to 11V	3A
PDO5	0b: Disabled	N/A		
PDO6	0b: Disabled	N/A		
PDO7	0b: Disabled	N/A		

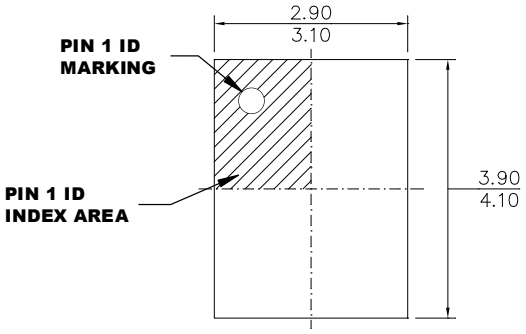
OTP Items	Description	Value
GPIO1	Configures the GPIO1 pin's function.	110b: NTC_CNT
GPIO2	Configures the GPIO2 pin's function.	1000b: NTC function
TSD_THRESHOLD	Sets the over-temperature shutdown threshold.	001b: 160°C
OTW1_THRESHOLD	Sets the over-temperature warning threshold.	100b: 130°C (default)
OTW1_PDP	Sets the maximum power rating when the die temperature is below the threshold.	15W
OTW1_PDO_SELECT	Selects which voltage is enabled in the PDO list.	0x8C
OTW2_THRESHOLD	Sets the over-temperature warning threshold.	110b: 150°C (default)
OTW2_NTC_PDP	Sets the maximum power rating when the die temperature is below the threshold.	7.5W
OTW2_NTC_PDO_SELECT	Selects which voltage is enabled in the PDO list.	0x08
OTW_HYSTERESIS	Sets the OTW1 and OTW2 recovery hysteresis temperature.	0b: 20°C (default)
NTC_HYSTERESIS	Set the NTC thermal recovery hysteresis	1b: 20% (default)
NTC_MODE	Set the MPQ4241 behavior when NTC is triggered.	0b: Shut down the MPQ4241 (default)
VBATT_LOW_THLD1	Set the first threshold for input voltage detection	0010b: 12.2V
VBATT_LOW_THLD2	Set the second threshold for input voltage detection	0101b: 10.2V
VBATT_LOW_THLD3	Sets the third threshold for input voltage detection. The device shuts down after the threshold is triggered.	1001b: 6.6V
VBATT_LOW_BLK	Sets the VBATTERY_LOW1 and VBATTERY_LOW2 blanking time.	00b: 2ms
VBATT_LOW1_PDP	Sets the maximum power rating when V_{BATT} is below the first threshold.	27W
VBATT_L1_PDO_SELECT	Selects the voltage that is enabled in the PDO list.	0x88
VBATT_LOW2_PDP	Sets the maximum power rating when V_{BATT} is below the second threshold.	15W
VBATT_L2_PDO_SELECT	Selects which voltage is enabled in the PDO list.	0X08
PS_PDP_THD	Sets the threshold for PDO power rating reduction.	15W
PS_PDP_THD_PDO_SELECT	Selects which voltage is enabled in the PDO list.	0x8C
VBUS_VOLTAGE	Sets the default V_{BUS}.	10b: 5.1V (default)

MPQ4241GLE-0001 CONFIGURATION TABLES *(continued)*

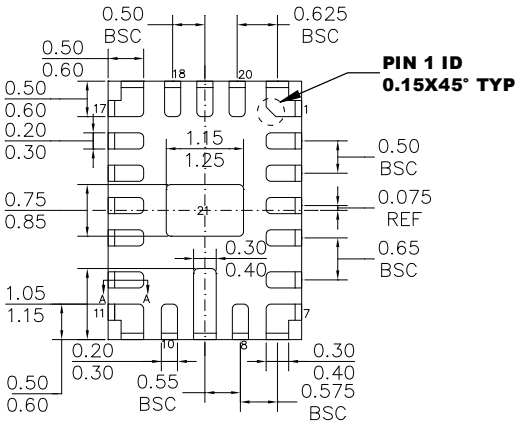
OTP Items	Description	Value
MODE	Selects the PFM/PWM mode.	1b: Forced PWM mode (default)
FREQ	Sets the switching frequency.	01b: 420kHz (default)
DITHER	Enables the spread spectrum feature.	1b: Enable frequency spread spectrum
EN_OFF_TIMER	Sets the different EN off timer.	000b: No delay (default)
LINE_DROP_COMP	Sets output voltage compensation vs. load feature.	00b: No compensation (default)
PPS_LDC_EN	Enables line drop compensation (LDC), even in PPS.	0b: Disable LDC in PPS (default)
SLEW RATE	Sets the output slew rate to adjust V_{OUT}.	1b: 0.08mV/μs V_{REF} rising slew rate, 0.08mV/μs V_{REF} falling slew rate (default)
PEAK_CL	Sets the high-side peak current limit.	00b: 8A
CC_BLANK_TIMER	Sets the blanking time when the output CC over-current threshold is reached.	10b: 12ms
LEGACY_CHARGING_ MODE_SEL	QC 3.0/DCP short mode/divider mode selection.	00b: All DCP modes are active (default)
I2C_SLAVE_ADDRESS	Sets the MPQ4241's I^2C slave address.	61h (default)

PACKAGE INFORMATION

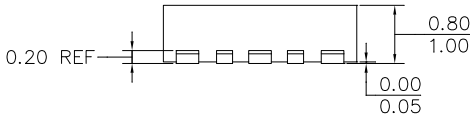
QFN-21 (3mmx4mm)



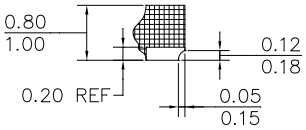
TOP VIEW



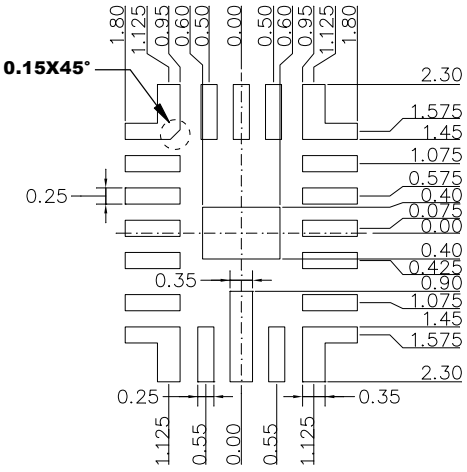
BOTTOM VIEW



SIDE VIEW



SECTION A-A

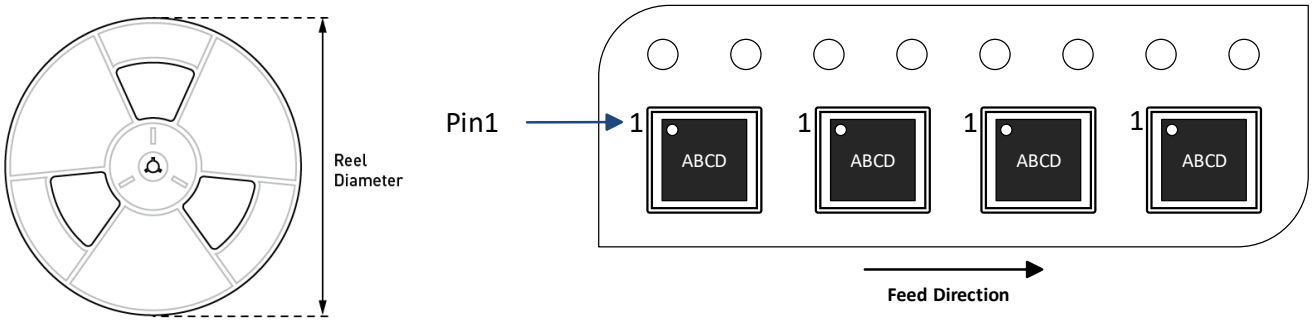


RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ4241GLE-0000-AEC1-Z	QFN-21 (3mmx4mm)	5000	N/A	N/A	13in	12mm	8mm
MPQ4241GLE-0001-AEC1-Z	QFN-21 (3mmx4mm)						
MPQ4241GLE-xxxx-AEC1-Z	QFN-21 (3mmx4mm)						

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	1/8/2025	Initial Release	-