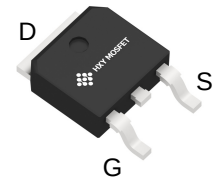




Description

The PHD101NQ03LT uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.



TO-252-2L

General Features

$V_{DS} = 30V$ $I_D = 100A$

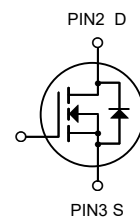
$R_{DS(ON)} < 5.5m\Omega @ V_{GS}=10V$

Application

Battery protection

Load switch

Uninterruptible power supply



N-Channel MOSFET

Ordering Information

Product ID	Pack	Brand	Qty(PCS)
PHD101NQ03LT	TO-252-2L	HXY MOSFET	2500

Absolute Maximum Ratings (Tc=25°C unless otherwise noted)

Symbol	Parameter	Rating		Units
VDS	Drain- Source Voltage	30		V
VGS	Gate-Source Voltage	± 20		V
$I_D@T_C=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	100		A
$I_D@T_C=100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	57		A
$I_D@T_A=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	27	17	A
$I_D@T_A=70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	23	14.5	A
I_{DM}	Pulsed Drain Current ²	160		A
EAS	Single Pulse Avalanche Energy ³	115.2		mJ
I_{AS}	Avalanche Current	48		A
$P_D@T_C=25^\circ C$	Total Power Dissipation ⁴	53		W
$P_D@T_A=25^\circ C$	Total Power Dissipation ⁴	6	2.4	W
TSTG	Storage Temperature Range	-55 to 175		°C
TJ	Operating Junction Temperature Range	-55 to 175		°C
$R_{\theta JA}$	Thermal Resistance Junction-ambient (Steady State) ¹	62		°C/W
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹ (t ≤10s)	25		°C/W
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	2.8		°C/W



Electrical Characteristics (T_J=25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	30	---	---	V
ΔBV _{DSS} /ΔT _J	BVDSS Temperature Coefficient	Reference to 25°C, I _D =1mA	---	0.028	---	V/°C
R _{DS(on)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =30A	---	3.8	5.5	mΩ
		V _{GS} =4.5V, I _D =15A	---	7.5	9	
V _{GS(th)}	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =250uA	1.0	1.5	2.5	V
ΔV _{GS(th)}	V _{GS(th)} Temperature Coefficient		---	-6.16	---	mV/°C
I _{DSS}	Drain-Source Leakage Current	V _{DS} =24V, V _{GS} =0V, T _J =25°C	---	---	1	uA
		V _{DS} =24V, V _{GS} =0V, T _J =55°C	---	---	5	
I _{GSS}	Gate-Source Leakage Current	V _{GS} =±20V, V _{DS} =0V	---	---	±100	nA
g _{fs}	Forward Transconductance	V _{DS} =5V, I _D =30A	---	22	---	S
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz	---	1.7	3.4	Ω
Q _g	Total Gate Charge (4.5V)	V _{DS} =15V, V _{GS} =4.5V, I _D =15A	---	20	---	nC
Q _{gs}	Gate-Source Charge		---	7.6	---	
Q _{gd}	Gate-Drain Charge		---	7.2	---	
T _{d(on)}	Turn-On Delay Time	V _{DD} =15V, V _{GS} =10V, R _G =3.3Ω, I _D =15A	---	7.8	---	ns
T _r	Rise Time		---	15	---	
T _{d(off)}	Turn-Off Delay Time		---	37.3	---	
T _f	Fall Time		---	10.6	---	
C _{iss}	Input Capacitance	V _{DS} =15V, V _{GS} =0V, f=1MHz	---	2295	---	pF
C _{oss}	Output Capacitance		---	267	---	
C _{rss}	Reverse Transfer Capacitance		---	210	---	
I _S	Continuous Source Current ^{1,5}	V _G =V _D =0V, Force Current	---	---	80	A
I _{SM}	Pulsed Source Current ^{2,5}		---	---	160	A
V _{SD}	Diode Forward Voltage ²	V _{GS} =0V, I _S =1A, T _J =25°C	---	---	1	V
t _{rr}	Reverse Recovery Time	IF=30A, dI/dt=100A/μs, T _J =25°C	---	14	---	nS
Q _{rr}	Reverse Recovery Charge	T _J =25°C	---	5	---	nC

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width .The EAS data shows Max. rating .
- 3.The test cond≤ 300us , duty cycle ition is V_{DD}=25≤V, V 2%_{GS} =10V, L=0.1mH, I_{AS}=53.8A
- 4.The power dissipation is limited by 175°C junction temperature
- 5.The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.



Typical Characteristics

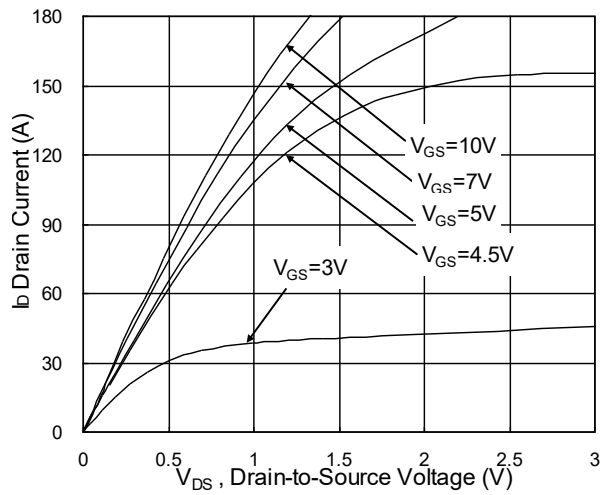


Fig.1 Typical Output Characteristics

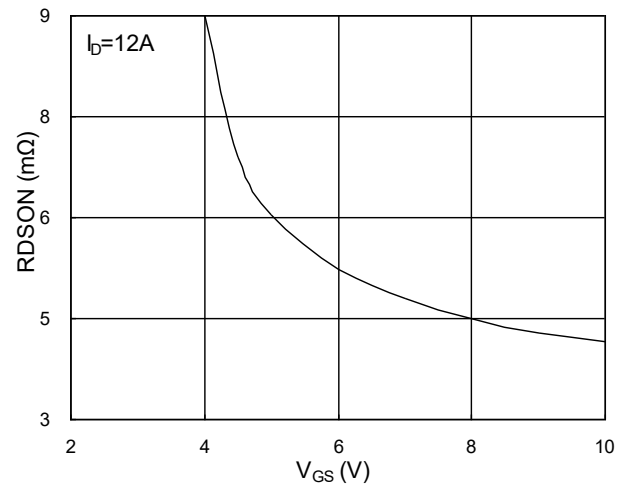


Fig.2 On-Resistance vs. G-S Voltage

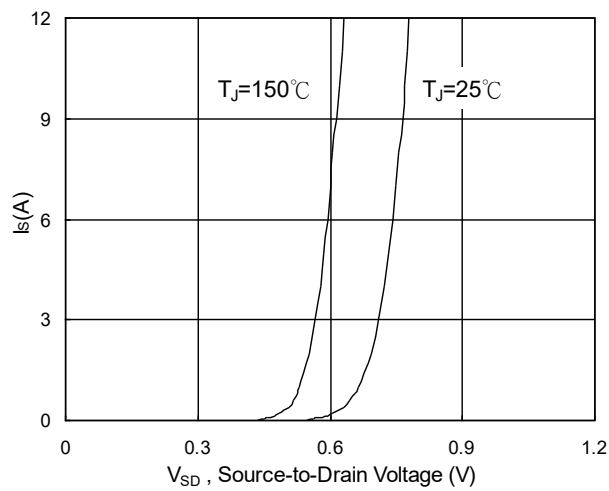


Fig.3 Forward Characteristics of Reverse

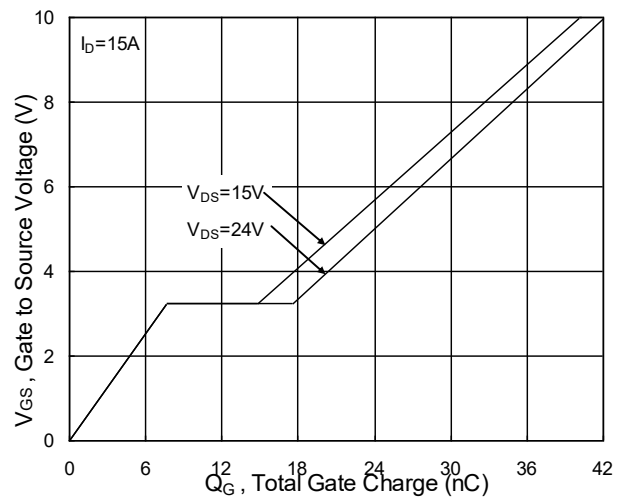


Fig.4 Gate-Charge Characteristics

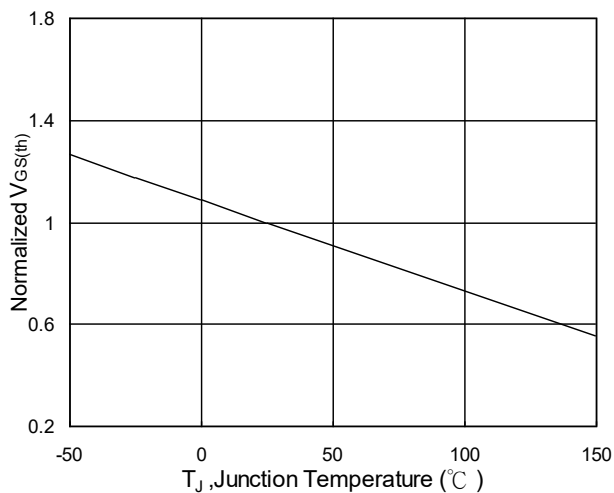


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

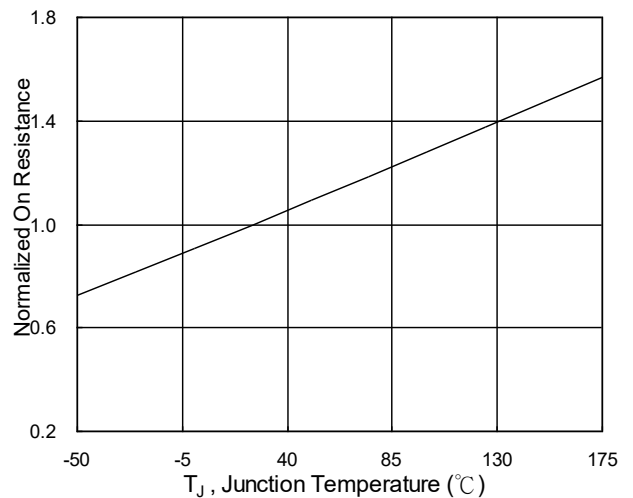


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

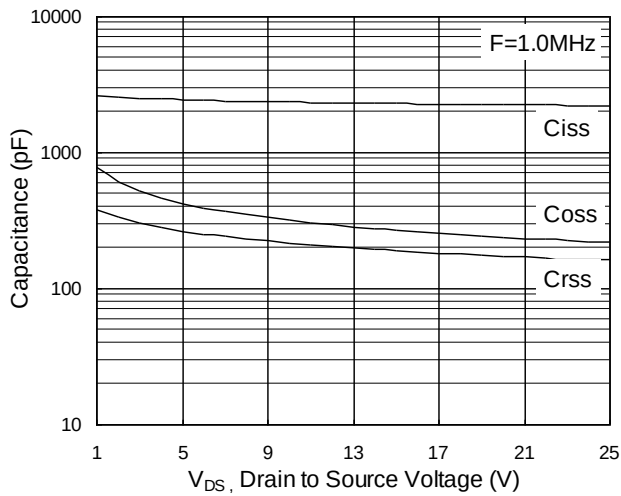


Fig.7 Capacitance

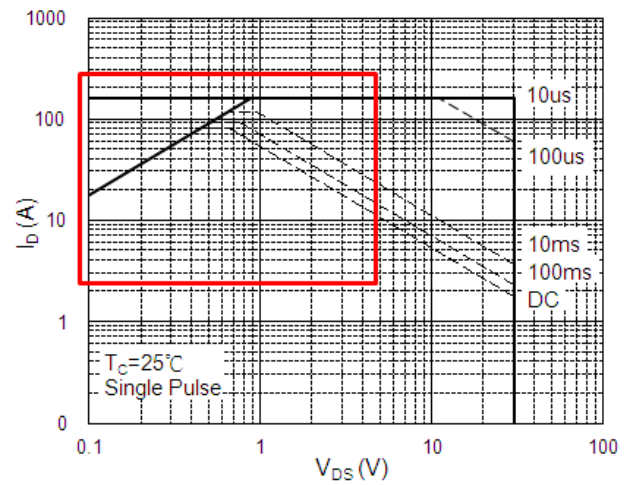


Fig.8 Safe Operating Area

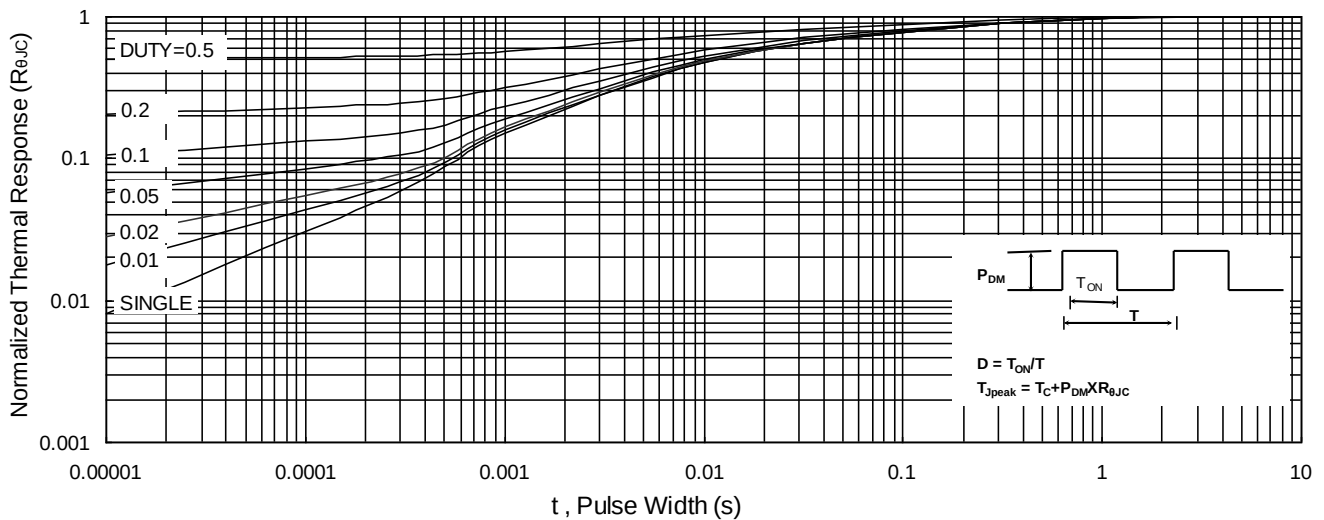


Fig.9 Normalized Maximum Transient Thermal Impedance

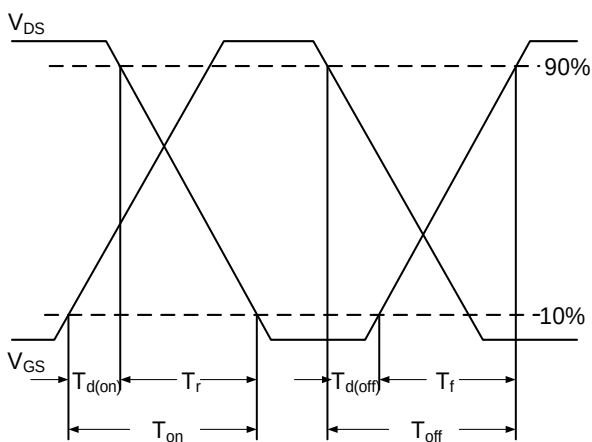


Fig.10 Switching Time Waveform

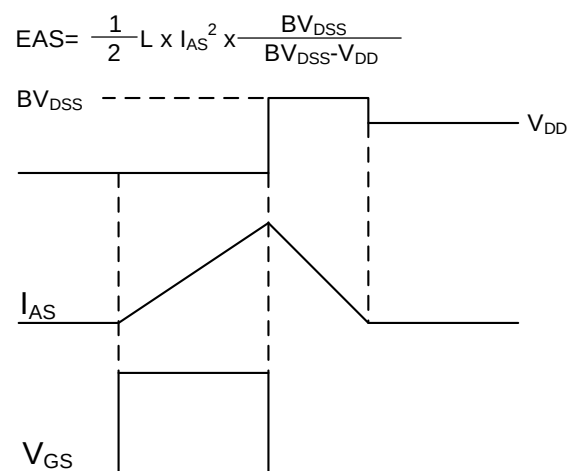
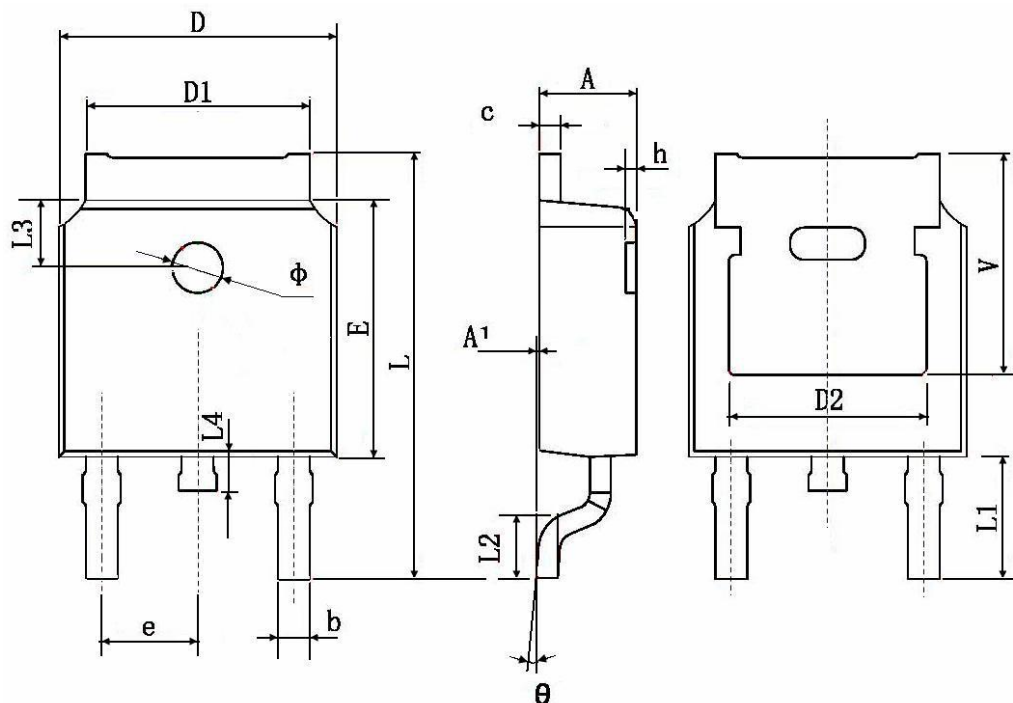


Fig.11 Unclamped Inductive Switching Waveform



N-Channel Enhancement Mode MOSFET

TO-252-2L Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	0.483 TYP.		0.190 TYP.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 TYP.		0.114 TYP.	
L2	1.400	1.700	0.055	0.067
L3	1.600 TYP.		0.063 TYP.	
L4	0.600	1.000	0.024	0.039
Φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 TYP.		0.211 TYP.	



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