



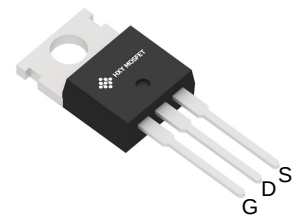
Description

The STP120NF10 use advanced SGT MOSFET

technology to provide low $R_{DS(ON)}$, low gate charge,

fast switching and excellent avalanche characteristics.

This device is specially designed to get better ruggedness
and suitable.



TO-220C

General Features

$V_{DS} = 100V$ $I_D = 70A$

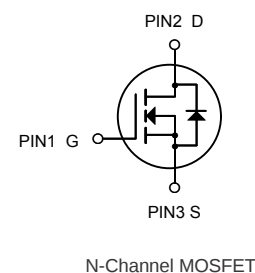
$R_{DS(ON)} < 10.5m\Omega @ V_{GS}=10V$

Application

Battery protection

Load switch

Uninterruptible power supply



Ordering Information

Product ID	Pack	Brand	Qty(PCS)
STP120NF10	TO-220C	HXY MOSFET	50

Absolute Maximum Ratings ($T_C=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	100	V
V_{GS}	Gate-Source Voltage	± 20	V
I_D	Continuous Drain Current@ $T_C=25^\circ C$	70	A
I_{DM}	Puled Drain Current ¹	280	A
EAS	Single Pulse Avalanche Energy ³	110	mJ
$P_D@T_C=25^\circ C$	Total Power Dissipation ⁴	100	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ C$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	64	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Ambient ¹	1.25	$^\circ C/W$



Electrical Characteristics ($T_J=25^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V$, $I_D=250\mu A$	100	---	---	V
$\Delta BV_{DSS}/\Delta T_J$	BVDSS Temperature Coefficient	Reference to 25°C , $I_D=1\text{mA}$	---	0.098	---	$V/^{\circ}\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V$, $I_D=20A$	---	8.5	10.5	$m\Omega$
		$V_{GS}=4.5V$, $I_D=15A$	---	9.5	15	$m\Omega$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}$, $I_D=250\mu A$	1.0	---	2.5	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	-4.57	---	$mV/^{\circ}\text{C}$
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=80V$, $V_{GS}=0V$, $T_J=25^{\circ}\text{C}$	---	---	1	μA
		$V_{DS}=80V$, $V_{GS}=0V$, $T_J=55^{\circ}\text{C}$	---	---	5	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V$, $V_{DS}=0V$	---	---	± 100	nA
R_g	Gate Resistance	$V_{DS}=0V$, $V_{GS}=0V$, $f=1\text{MHz}$	---	0.48	---	Ω
Q_g	Total Gate Charge (10V)	$V_{DS}=50V$, $V_{GS}=50V$, $I_D=10A$	---	31.3	---	nC
Q_{gs}	Gate-Source Charge		---	3.49	---	
Q_{gd}	Gate-Drain Charge		---	7.63	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=50V$, $V_{GS}=10V$, $R_G=4\Omega$ $I_D=10A$	---	16	---	ns
T_r	Rise Time		---	10	---	
$T_{d(off)}$	Turn-Off Delay Time		---	40	---	
T_f	Fall Time		---	6	---	
C_{iss}	Input Capacitance	$V_{DS}=50V$, $V_{GS}=0V$, $f=1\text{MHz}$	---	1368	---	pF
C_{oss}	Output Capacitance		---	451	---	
C_{rss}	Reverse Transfer Capacitance		---	12.9	---	
I_S	Continuous Source Current ^{1,5}	$V_G=V_D=0V$, Force Current	---	---	70	A
I_{SM}	Pulsed Source Current ^{2,5}		---	---	280	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V$, $I_S=1A$, $T_J=25^{\circ}\text{C}$	---	---	1.2	V
t_{rr}	Reverse Recovery Time	$I_F=10A$, $dI/dt=100A/\mu s$, $T_J=25^{\circ}\text{C}$	---	103	---	nS
Q_{rr}	Reverse Recovery Charge		---	187	---	nC

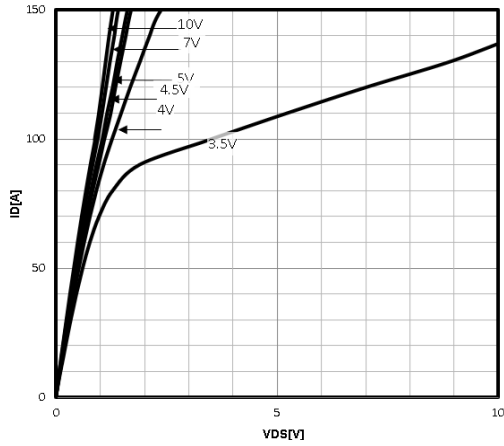
Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is $V_{DD}=25V$, $V_{GS}=10V$, $L=0.1\text{mH}$, $I_{AS}=11A$
- 4.The power dissipation is limited by 150°C junction temperature
- 5 .The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

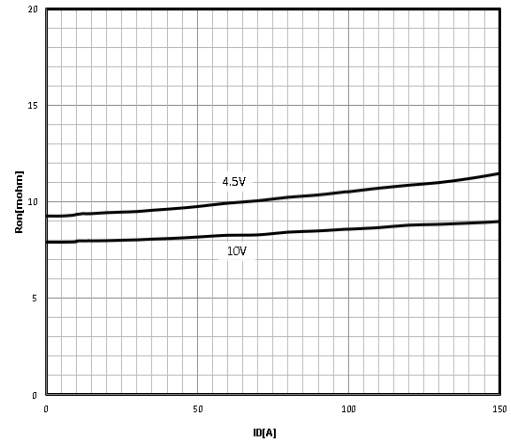


Typical Characteristics

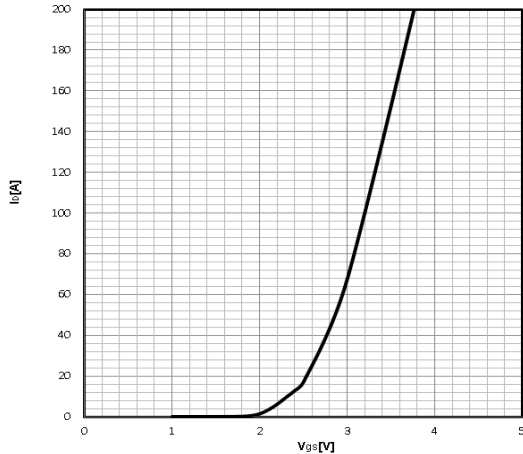
Typ. output characteristics
 $I_D = f(V_{DS})$



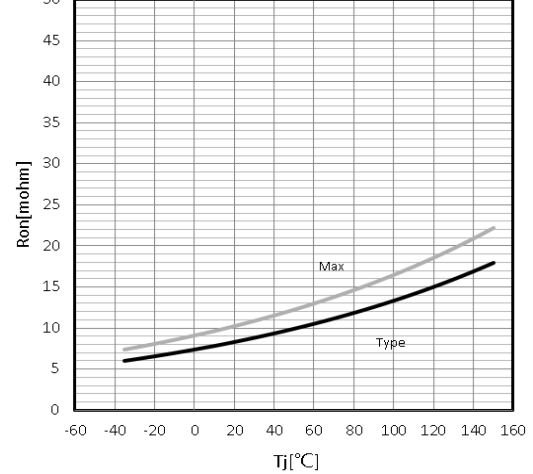
Typ. drain-source on resistance
 $R_{DS(on)} = f(I_D)$



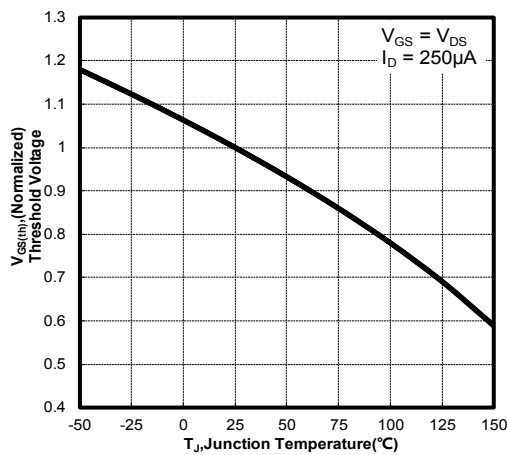
Typ. transfer characteristics
 $I_D = f(V_{GS})$



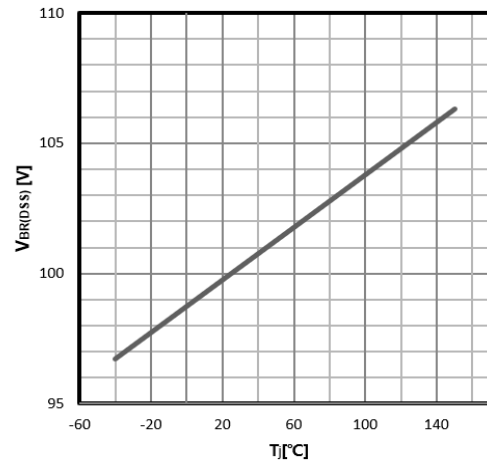
Drain-source on-state resistance
 $R_{DS(on)} = f(T_J); I_D = 20A; V_{GS} = 10V$



Gate Threshold Voltage
 $V_{TH} = f(T_J); I_D = 250\mu A$

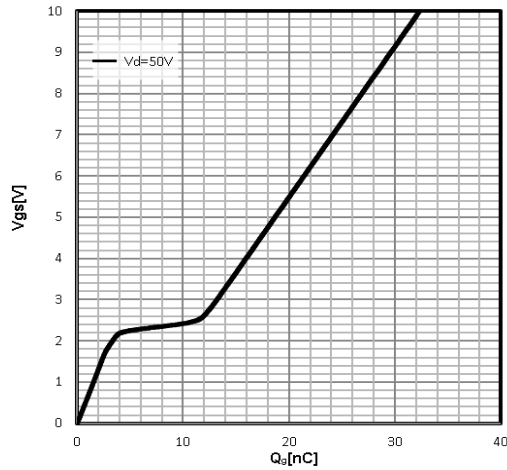


Drain-source breakdown voltage
 $V_{BR(DSS)} = f(T_J); I_D = 250\mu A$

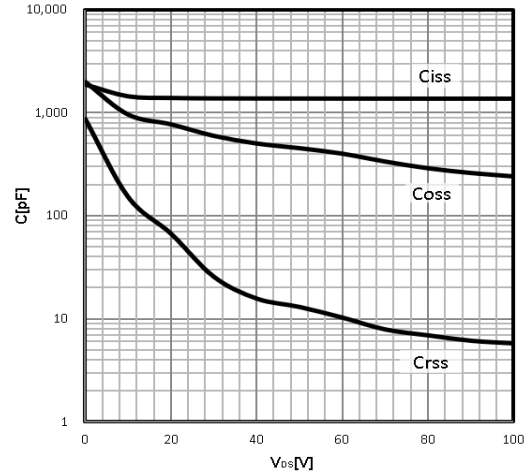




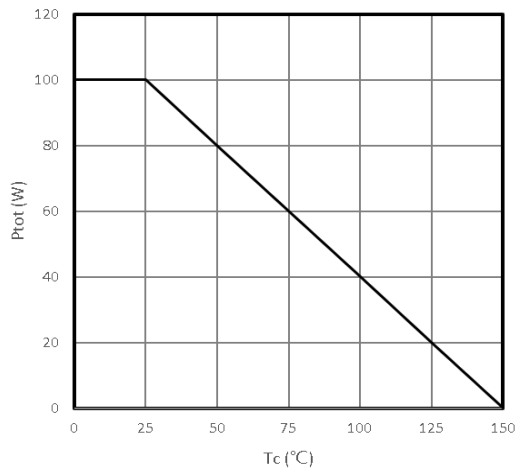
Typ. gate charge
 $V_{GS}=f(Q_g)$; $I_D=10A$



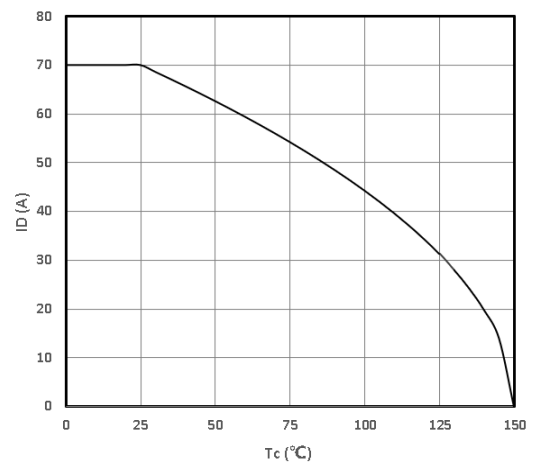
Typ. capacitances
 $C=f(V_{DS})$; $V_{GS}=0V$; $f=1MHz$



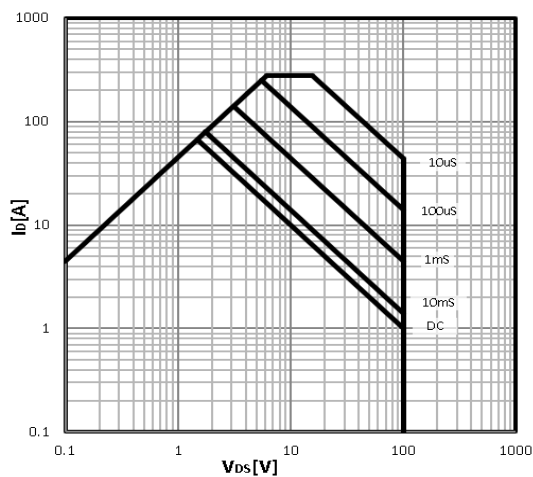
Power Dissipation
 $P_{tot}=f(T_C)$



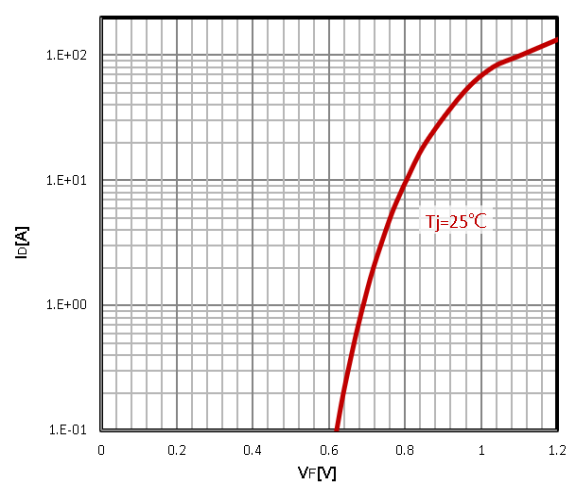
Maximum Drain Current
 $I_D=f(T_C)$



Safe operating area
 $I_D=f(V_{DS})$



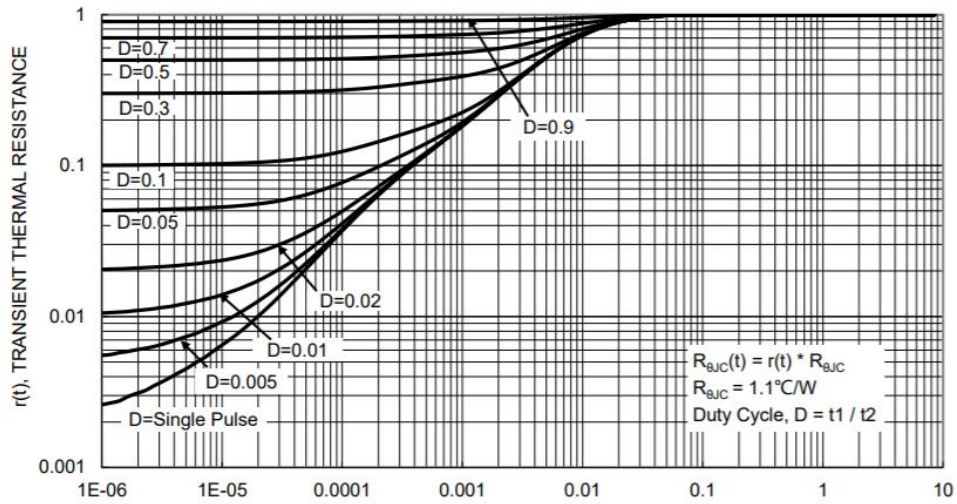
Body Diode Forward Voltage Variation
 $I_F=f(V_{GS})$





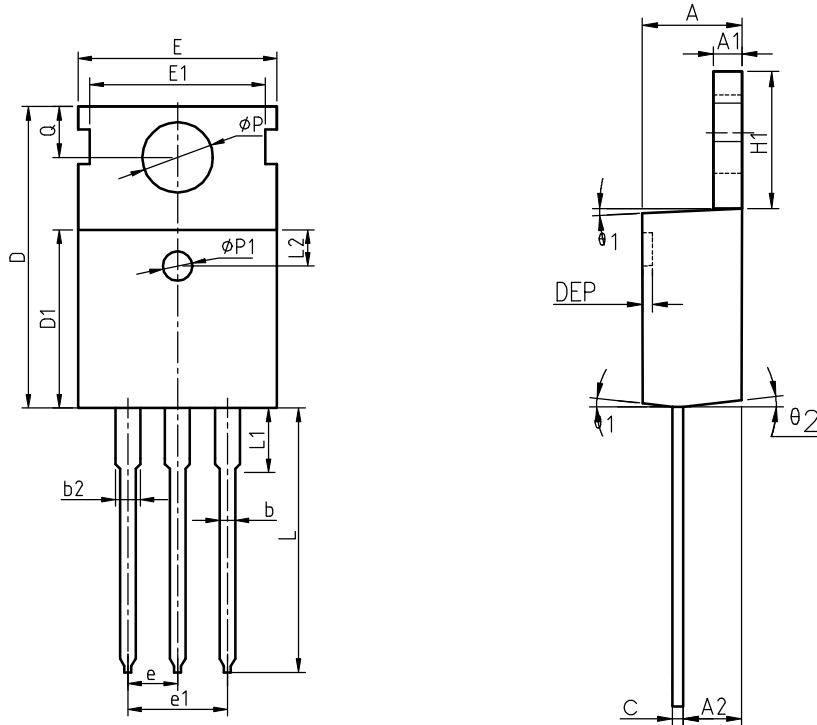
Max. transient thermal impedance

$$Z_{thJC}=f(t_p)$$



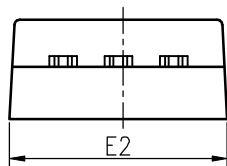


Package Information
TO-220C



COMMON DIMENSIONS

SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	4.40	4.57	4.70	0.173	0.180	0.185
A1	1.27	1.30	1.33	0.050	0.051	0.052
A2	2.35	2.40	2.50	0.093	0.094	0.098
b	0.77	0.80	0.90	0.030	0.031	0.035
b2	1.17	1.27	1.36	0.046	0.050	0.054
c	0.48	0.50	0.56	0.019	0.020	0.022
D	15.40	15.60	15.80	0.606	0.614	0.622
D1	9.00	9.10	9.20	0.354	0.358	0.362
DEP	0.05	0.10	0.20	0.002	0.004	0.008
E	9.80	10.00	10.20	0.386	0.394	0.402
E1	-	8.70	-	-	0.343	-
E2	9.80	10.00	10.20	0.386	0.394	0.402
e		2.54	BSC		0.100	BSC
e1		5.08	BSC		0.200	BSC
H1	6.40	6.50	6.60	0.252	0.256	0.260
L	12.75	13.50	13.65	0.502	0.531	0.537
L1	-	3.10	3.30	-	0.122	0.130
L2		2.50	REF		0.098	REF
P	3.50	3.60	3.63	0.138	0.142	0.143
P1	3.50	3.60	3.63	0.138	0.142	0.143
Q	2.73	2.80	2.87	0.107	0.110	0.113
θ 1	5°	7°	9°	5°	7°	9°
θ 2	1°	3°	5°	1°	3°	5°
θ 3	1°	3°	5°	1°	3°	5°





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