



## Description

The SI7145DP-T1-GE3 uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

## General Features

$V_{DS} = -30V$   $I_D = -100A$

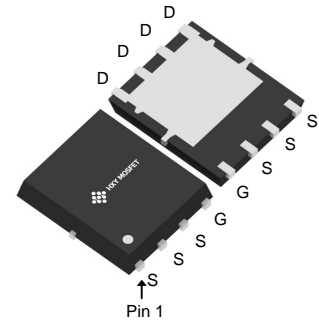
$R_{DS(ON)} < 4\text{ m}\Omega$   $V_{GS} = -10V$

## Application

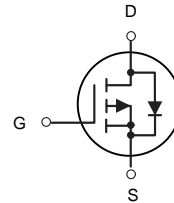
Battery protection

Load switch

Uninterruptible power supply



DFN5X6-8L  
(PowerPAK-SO-8)



P-Channel MOSFET

## Ordering Information

Product ID	Pack	Brand	Qty(PCS)
SI7145DP-T1-GE3	DFN5X6-8L (PowerPAK-SO-8)	HXY MOSFET	5000

## Absolute Maximum Ratings ( $T_C=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	-30	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D@T_C=25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^1$	-100	A
$I_D@T_C=100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^1$	-70	A
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	-250	A
EAS	Single Pulse Avalanche Energy <sup>3</sup>	80	mJ
$I_{AS}$	Avalanche Current	-70	A
$P_D@T_C=25^\circ\text{C}$	Total Power Dissipation <sup>4</sup>	120	W
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient <sup>1</sup>	50	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance Junction-Case <sup>1</sup>	1.6	$^\circ\text{C/W}$



**Electrical Characteristics ( $T_J=25^\circ\text{C}$ , unless otherwise noted)**

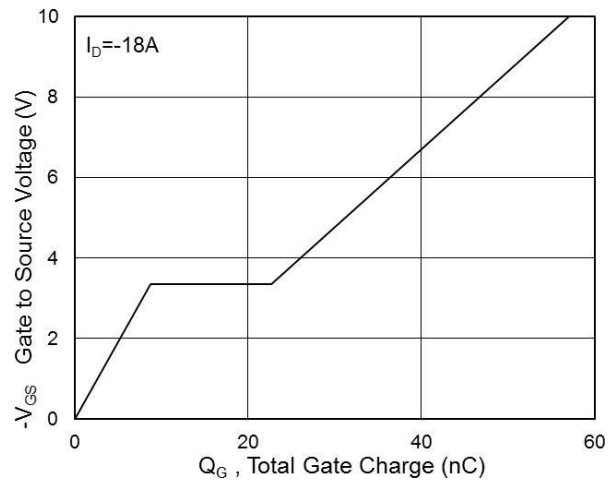
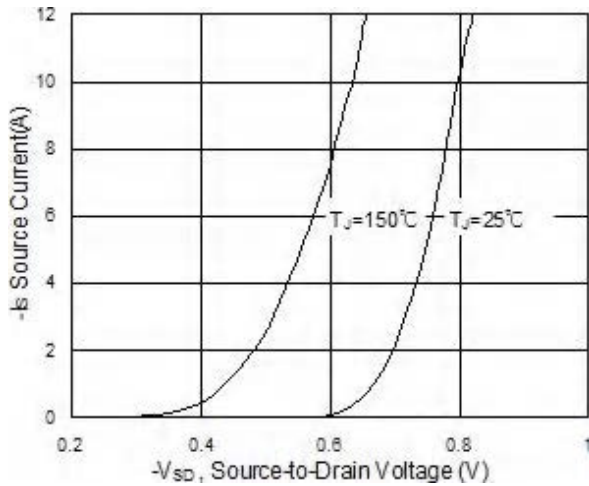
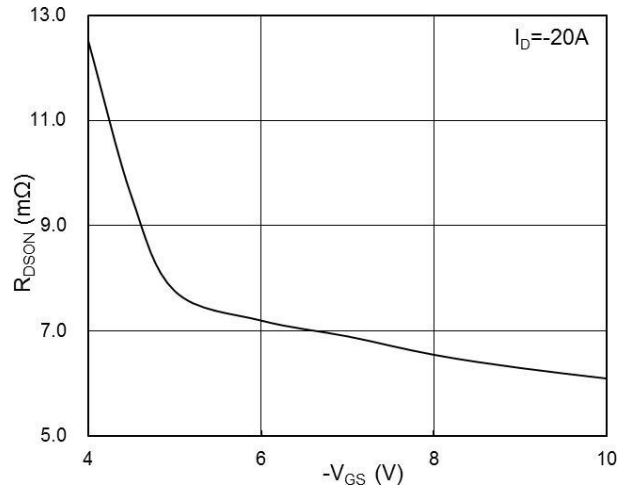
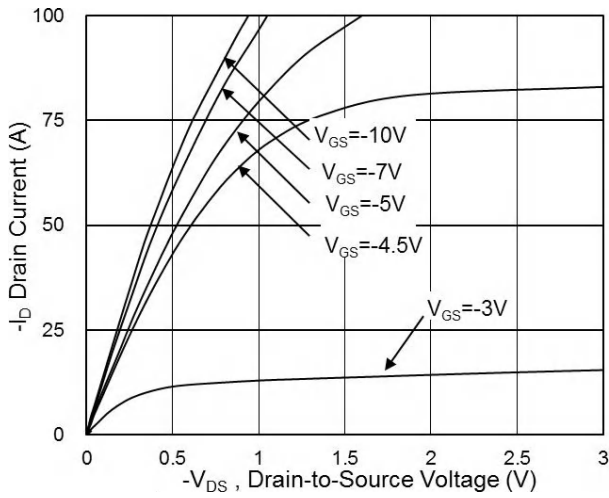
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-30	---	---	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance <sup>2</sup>	$V_{GS}=-10V, I_D=-20A$	---	3	4.0	$m\Omega$
		$V_{GS}=-4.5V, I_D=-15A$	---	4.2	6.0	$m\Omega$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=-250\mu A$	-1.2	---	-2.5	V
$I_{DSS}$	Drain-Source Leakage Current	$V_{DS}=-24V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	-1	$\mu A$
		$V_{DS}=-24V, V_{GS}=0V, T_J=55^\circ\text{C}$	---	---	-5	
$I_{GSS}$	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	$\pm 100$	nA
$R_g$	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1\text{MHz}$	---	1.2	---	$\Omega$
$Q_g$	Total Gate Charge (-10V)	$V_{DS}=-15V, V_{GS}=-10V, I_D=-18A$	---	60	---	nC
$Q_{gs}$	Gate-Source Charge		---	9	---	
$Q_{gd}$	Gate-Drain Charge		---	15	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=-15V, V_{GS}=-10V, R_G=3.3\Omega, I_D=-20A$	---	17	---	ns
$T_r$	Rise Time		---	40	---	
$T_{d(off)}$	Turn-Off Delay Time		---	55	---	
$T_f$	Fall Time		---	13	---	
$C_{iss}$	Input Capacitance	$V_{DS}=-25V, V_{GS}=0V, f=1\text{MHz}$	---	3450	---	pF
$C_{oss}$	Output Capacitance		---	255	---	
$C_{rss}$	Reverse Transfer Capacitance		---	140	---	
$I_S$	Continuous Source Current <sup>1,5</sup>	$V_G=V_D=0V$ , Force Current	---	---	-100	A
$V_{SD}$	Diode Forward Voltage <sup>2</sup>	$V_{GS}=0V, I_S=-1A, T_J=25^\circ\text{C}$	---	---	-1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F=-20A, di/dt=100A/\mu s,$	---	22	---	nS
$Q_{rr}$	Reverse Recovery Charge	$T_J=25^\circ\text{C}$	---	72	---	nC

Note :

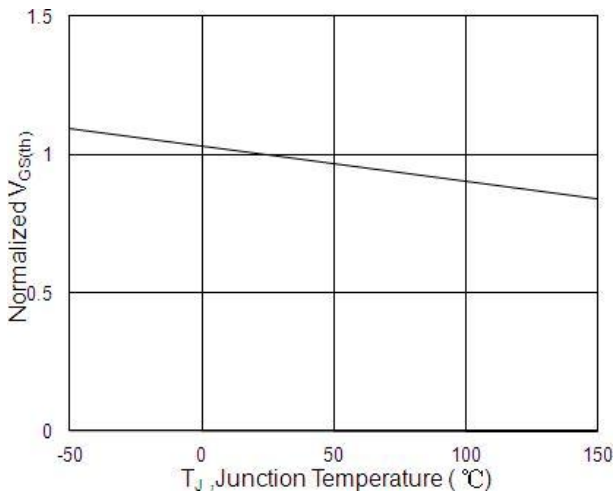
1. The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
2. The data tested by pulsed, pulse width  $\leq 300\mu s$ , duty cycle  $\leq 2\%$
3. The EAS data shows Max. rating. The test condition is  $V_{DD}=-50V, V_{GS}=-10V, L=0.1mH, I_{AS}=-40A$
4. The power dissipation is limited by  $150^\circ\text{C}$  junction temperature
5. The data is theoretically the same as  $I_D$  and  $I_{DM}$ , in real applications, should be limited by total power dissipation
6. The maximum current rating is package limited.



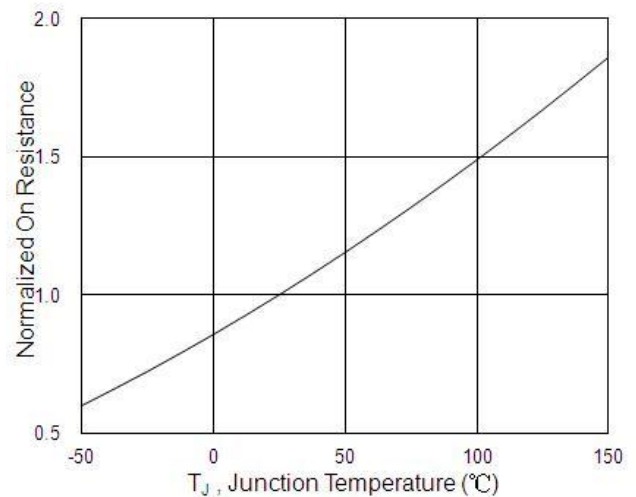
### Typical Characteristics



### Fig.5 Normalized $V_{GS(th)}$ vs $T_J$



### Fig.6 Normalized $R_{DS(on)}$ vs $T_J$



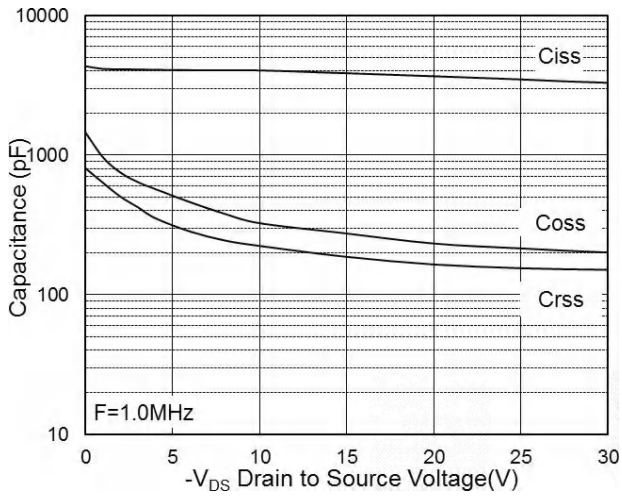


Fig.7 Capacitance

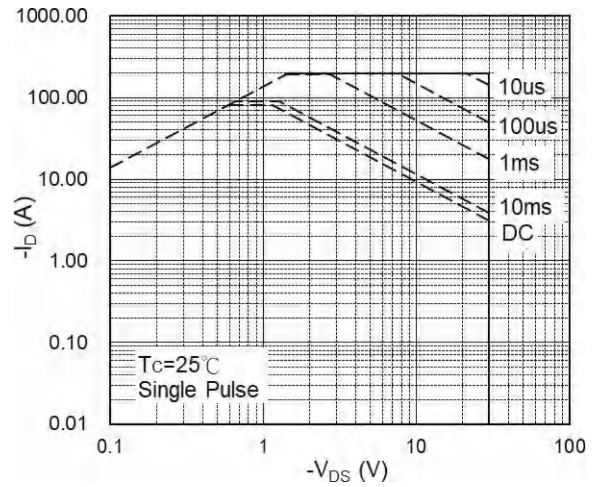


Fig.8 Safe Operating Area

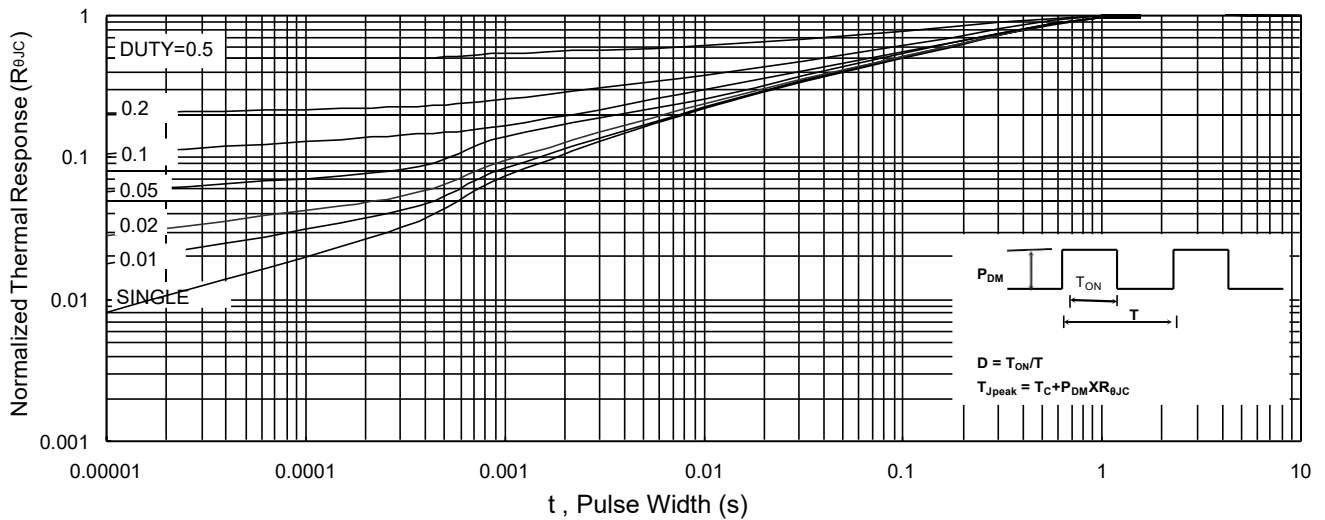


Fig.9 Normalized Maximum Transient Thermal Impedance

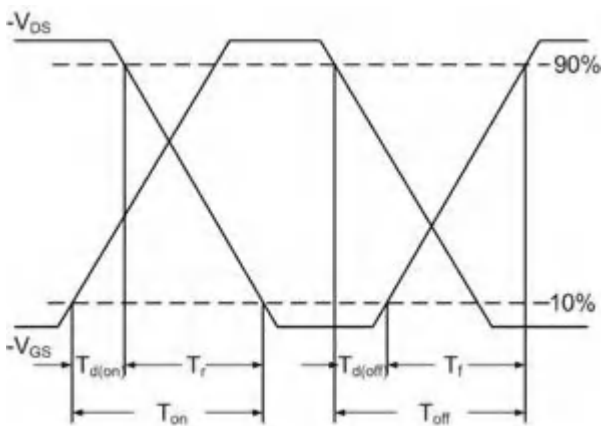


Fig.10 Switching Time Waveform

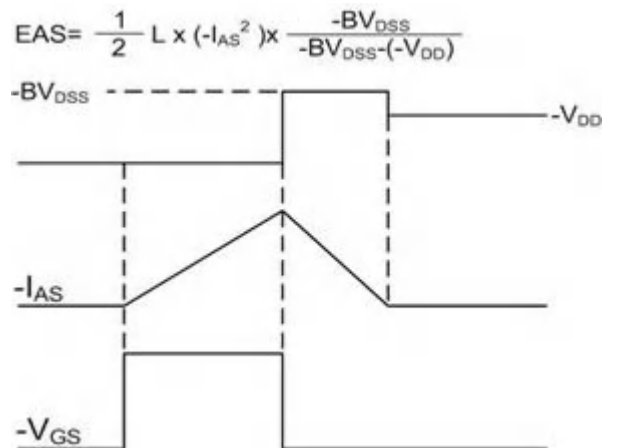
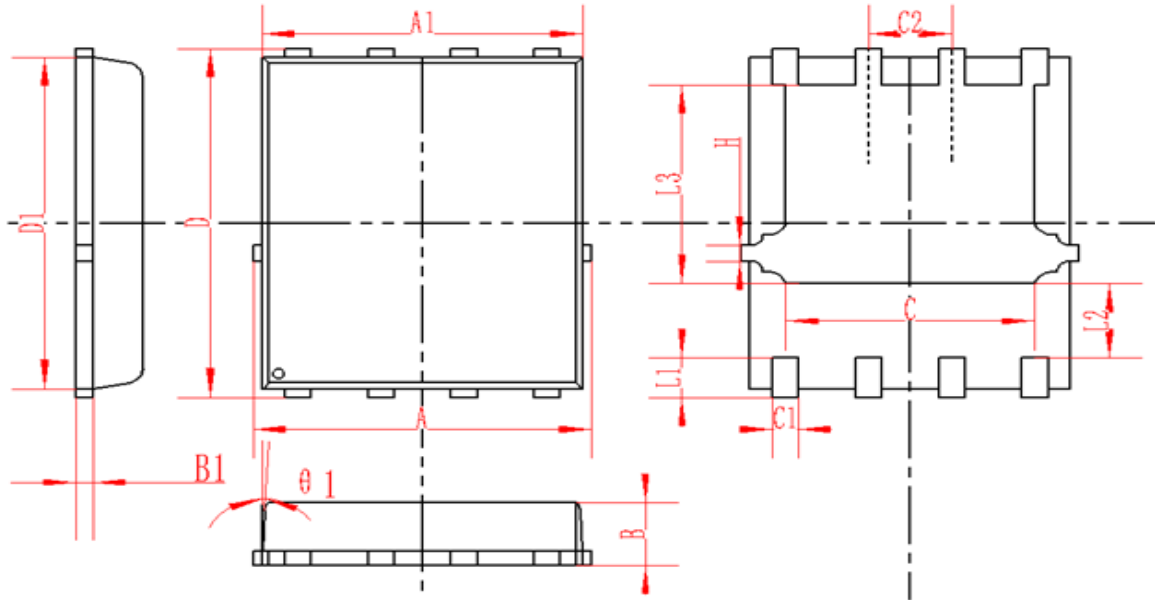


Fig.11 Unclamped Inductive Switching Waveform



**DFN3X3-8L(PowerPAK-SO-8) Package Information**



SYMBOL	MM			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	4.95	5	5.05	0.195	0.197	0.199
A1	4.82	4.9	4.98	0.190	0.193	0.196
D	5.98	6	6.02	0.235	0.236	0.237
D1	5.67	5.75	5.83	0.223	0.226	0.230
B	0.9	0.95	1	0.035	0.037	0.039
B1	0.254REF			0.010REF		
C	3.95	4	4.05	0.156	0.157	0.159
C1	0.35	0.4	0.45	0.014	0.016	0.018
C2	1.27TYP			0.5TYP		
$\theta 1$	8°	10°	12°	8°	10°	12°
L1	0.63	0.64	0.65	0.025	0.025	0.026
L2	1.2	1.3	1.4	0.047	0.051	0.055
L3	3.415	3.42	3.425	0.134	0.135	0.135
H	0.24	0.25	0.26	0.009	0.010	0.010



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