



Description

The SPD03N50C3ATMA1 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

$V_{DS} = 500V$ $I_D = 5A$

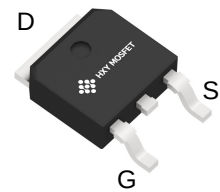
$R_{DS(ON)} < 1.3 \Omega$ @ $V_{GS}=10V$

Application

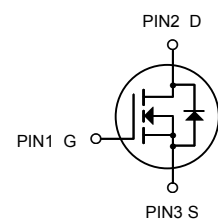
PWM Application

Load switch

Power Management



TO-252-2L
(DPAK)



N-Channel MOSFET

Ordering Information

Product ID	Pack	Brand	Qty(PCS)
SPD03N50C3ATMA1	TO-252-2L (DPAK)	HXY MOSFET	2500

Absolute Maximum Ratings ($T_c=25^{\circ}C$ unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	500	V
V_{GS}	Gate-Source Voltage	± 30	V
$I_D@T_c=25^{\circ}C$	Continuous Drain Current, V_{GS} @ 10V ¹	5	A
$I_D@T_c=100^{\circ}C$	Continuous Drain Current, V_{GS} @ 10V ¹	3	A
I_{DM}	Pulsed Drain Current ²	20	A
EAS	Single Pulse Avalanche Energy ³	137	mJ
$P_D@T_c=25^{\circ}C$	Total Power Dissipation ⁴	83	W
T_{STG}	Storage Temperature Range	-55 to 150	$^{\circ}C$
T_J	Operating Junction Temperature Range	-55 to 150	$^{\circ}C$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	33	$^{\circ}C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	1.5	$^{\circ}C/W$



Electrical Characteristics (T_J=25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	I _D = 250μA, V _{GS} = 0V	500	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 500V, V _{GS} = 0V	-	-	1.0	μA
I _{GSS}	Gate-Body Leakage Current	V _{DS} = 0V, V _{GS} = ±30V	-	-	±100	nA
On Characteristics						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	2	3.4	3.6	V
R _{DS(ON)}	Static Drain-Source ON-Resistance ⁽⁴⁾	V _{GS} = 10V, I _D = 2.5A	-	1.30	1.50	Ω
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{GS} = 0V, V _{DS} = 25V, f = 1MHz	-	582	-	pF
C _{oss}	Output Capacitance		-	42	-	pF
C _{rss}	Reverse Transfer Capacitance		-	4	-	pF
Q _g	Total Gate Charge	V _{GS} = 0 to 10V V _{DS} = 250V, I _D = 2A	-	14	-	nC
Q _{gs}	Gate Source Charge		-	3.3	-	nC
Q _{gd}	Gate Drain("Miller") Charge		-	4	-	nC
Switching Characteristics						
t _{d(on)}	Turn-On DelayTime	V _{GS} = 10V, V _{DD} = 240V I _D = 2A, R _{GEN} = 24Ω	-	12	-	ns
t _r	Turn-On Rise Time		-	17	-	ns
t _{d(off)}	Turn-Off DelayTime		-	45	-	ns
t _f	Turn-Off Fall Time		-	25	-	ns
Drain-Source Diode Characteristics and Max Ratings						
I _S	Maximum Continuous Drain to Source Diode Forward Current		-	-	5	A
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	20	A
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0V, I _S = 5A	-	-	1.2	V
trr	Body Diode Reverse Recovery Time	I _F = 5A, di/dt = 100A/us	-	340	-	ns
Qrr	Body Diode Reverse Recovery Charge		-	2.9	-	μC

- Notes:
1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.
 2. E_{AS} condition: Starting T_J=25°C, V_{DD}=50V, V_G=10V, R_G=25ohm, L=10mH, I_{AS}=5.3A
 3. R_{θJA} is measured with the device mounted on a minimum recommended pad of 2oz copper FR4 PCB
 4. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%.



Typical Characteristics

Figure 1: Output Characteristics

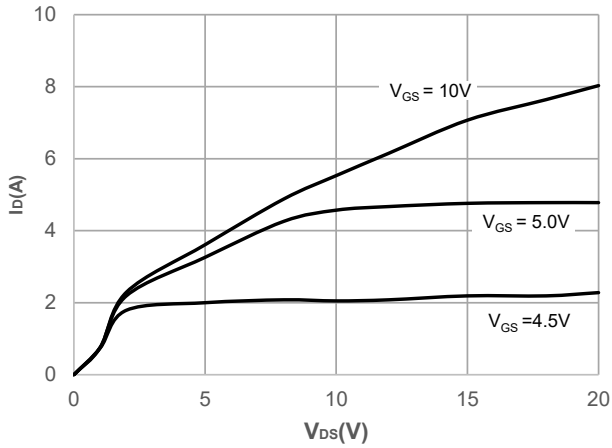


Figure 2: Typical Transfer Characteristics

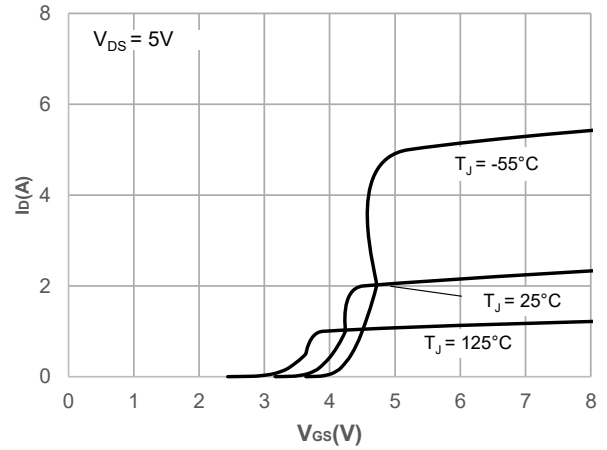


Figure 3: On-resistance vs. Drain Current

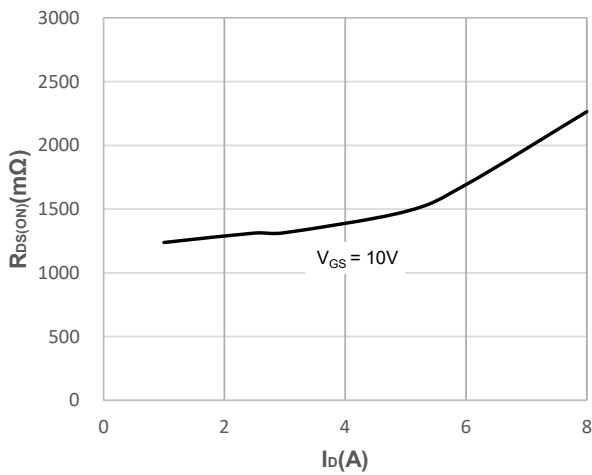


Figure 4: Body Diode Characteristics

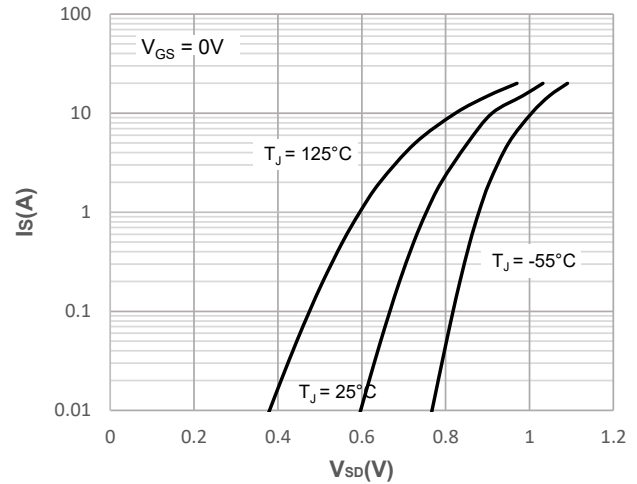


Figure 5: Gate Charge Characteristics

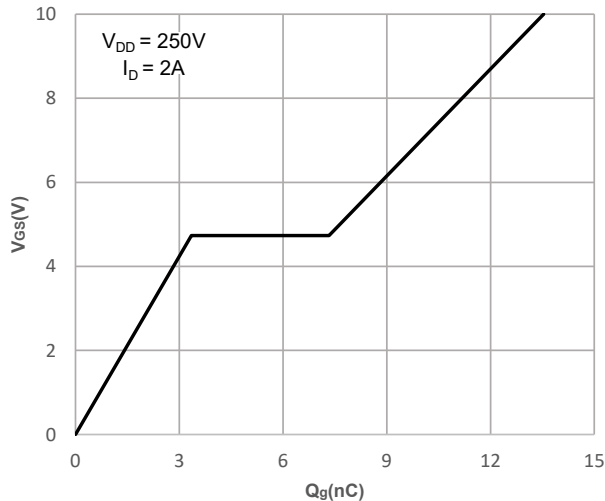


Figure 6: Capacitance Characteristics

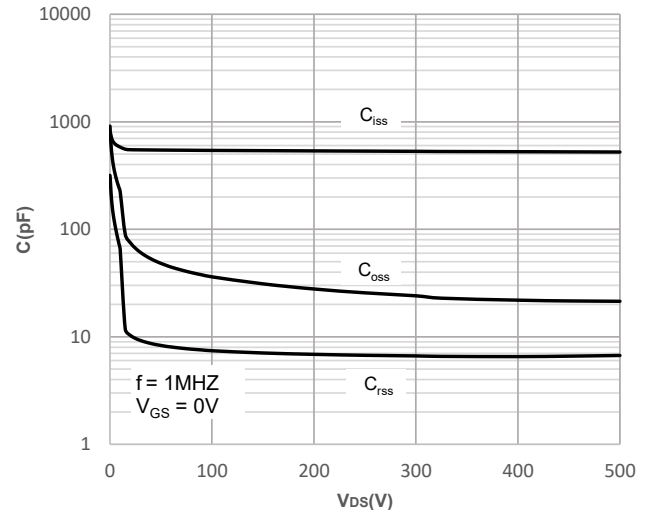




Figure 7: Normalized Breakdown voltage vs. Junction Temperature

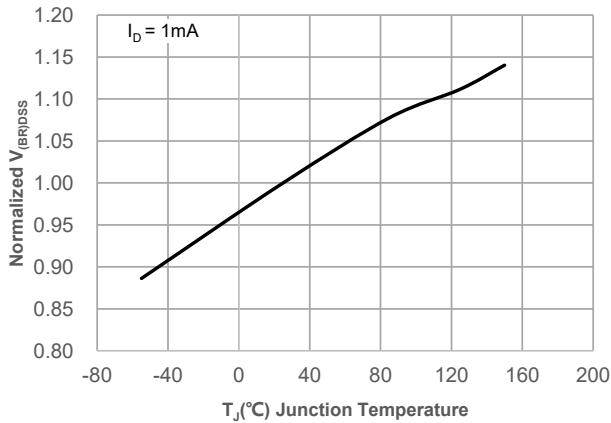


Figure 8: Normalized on Resistance vs. Junction Temperature

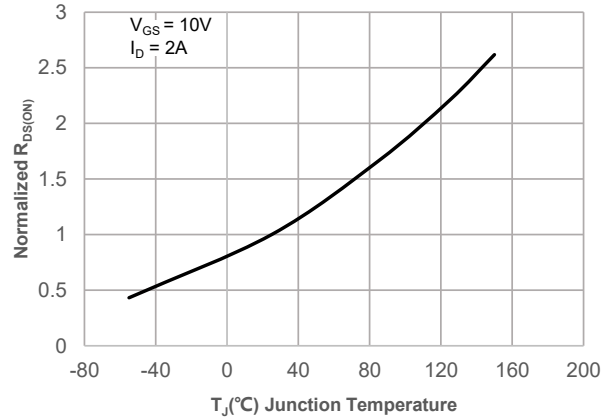


Figure 9: Maximum Safe Operating Area

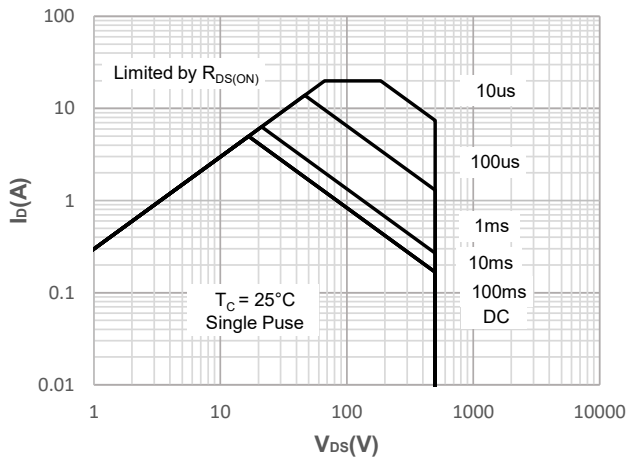


Figure 10: Maximum Continuous Drian Current vs. Case Temperature

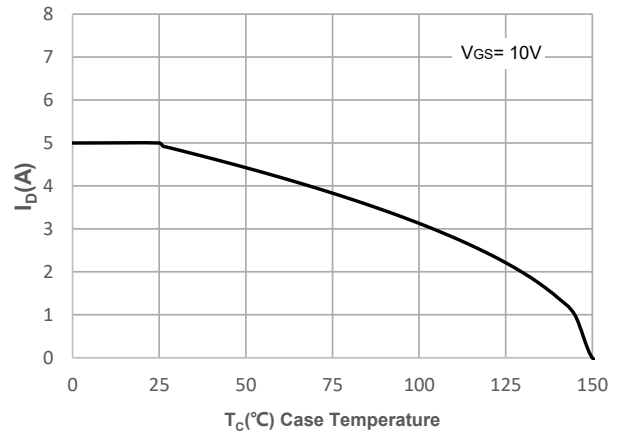


Figure 11: Normalized Maximum Transient Thermal Impedance

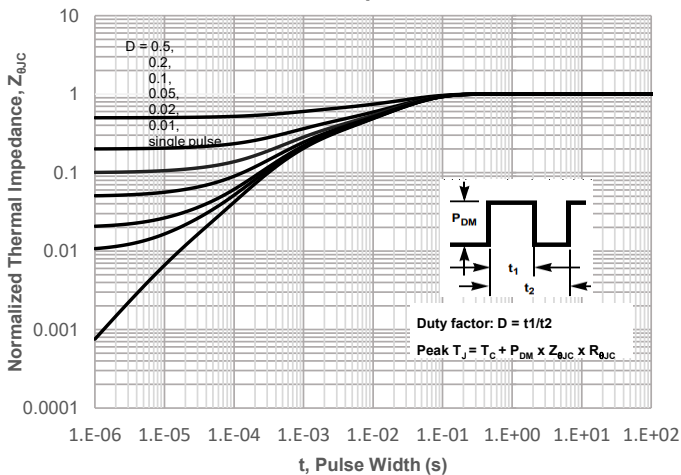
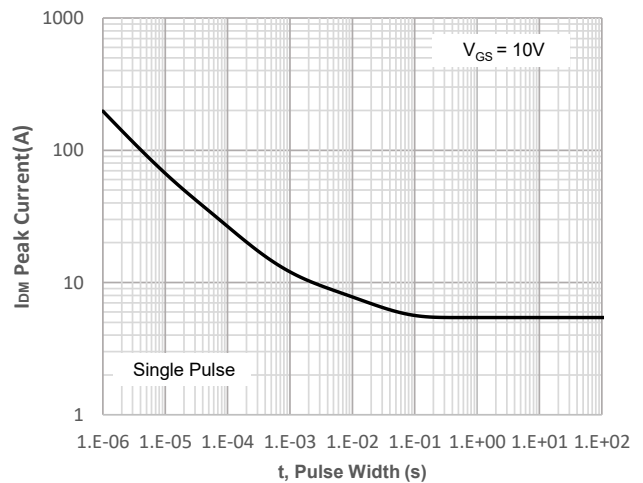


Figure 12: Peak Current Capacity





Test Circuit

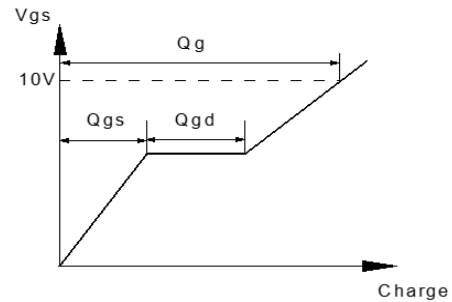
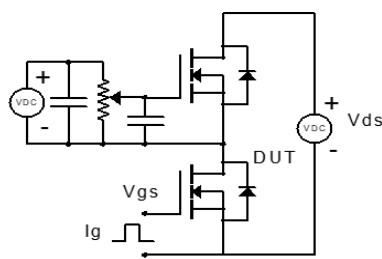


Figure 1: Gate Charge Test Circuit & Waveform

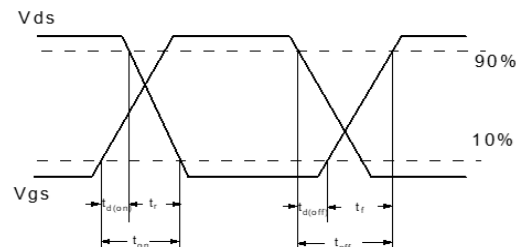
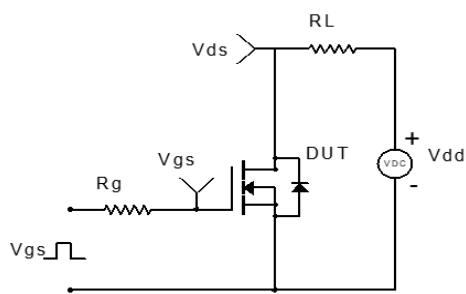


Figure 2: Resistive Switching Test Circuit & Waveform

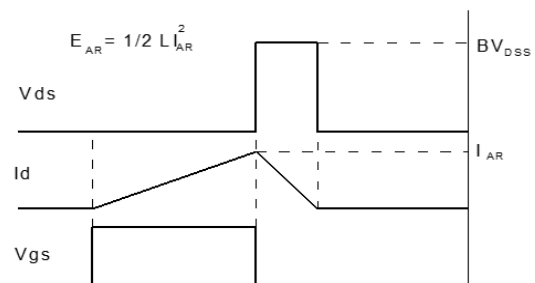
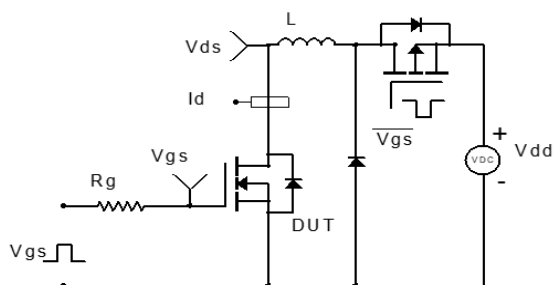


Figure 3: Unclamped Inductive Switching Test Circuit& Waveform

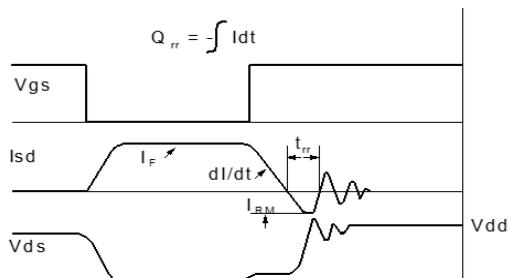
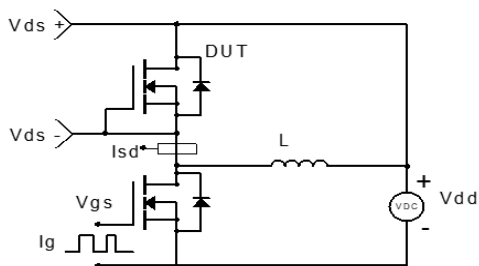
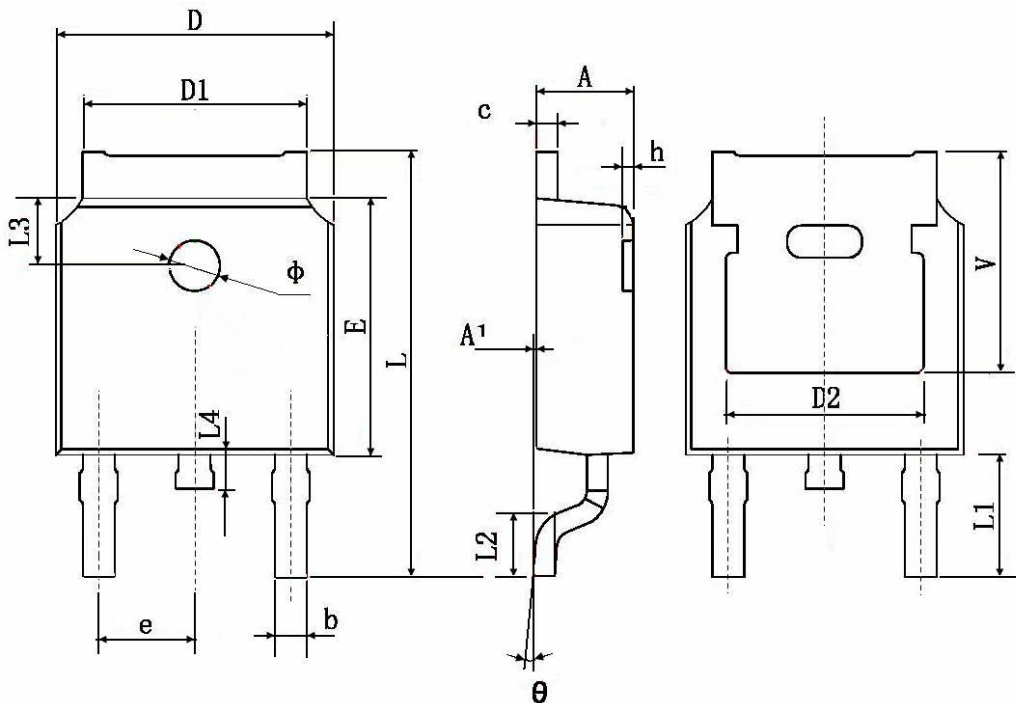


Figure 4: Diode Recovery Test Circuit & Waveform



N-Channel Enhancement Mode MOSFET

TO-252-2L(DPAK) Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	0.483 TYP.		0.190 TYP.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 TYP.		0.114 TYP.	
L2	1.400	1.700	0.055	0.067
L3	1.600 TYP.		0.063 TYP.	
L4	0.600	1.000	0.024	0.039
Φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 TYP.		0.211 TYP.	



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