



Description

The AO4421 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

$V_{DS} = -60V$ $I_D = -6A$

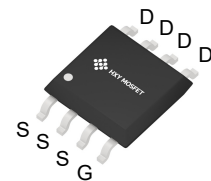
$R_{DS(ON)} < 63m\Omega @ V_{GS}=10V$

Application

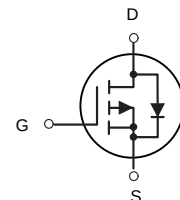
Battery protection

Load switch

Uninterruptible power supply



SOP-8
(SOIC-8)



P-Channel MOSFET

Ordering Information

Product ID	Pack	Brand	Qty(PCS)
AO4421	SOP-8(SOIC-8)	HXY MOSFET	3000

Absolute Maximum Ratings (Tc=25°C unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-60	V
V_{GS}	Gate-Source Voltage	+20	V
$I_D @ T_A=25^\circ C$	Drain Current ³ , $V_{GS} @ 10V$	-6	A
$I_D @ T_A=70^\circ C$	Drain Current ³ , $V_{GS} @ 10V$	-4.8	A
I_{DM}	Pulsed Drain Current ¹	-40	A
$P_D @ T_A=25^\circ C$	Total Power Dissipation	3.1	W
T_{STG}	Storage Temperature Range	-55 to 150	°C
T_J	Operating Junction Temperature Range	-55 to 150	°C
R_{thj-a}	Maximum Thermal Resistance, Junction-ambient ³	40	°C/W



Electrical Characteristics@T_j=25 °C(unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V _{DSS}	I _D =-250 μA, V _{GS} =0V	-60			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-48V, V _{GS} =0V			-1	uA
		V _{DS} =-48V, V _{GS} =0V, T _J =55°C			-5	
Gate-Body leakage current	I _{GSS}	V _{DS} =0V, V _{GS} =±20V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250 μA	-1		-3	V
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =-10V, I _D =-6.2A		53	63	mΩ
		V _{GS} =-10V, I _D =-6.2A T _J =125°C		75	87	
		V _{GS} =-4.5V, I _D =-5A		55		
On state drain current	I _{D(ON)}	V _{GS} =-10V, V _{DS} =-5V	-40			A
Forward Transconductance	g _{FS}	V _{DS} =-5V, I _D =-6.2A		18		S
Input Capacitance	C _{iss}	V _{GS} =0V, V _{DS} =-30V, f=1MHz		2417	2900	pF
Output Capacitance	C _{oss}			179		
Reverse Transfer Capacitance	C _{rss}			120		
Gate resistance	R _g	V _{GS} =0V, V _{DS} =0V, f=1MHz		1.9	2.3	Ω
Total Gate Charge (10V)	Q _g	V _{GS} =-10V, V _{DS} =-30V, I _D =-6.2A		46.5	55	nC
Total Gate Charge (4.5V)				22.7		
Gate Source Charge	Q _{gs}			9.1		
Gate Drain Charge	Q _{gd}			9.2		
Turn-On DelayTime	t _{d(on)}	V _{GS} =-10V, V _{DS} =-30V, R _L =4.7Ω, R _{GEN} =3Ω		9.8		ns
Turn-On Rise Time	t _r			6.1		
Turn-Off DelayTime	t _{d(off)}			44		
Turn-Off Fall Time	t _f			12.7		
Body Diode Reverse Recovery Time	t _{rr}	I _F =-6.2A, di/dt=100A/us		34	42	nC
Body Diode Reverse Recovery Charge	Q _{rr}			47		
Maximum Body-Diode Continuous Current	I _S				-4.2	A
Diode Forward Voltage	V _{SD}	I _S =-1A, V _{GS} =0V			-1	V

Note : The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.



Typical Characteristics

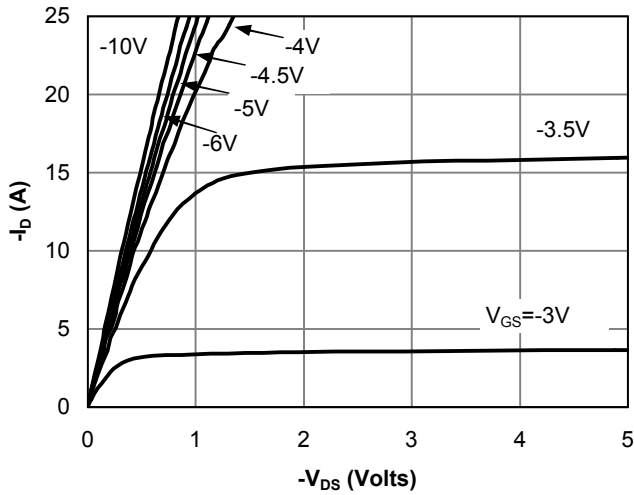


Fig 1: On-Region Characteristics

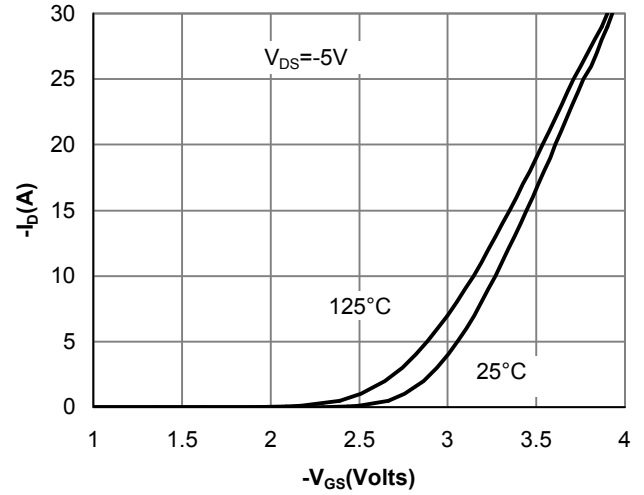


Figure 2: Transfer Characteristics

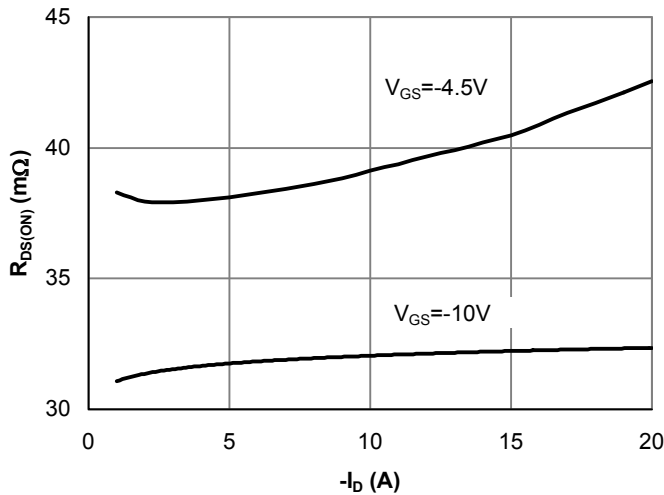


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

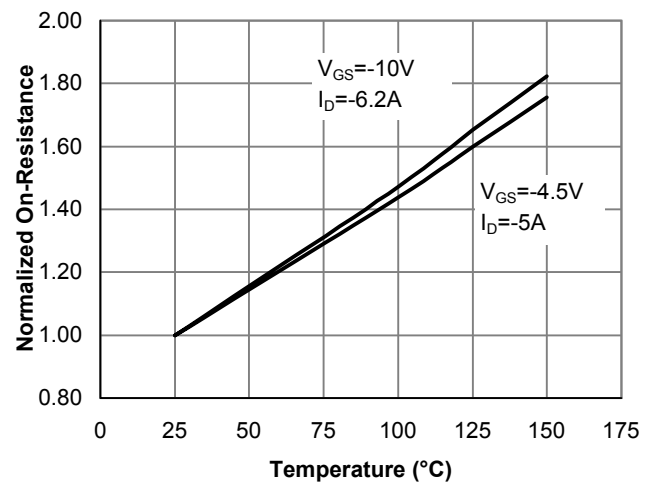


Figure 4: On-Resistance vs. Junction Temperature

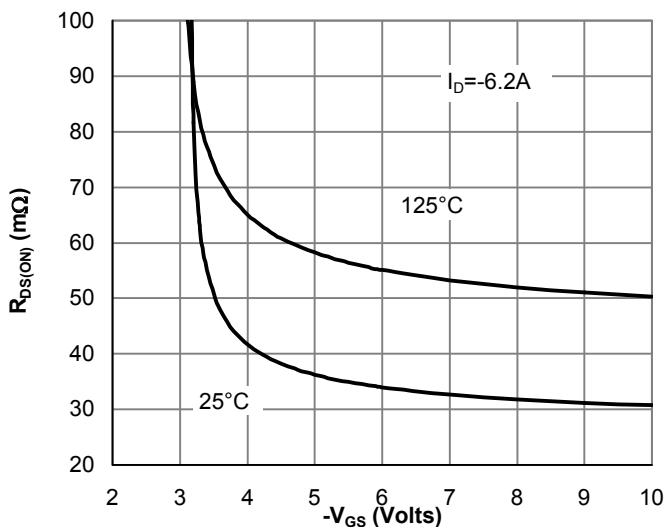


Figure 5: On-Resistance vs. Gate-Source Voltage

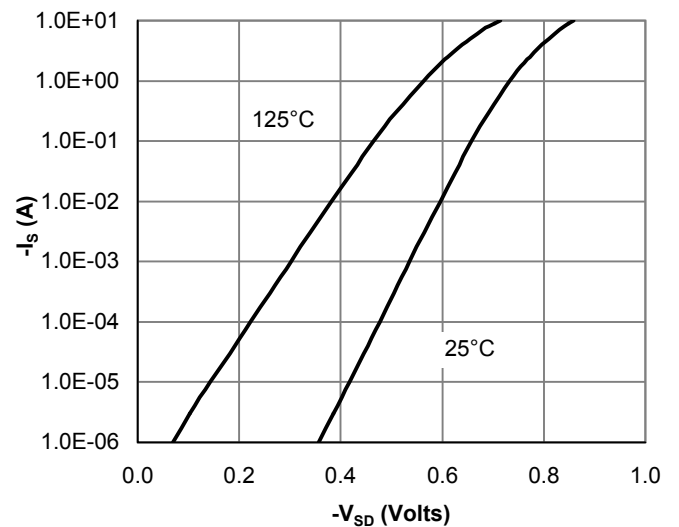


Figure 6: Body-Diode Characteristics

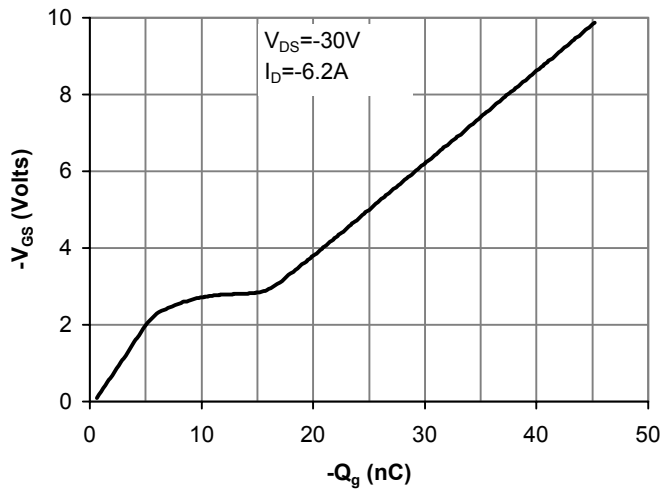


Figure 7: Gate-Charge Characteristics

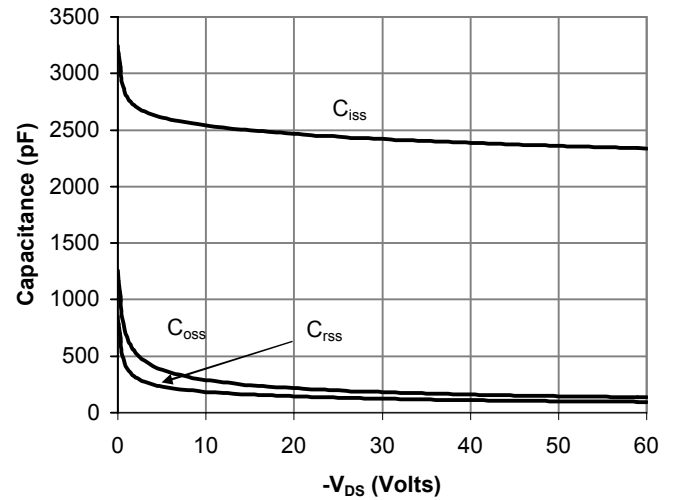


Figure 8: Capacitance Characteristics

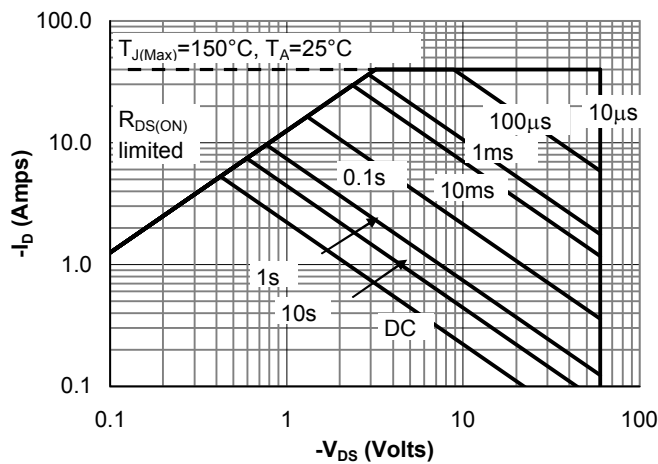


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

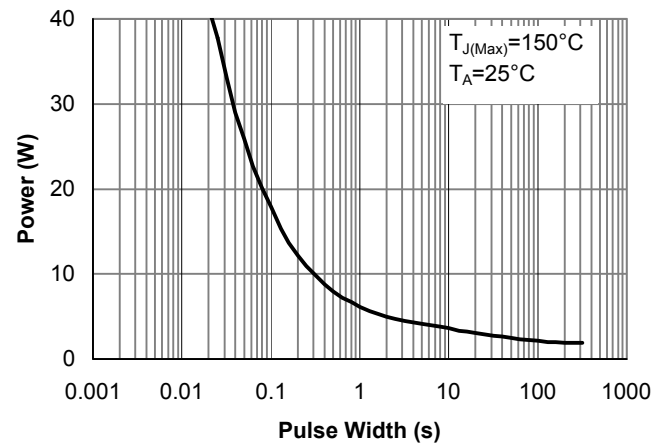


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

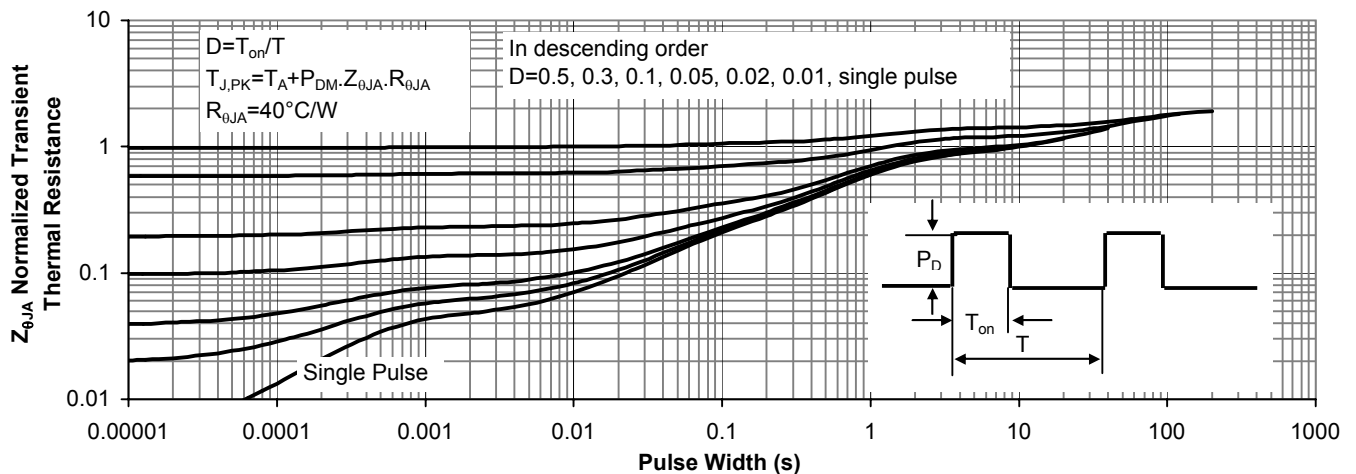
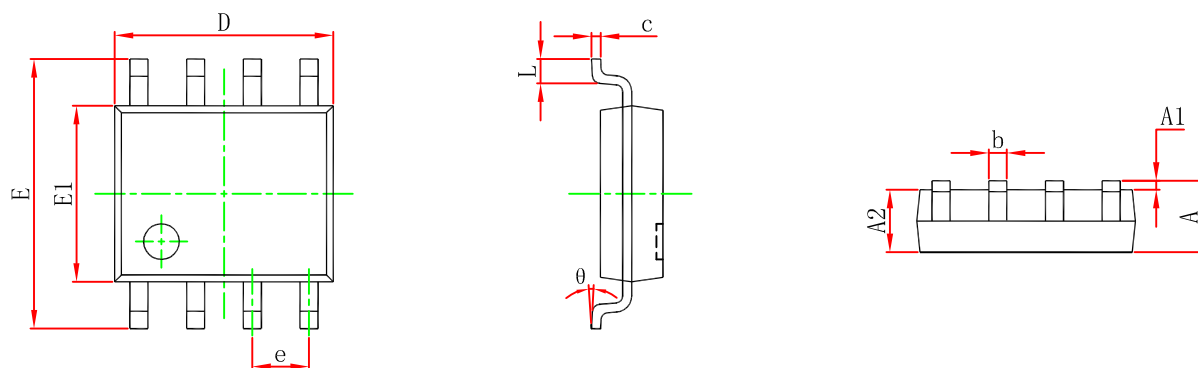


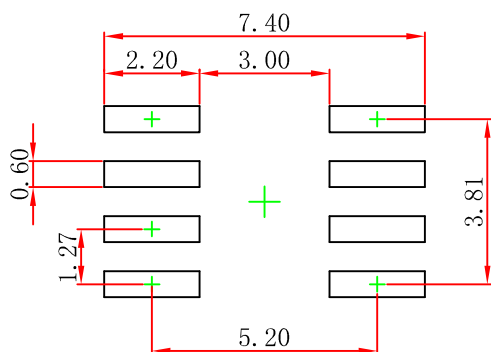
Figure 11: Normalized Maximum Transient Thermal Impedance



SOP-8(SOIC-8) Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270 (BSC)		0.050 (BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



Note:
1. Controlling dimension; in millimeters.
2. General tolerance: $\pm 0.05\text{mm}$.
3. The pad layout is for reference purposes only.



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