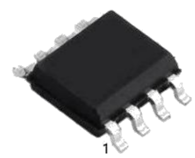
H-Bridge Brushed DC Motor Driver (PWM Control)

Features

- Wide operating voltage range: 8 V to 36 V
- Low $R_{RDS(on)}$ (0.65 Ω @ 2.5 A)
- Low power standby mode
- Adjustable output current limit
- Integrated synchronized regulation
- Forward, reverse, brake and standby modes
- 3.5 A peak current drive, 2.5 A continuous current drive
- Integrated protection features:
  - Undervoltage Lockout (UVLO)
  - Overcurrent protection (OCP)
    Motor short protection
    Motor lead short to ground protection
    Motor lead short to battery protection
  - Over-temperature protection (OTP)



ESOP-8

Ordering Information

DEVICE	Package Type	MARKING	Packing	Packing Qty
DRV8870DDAR/HG	ESOP-8	8870	REEL	4000pcs/reel

General Description

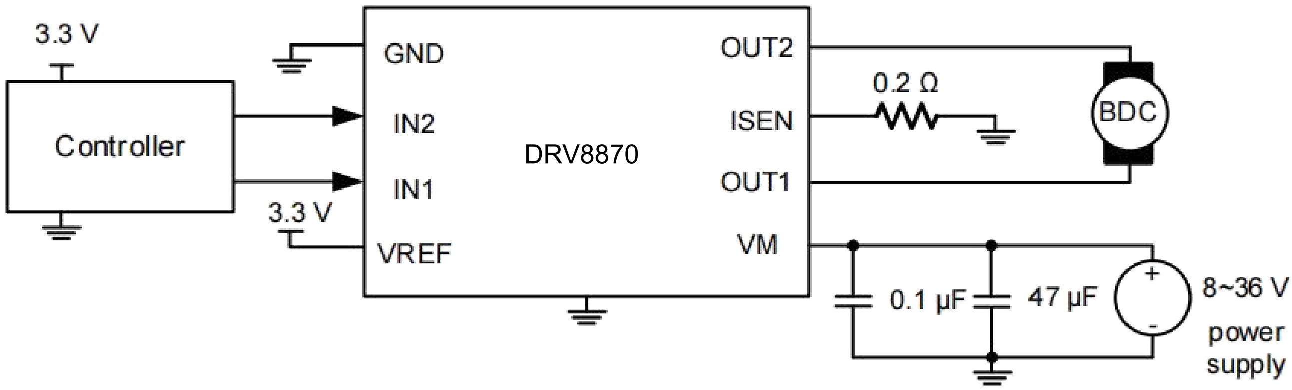
The DRV8870 is used for PWM speed control to drive DC motors, with an integrated H-bridge driver and control circuit, peak output current ±3.5 A, and a maximum operating voltage of 36 V. By inputting PWM control signals through the input ports IN1 and IN2, the speed and direction of DC motors can be controlled. The internal synchronous adjustment circuit of the IC can reduce the power consumption during the PWM control process.

The DRV8870 device features integrated current regulation, based on the analog input VREF and the voltage on the ISEN pin, which is proportional to motor current through an external sense resistor.

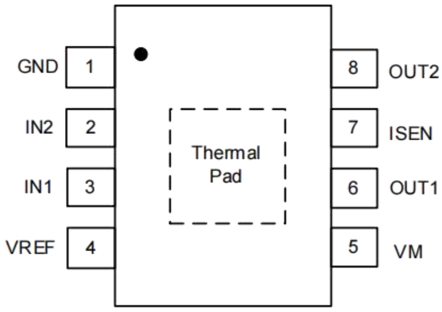
The DRV8870 has an ultra-low power sleep mode. The IC has integrated over-current protection (OCP), motor lead to ground or power short circuit protection, Undervoltage Lockout (UVLO), and over-temperature protection (OTP).

The IC is packaged in an ESOP-8 package with exposed thermal pad to effectively dissipate heat from the chip.

Typical Application



Pin Configurations (Top View)



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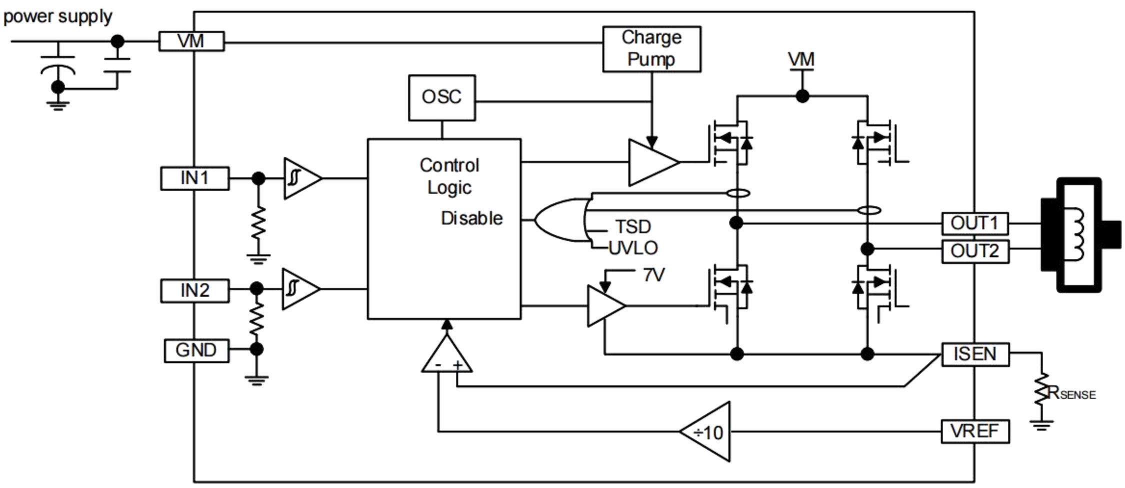
Pin Function

Pin no.	Symbol	Function
1	GND	Logic ground. Connect to board ground.
2	IN2	Input signal 2, internal pull-down resistor included.
3	IN1	Input signal 1, internal pull-down resistor included.
4	VREF	Analog input.
5	VM	Power supply, need to connect the input electrolytic capacitor to avoid instantaneous spikes.
6	OUTI	H - Bridge Output 1, connected to OUT2 via the load.
7	ISEN	Adjust the drive current limit pin to set the current limit threshold by connecting a power resistor to ground, if no current limit adjustment is required, the ISEN pin can be connected directly to ground.
8	OUT2	H - Bridge Output 2, connected to OUT1 via the load.
/	Thermal pad	Heat sink, needs to be connected to ground.

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Condition	Value	Unit
Power Supply Voltage	V_M		40	V
Logic Input Voltage (IN1, IN2)	V_{IN}		-0.3 to 6	
Vref input voltage	V_{REF}		-0.3 to 6	
Current sense input pin voltage (ISEN)	V_S		-0.5 to 0.5	
OUT1,2 output voltage	V_{OUT}		-2 to 36	
Input Current	I_{OUT}	PWM duty cycle 100%	3.5	A
Peak input current	i_{out}	T_W < 500 ns	6	A
Operating Temperature Range(1)	T_A		-40 to 125	°C
Maximum Junction Temperature	$T_{J(MAX)}$		150	°C
Storage temperature	T_{STG}		-55 to 150	°C

Note: Stresses exceeding those listed in the Maximum Rating table may damage the device. Operation beyond the maximum Rating conditions or under harsh conditions may affect product reliability and function.

(1) Operating temperature range: -40°C to +125°C. This product is designed for industrial grade applications. For automotive grade versions compliant with AEC-Q100, please conduct internal screening per the standard or contact our sales team for availability.

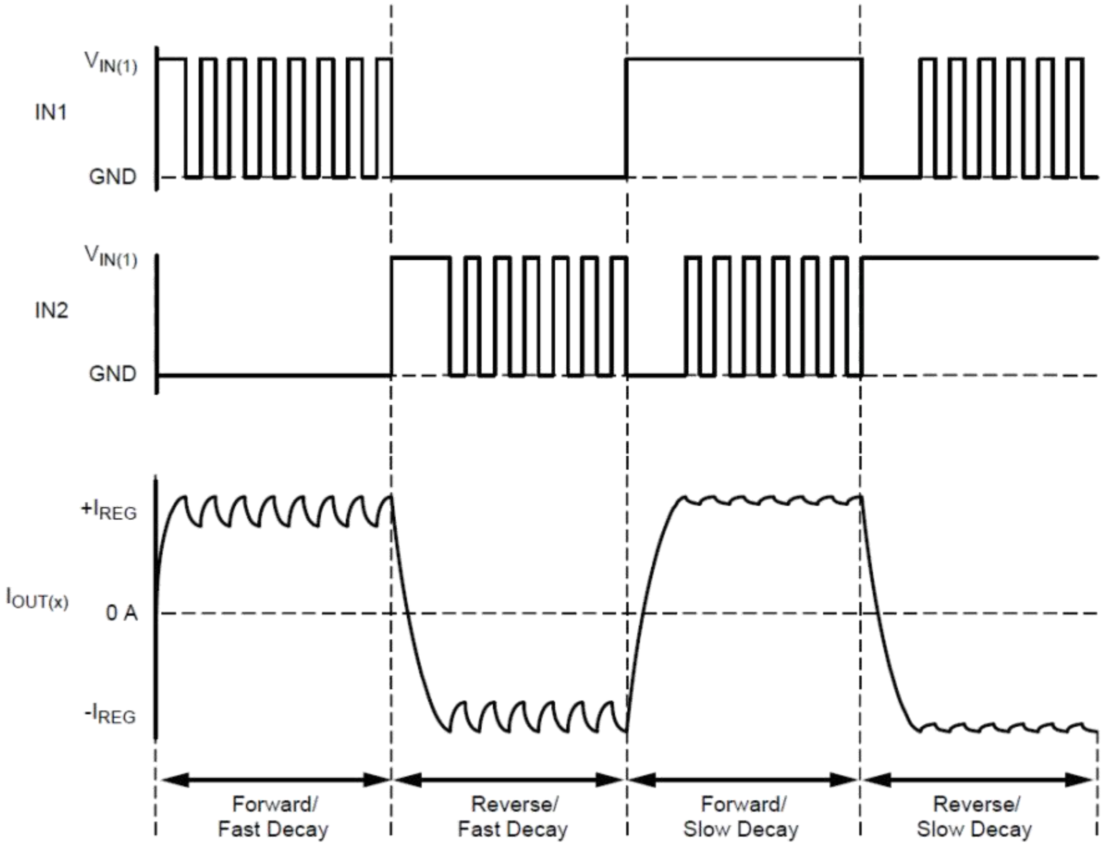
Electrical Characteristics

T_J =25℃, VM =24V, OUT terminal connect 1nF capacitor to ground respectively, special conditions are described separately.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
General Parameters						
VM Operating voltage	V_M		8		36	V
RDS(on) (HS + LS)	$R_{DS(on)}$	I_{OUT} = |2.5 A|, T_J = 25℃		0.6	0.8	Ω
		I_{OUT} = |2.5 A|, T_J = 150℃		1.1	1.5	Ω
VM Operating current	I_{VM}	f_{PWM} < 30 kHz		10	20	mA
		Low power standby mode			10	μA
Body Diode Forward Voltage	V_f	Source diode, I_f = -2.5 A			1.5	V
		Sink diode, I_f = 2.5 A			1.5	V
Logic input parameters						
Input Logic Voltage	$V_{IN(1)}$		2.5			V
	$V_{IN(0)}$				0.8	V
	$V_{IN(STANDBY)}$	Low power standby mode			0.4	V
Input Logic Current	$I_{IN(1)}$	V_{IN} = 2.5 V		40	100	μA
	$I_{IN(0)}$	V_{IN} = 0.8 V		16	40	μA
Input Logic pull-down resistor	$R_{LOGIC(PD)}$	V_{IN} =0V=IN1=IN2		50		kΩ
Input logic hysteresis	V_{HYS}			250	550	mV
Timing parameter						
Output dead time	t_{COD}		50		500	ns
VREF Input Voltage Range	V_{REF}		0		5	V
Current Limiting Gain Ratio	A_V	V_{REF} / I_{SS} , V_{REF} = 5 V	9.5		10.5	V/V
		V_{REF} / I_{SS} , V_{REF} = 2.5 V	9		10	V/V
		V_{REF} / I_{SS} , V_{REF} = 1 V	8		10	V/V
PWM blanking time	t_{BLANK}		2	3	4	μs
PWM off-time	t_{off}		16	25	34	μs
Time to Standby mode	t_{st}	I_{N1} = I_{N2} <$V_{IN(STANDBY)}$		1	1.5	μs
Power-up time	t_{pu}				30	ms
Protection circuit parameters						
VM Undervoltage Lockout	V_{UVLO}	V_M increasing	7	7.5	7.95	V
VM Undervoltage Lockout hysteresis	$V_{UVLOhys}$			500		mV
Thermal shutdown temperature	T_{SD}	Temperature increasing		160		℃
Thermal shutdown hysteresis	T_{SDhys}	Recovery = T_{JTSD} - T_{TSDhys}		15		℃

Typical Performance Characteristics

PWM control diagram



PWM Control Truth Table

IN1	IN2	10 x V_S > V_{REF} (current overrun)	OUT1	OUT2	Functionality
0	1	False	L	H	Reverse (Current OUT2 → OUT1)
1	0	False	H	L	Forward (Current OUT1 → OUT2)
0	1	True	H/L	L	Amplitude Decay, Reverse
1	0	True	L	H/L	Amplitude Decay, Forward
1	1	False	L	L	Brake; low-side slow decay
0	0	False	Z	Z	Coast; H-bridge disabled to High-Z (sleep entered after 1 ms)

Note: Z indicates high impedance.

Functional Description

The DRV8870 is designed to operate brushed DC motors. The output driver H-bridges, consist of low resistance N-channel D-MOSFET with internal synchronization regulation to reduce the power consumption. The H-Bridge output current is regulated by a pulse-width modulation (PWM) with a fixed off-time. the IN1 and IN2 inputs control the bridge separately.

Protection includes thermal shutdown (OTP), Overcurrent protection (OCP), Undervoltage lockout protection (UVLO) prevents damage by holding the output off until the drive reaches sufficient operating voltage.

Low power standby mode

The device enters the low-power standby mode when both input (INx) pins are low for more than 1 ms. The low-power standby mode shuts down most of the internal circuitry, including the charge pump and voltage regulator. When the DRV8870 exits standby mode, it needs to wait for the charge pump to ramp up to a stable voltage (with a maximum delay of 1.5 μs) before it can receive PWM commands.

Internal PWM current control

The IC turns on the diagonal upper and lower FET outputs first, and the current passes through the motor windings and the optional external current sense resistor RS . When the voltage drop across RS exceeds the threshold set by the comparator, the PWM control is suspended, and the lower and upper FETs are turned off automatically (in mixed decay mode).

V_{REF}

Setting the maximum current limit $I_{TripMAX\ (A)}$. via external RS and VREF.

$$I_{TripMAX} = \frac{V_{REF}}{10 \times R_S}$$

Where V_{REF} is the input voltage on the V_{REF} pin, RS is the resistance (Ω) of the sense resistor on the ISEN pin.

Overcurrent protection (OCP)

An internal current monitoring circuit protects the IC from damage due to an output short circuit. When a short circuit is detected, the IC will latch the fault and disable the output. Fault lockout can only be cleared by exiting low power standby mode or by restarting VM power up. During overcurrent protection, limit operating parameters may be exceeded for a short period of time before the IC locks out.

Automatic switching off

If the IC (DIE) temperature rises to approximately 160℃, the H-Bridge outputs will be switched off until the internal temperature drops by more than 15℃ (hysteresis parameter T_{SDhys}). An internal undervoltage protection circuit （UVLO）detects the voltage on VM to prevent switching on the output driver if VM falls below the UVLO threshold.

Braking

IN1 and IN2 input logic are high level at the same time, the IC enters the braking state, OUT1 and OUT2 both output low level, the motor winding current into the slow decay mode. Or after detecting that the output exceeds the limit current, the bridge enables the chop action, the IC will also temporarily enter the braking state (see PWM control truth table). Because the current can be driven in both directions by the DMOS switches, this path setting effectively reduces the BEMF generated by the motor when enabling the Chop action. The maximum current in the path can be approximated as V_{BEMF} / R_L . It is important to note that in the worst braking case (high speed, high inertia loads) this current does not exceed the chip's limiting operating parameters.

Synchronization

When the PWM off cycle is triggered by an internal fixed time off cycle (T_{off}), the load current will remain circulating. The synchronous regulation turns on the D-MOSFETs on the current path during the current decay, bypassing their body diodes with DMOSFETs with low on-resistance $R_{DS(on)}$. This greatly reduces the IC power consumption. When a current decay of 0 is detected, the synchronous regulation is turned off to prevent load current reversal. Figure 1 illustrates the process of synchronous regulation current change during positive rotation .

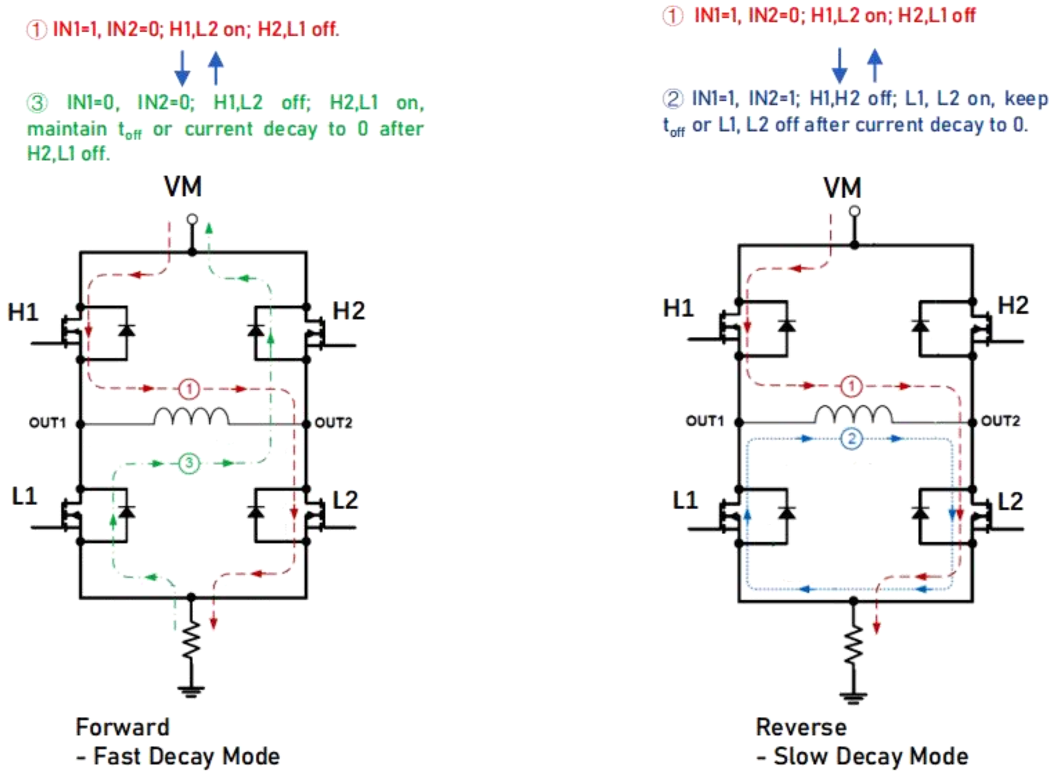


Figure 1. Synchronized regulation current (forward)

Mixed Decay

When the output current exceeds the limit, the IC controls the H-bridge to regulate the drive current in mixed decay mode, as shown in Figure 2. When the output current reaches the set threshold $I_{TripMAX}$, the device enters into the fast decay mode, which lasts for 50% of the fixed off time (T_{off}) . After that the device switches to the slow decay mode for the remaining off time, as in Figure 2(b). During the transition from fast to slow decay, the H-bridge is forced to disconnect T_{COD} , preventing the upper and lower FETs from passing through. During this "dead zone", the synchronization is not effective and the device operates only in fast decay and slow decay. Figure 3 illustrates the current change during the mixed decay process after the forward current is overrun.

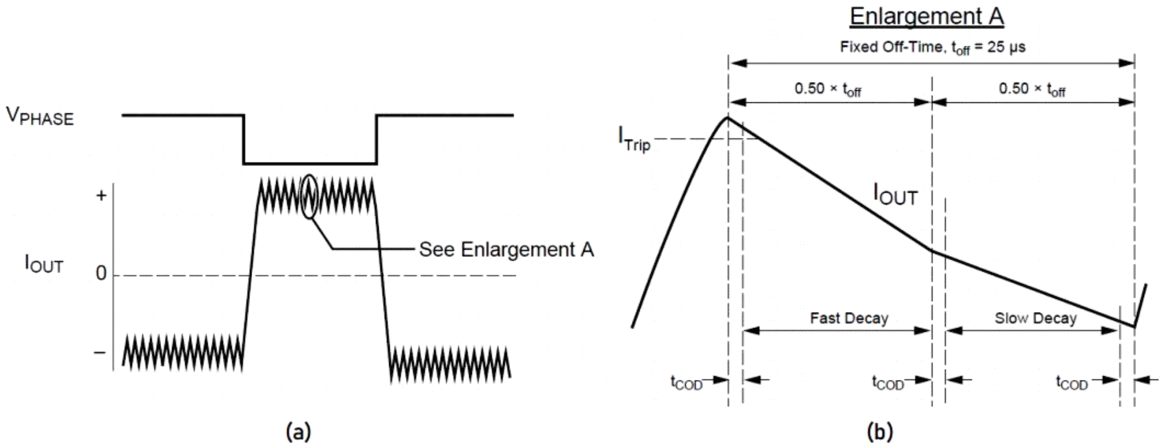


Figure 2. Hybrid attenuation mode clipping drive current

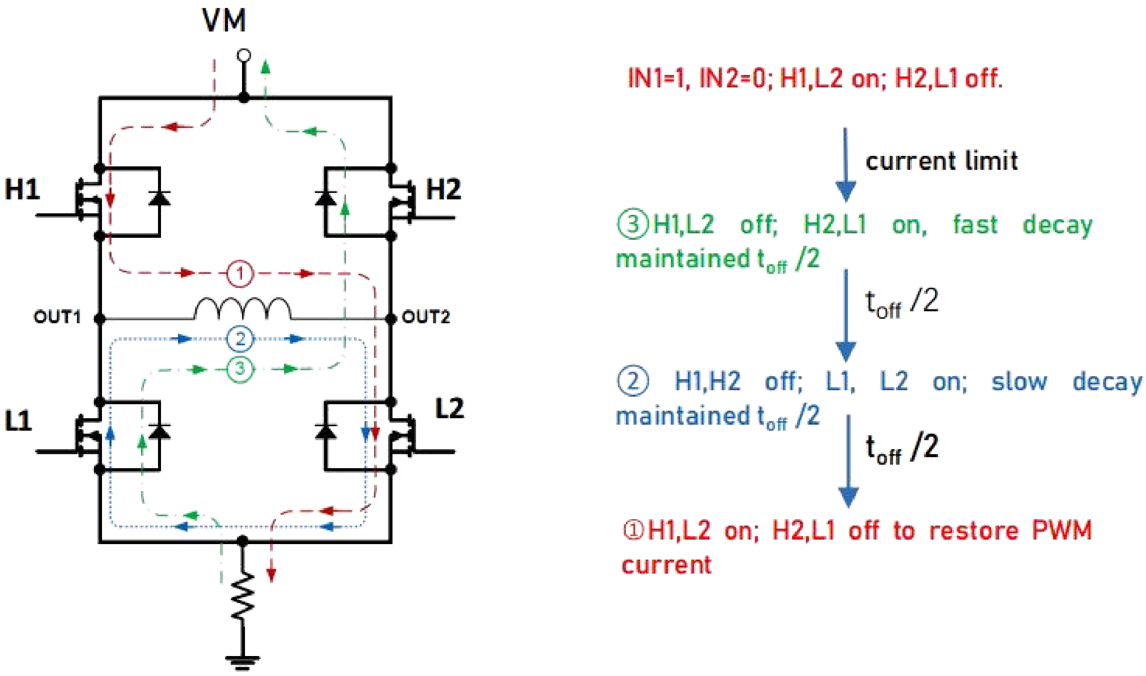


Figure3. Mixed decay process after over current (Forward)

Application notes

Current Sampling Pin (ISEN)

To use PWM motor control, place a low resistance resistor RS between the ISEN pin and ground for current sampling. In order to minimize the effect of the resistive voltage drop of the ground resistor on the current sampling of RS , RS should have a separate connection to the star ground point as shown in Figure 4, which needs to be as short as possible because the PCB ground resistance has a large effect on the lowresistance resistor and must be taken into account.

The voltage can be sampled directly at both ends of Rs. It is not recommended to add a sense resistor to the GND pin. when selecting the resistance value of the resistor, make sure that the voltage at the ISEN pin does not exceed the maximum voltage ±500 mV at the maximum load. During the overcurrent protection occurs, it is possible that this maximum voltage may be exceeded for a short period of time.

Ground

The star ground point should be as close as possible to the DRV8870. The ground below the exposed thermal pad of the IC is a good location for the star ground point.

PCB Layout

The PCB should have a thick ground plane. For optimum electrical and thermal performance, the DRV8870 must be soldered directly to the PCB. At the bottom of the DRV8870 package is an exposed thermal pad that provides a path for enhanced heat dissipation. The thermal pad must be soldered directly to an exposed copper plane on the PCB for optimal heat transfer. Thermal vias are used to transfer heat to other layers of the PCB. It is recommended to increase the area of the top and bottom layers of the PCB to improve heat dissipation performance; keep the copper planes from the thermal pad to the rest of the board continuous; If these planes are interrupted, the thermal resistance will increase.

Input capacitor C2 affects the instantaneous load capacity, to avoid spikes, The recommended value of 100uF/50V or more, CI and C2 need to be placed close to the VM pins; recommended PCB thermal pads using a diameter of 20mil, the hole size of 8mil heat dissipation holes, reduce thermal resistance. Highcurrent paths (OUT1, OUT2, ISEN, VM etc.) as much as possible to increase the line width.

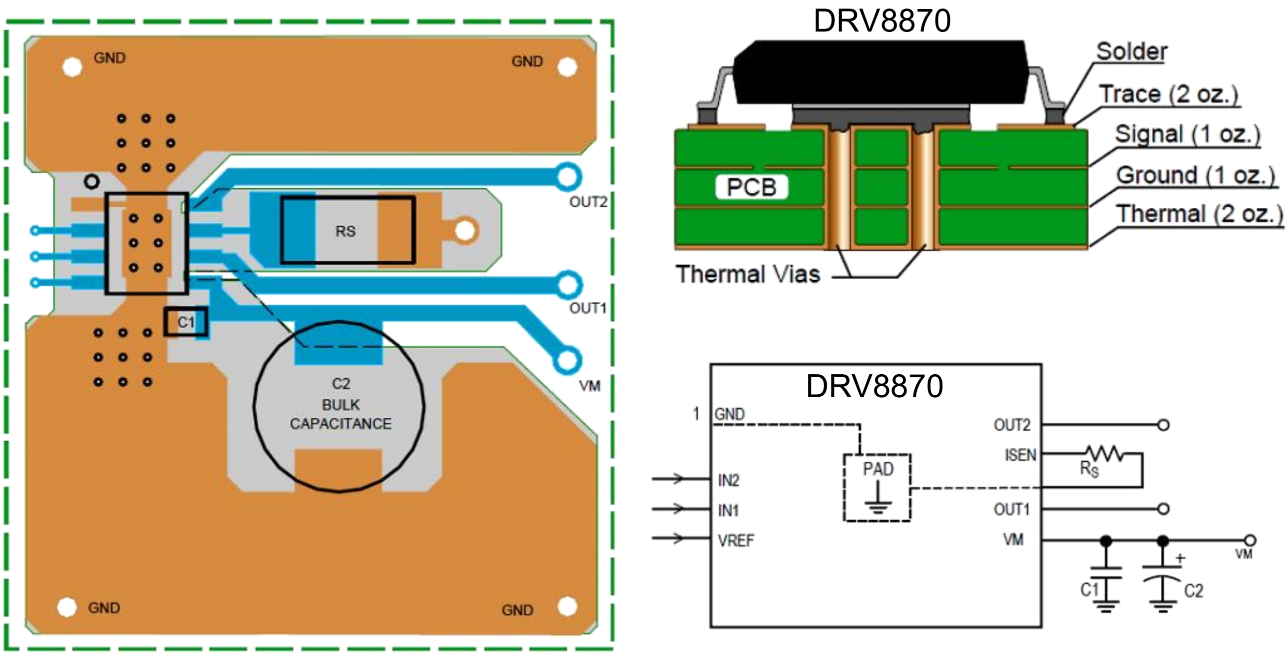


Figure 4. PCB Layout

Bill of Materials

SN	Name	Specification	Descriptions	Unit
1	R_S	0.25 (for VREF = 5 V, IOUT = 2 A)	2512, 1 W, 1% or better, carbon film chip resistor	Ω
2	C1	0.22	X5R minimum, 50 V or greater	μF
3	C2	100	Electrolytic, 50 V or greater	μF

Physical Dimensions

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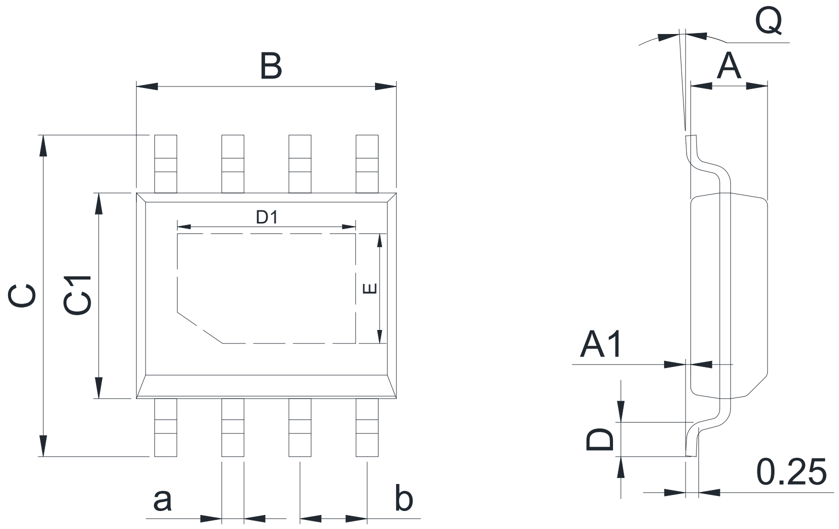

Dimensions In Millimeters(ESOP-8)										
Symbol:	**A**	**A1**	**B**	**C**	**C1**	**D**	**D1**	**E**	**Q**	**a**	**b**
Min:	1.35	0.05	4.90	5.80	3.80	0.40	3.20	2.31	0°	0.35	1.27 BSC
Max:	1.55	0.20	5.10	6.20	4.00	0.80	3.40	2.51	8°	0.45	

Revision History

REVISION NUMBER	DATE	REVISION	PAGE
V1.0	2018-9	New	1-14
V1.1	2025-9	Document Reformatting	1-14

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