钛地半导体
Tudi Semiconductor

Product Specification

TUDI-DS2431

1024 Bit 1-Wire EEPROM Memory

网址 www.sztdbdt.com

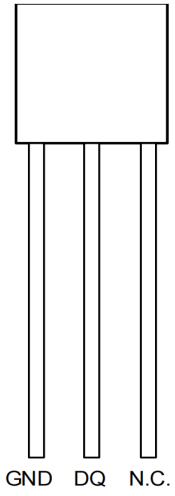
用芯智造·卓越品质

semiconductor device manufacturer

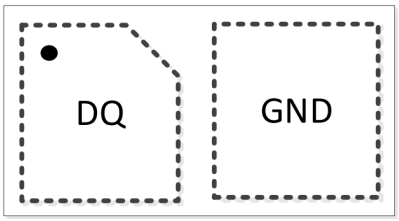
- Design
- research and development
- production
- and sales

Features

- Easily Add Traceability and Relevant Information to Any Individual System
- 1024 Bits of EEPROM Memory Partitioned Into Four Pages of 256 Bits
- Individual Memory Pages Can Be Permanently Write Protected or Put in EPROM-Emulation Mode (Write to 0)
- Switchpoint Hysteresis and Filtering to Optimize Performance in the Presence of Noise
- Minimalist 1-Wire Interface Lowers Cost and Interface Complexity
- IEC 1000-4-2 Level 4 ESD Protection (±8kV Contact, ±15kV Air, typ)
- Reads and Writes Over a Wide Voltage Range from 2.5V to 5.5V from -45°C to +125°C
- Communicates to Host with a Single Digital Signal at 15.4kbps or 125kbps



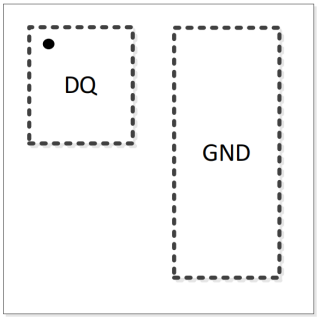
TO92



SFN2(3.5mm*6.5mm*0.75mm)

Application

- Accessory/PCB Identification
- Medical Sensor Calibration Data Storage
- Analog Sensor Calibration Including IEEEP1451.4 Smart Sensors
- Ink and Toner Print Cartridge Identification
- After-Market Management of Consumables



SFN2(6mm*6mm*0.75mm)

DFN6(4mm*4mm*0.75-0.95mm)

Pin description

Pin		Name	Description
TO-92	DFN6		
-	3,4,5,6	N.C.	Unused pin or no connection required
3	-	N.C.	Grounded or floating
2	2	DQ	Data input/output pin, drain pin, requires an external pull-up resistor
1	1	GND	Ground pin

Description

The DS2431 is a 1024-bit EEPROM that communicates with a host using the standard 1-Wire protocol. It consists of four memory pages, each 256 bits. Data is first written to an 8-byte buffer and then copied to the EEPROM memory after verification. feature is that the four memory pages are independent of each other, and write protection or EPROM emulation mode can be set individually. In EPROM storage mode, the state of bits can only change from 1 to 0. The DS2431 communicates via a single 1-Wire bus. Communication uses the standard 1-Wire protocol. Each has a unique, unchangeable 64-bit ROM address code, which is written into the chip by the factory using photolithography. In a multi-point -Wire network environment, this address code is used to address the device.The DS2431 contains a 1024-bit EEPROM, an 8-byte control configuration (up to 7 bytes of which are user-accessible), and integrates a full-featured 1-Wire interface on a single chip.

Each DS2431 has 64-bit ROM address code laser-etched into the chip at the factory to ensure absolute traceability. Data is transmitted serially according to the 1-Wire protocol requiring only a single data line and a return ground line. The DS2431 has an additional storage area called a scratchpad, which acts as a buffer when writing data the main memory or register page. Data is first written to the scratchpad and can be read back from there. After verification, the Copy Scratchpad command transfers the data to the memory cell. Applications of the DS2431 include peripheral/PC board identification, medical sensor calibration data storage, analog sensor calibration, including IEEE-P1451.4 smart sensors, ink cartridge/toner cartridge identification, and after-sales management of consumer products.

The DS2431 uses the 1-Wire protocol and through a single-wire port. When all devices are connected to the bus via a tri-state port or an open-drain port, the control line needs to be connected to pull-up resistor. In this bus system, the microprocessor (master device) relies on each device's unique 64-bit serial number to identify the devices on the and record their addresses. Since each device has a unique serial number, the number of devices that can be connected to the bus is practically unlimited. The 1-Wire protocol, including explanations of commands and "timing", can be found in the 1-Wire System section.

The DS2431 operates without an external power supply. When the bus is high, the DQ pin is connected to a pull-up resistor to the device through the single-wire bus. At the same time, the high bus signal charges an internal capacitor. When the bus is low, this capacitor provides power to the device This method of providing power is called "parasite power".

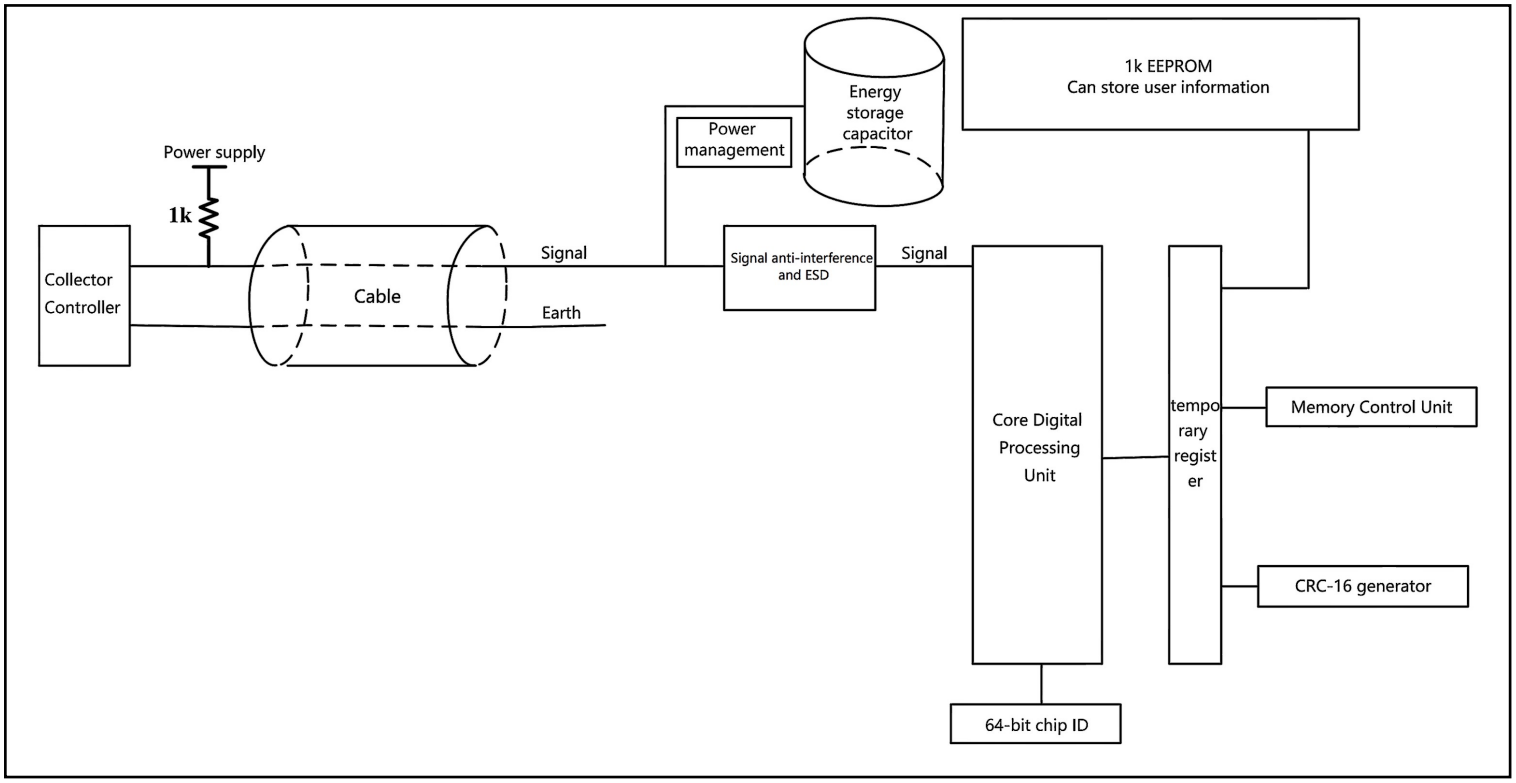


Figure 1.Block diagram of DS2431

The block diagram in Figure 1 illustrates the relationship between the DS2431 main control unit and the memory section. The DS2431 includes four main data components:
(1) a 64-bit mask ROM, (2) a 64-bit scratchpad, (3) four 2-byte EEPROM pages, and (4) a 64-bit register page. The hierarchy of the 1-Wire protocol is shown in Figure 2. master must first send one of the following seven ROM operation commands:
(1) Read ROM, (2) Match ROM, (3) Search ROM, (4) Skip ROM (5) Resume, (6) Overdrive-Skip ROM, and (7) Overdrive-Match ROM. After the Overdrive ROM command is executed at standard speed, the device enters high-speed mode, and all subsequent communications are conducted in high-speed mode. The protocol description related to ROM operation commands is shown in Figure 7. After successfully a ROM operation command, memory operations can be performed, and the master can issue any of the four memory operation commands. The protocol description related to memory operation commands is shown in Figure7. All data is read and written with the least significant bit first.

Power supply

The DS2431 operates in parasitic power mode. Parasitic power mode is very useful in long-distance testing or space-constrained applications. The circuit of the parasitic power is shown in Figure 2. When the bus is high, this control circuit "steals" energy from the bus. Part of the " stolen energy is stored in the parasitic power storage capacitor, and this energy is released to power the device when the bus is low.
In parasitic power mode, the 1-Wire and the storage capacitor can provide sufficient current to the DS2431 to meet the specified and voltage requirements for most operations (see DC and AC Characteristics sections). However, when the DS2431 is performing a data transfer from the register to the EEPROM, operating current can be as high as 0.5mA. This current may cause an unacceptable voltage drop across the weak pull-up resistor connected to the 1-Wire, requires a larger current that the storage capacitor cannot provide at this time. To ensure the DS2431 has an adequate power supply, a strong pull-up must be provided the 1-Wire when performing the copy data to EEPROM operation, implemented by using a MOSFET to directly pull the bus up to the power supply. It must remain in the pull-up state throughout the data copy timing (twr= 9ms). No other actions are allowed while the strong pull-up state is maintained. In addition, the pullup resistor value can also be limited to the specified range.

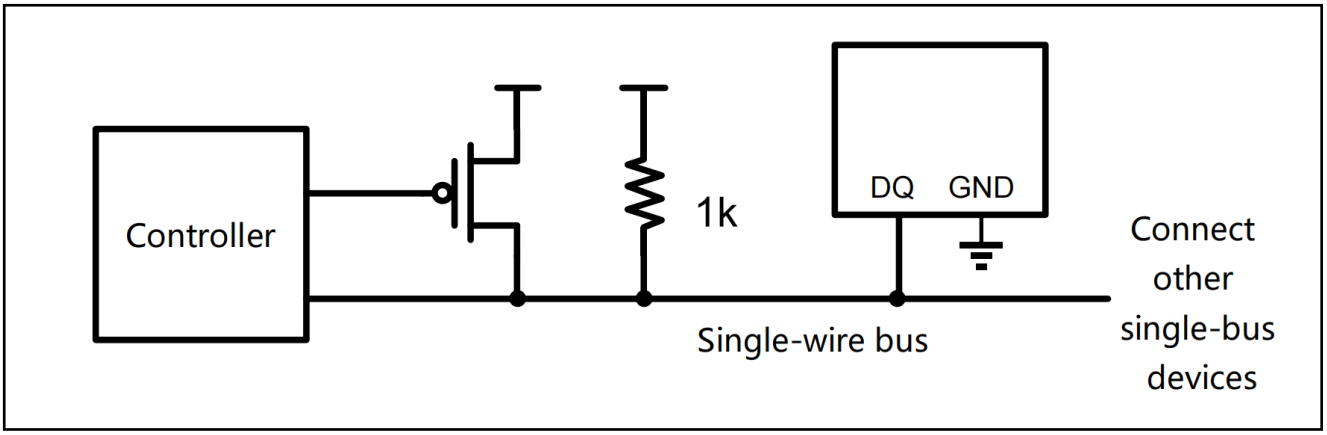


Figure. 2. DS2431 parasitic mode data replication circuit

64-bit ROM

Each DS2431 has a globally unique 64-bit code stored in ROM, as shown in Figure 3. The first 8 are the family code: 2Dh. The next 48 bits are a unique serial number. The last 8 bits are the CRC code for the above 56. For a detailed explanation of the CRC, see the CRC Generator section. The 64-bit ROM and ROM operations allow the DS2431 to act as a1-Wire device and operate according to the 1-Wire protocol detailed in the 1-Wire System section.

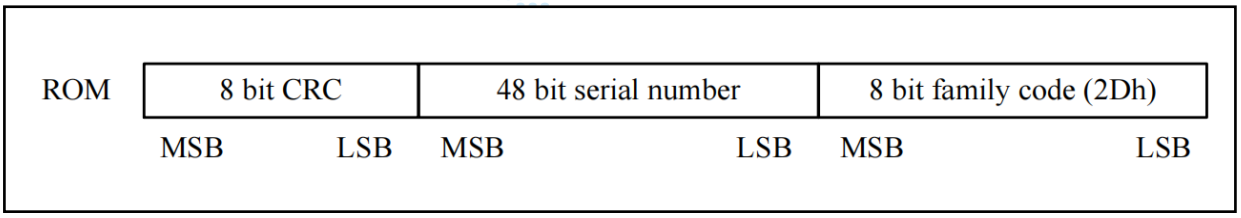


Figure 3. 64-bit ROM code

Memory

Data memory and registers are located in a linear address space, as shown in Table 1. There are no restrictions on read operations for data and registers. The EEPROM array of the DS2431 has a total of 18 rows, with 8 bytes per row. The first 16 rows are divided into 4 memory pages (32 bytes per page), and these 4 pages serve as the main data memory. Each page can be individually set to open (unprotected write-protected, or EPROM mode by setting the corresponding protection bytes in the register row. The last two rows include protection registers and reserved bytes. The register row includes 4 control bytes, 1 copy protection byte, 1 factory preset byte, and two user/manufacturer ID bytes. The manufacturer ID can be a customer-requested identification code used to application software identify products related to the DS2431. To set and register a custom manufacturer ID, please contact the factory. The last row is reserved for future applications./write functions are undefined, and these operations cannot be used.

In addition to the main EEPROM array, it also contains an 8-byte volatile scratchpad. Writing data to the EEPROM array involves two. First, the data is written to the scratchpad, and then it is copied to the main memory array. This allows the user to verify the data before copying it to the memory array. The device only supports full-row (8-byte) copy operations. To ensure the validity of the data in the scratchpad during the copy operation, the address by the Write Scratchpad command must start at a row boundary, and 8 full bytes must be written to the scratchpad.

The protection control register determines how input data is loaded into the scratchpad when executing the Write Scratchpad command. When the protection control register is set 55h (write protection), the input data is ignored, and the main memory data at the target address is loaded into the scratchpad. When the protection control register is to AAh (EPROM mode), the input data is logically ANDed with the main memory data at the target address, and the result is loaded into the scratchpad. Any setting of the protection control register leaves the corresponding memory page in an open state with unrestricted write operations. When the protection control byte is set to 55h or AAh, byte itself is also write-protected. Setting the protection control byte to 55h does not prevent copy operations. This allows write-protected data to be refreshed internally within the (i.e., reprogrammed with the current data).

The copy protection byte, used for a higher security level, should only be used after all other protection control bytes, user bytes, and write-protected pages have set to their final values. If the copy protection byte is set to 55h or AAh, all attempts to copy to the register row and user byte row will be. In addition, all attempts to copy to write-protected main memory pages (i.e., refresh) are also blocked.

Address	Type	Description	Protection Word
0000h to 001Fh	R/(W)	Page0	—
0020h to 003Fh	R/(W)	Page1	—
0040h to 005Fh	R/(W)	Page2	—
0060h to 007Fh	R/(W)	Page3	—
0080h*	R/(W)	Page 0 write protect byte	55h: Write Protect Page 0 AAh: EPROM Mode Page 0 55h or AAh: Write Protect80h
0081h*	R/(W)	Page 1 write protect byte	55h: Write Protect Page 1;AAh: EPROM Mode Page 1;55h or AAh: Write 81h
0082h*	R/(W)	Page 2 write protect byte	55h: Write Protect Page 2;AAh: EPROM Mode Page 2;55h or AAh: Protect 82h
0083h*	R/(W)	Page 3 write protect byte	55h: Write Protect 3;AAh: EPROM Mode Page 3;55h or AAh: Write 83h
0084h*	R/(W)	Copy protection bytes	55h or AAh: Copy Protect 0080h :008Fh,andAny Write-Protected PagesWrite-Protected Pages
0085h	R	Factory byte	AAh: Write Protect 85h, 86h,87h; 55h: Write Protect 8h;Unprotect 86h, 87h
0086h	R/(W)	User byte	—
0087h*	R/(W)	User byte	—
0088h to 008Fh	—	Operation prohibited	—

Table 1. Memory functions

Note: Once programmed to 55 or AA, these addresses become read-only; writing other data will not trigger write protection, nor will it have any.

Address register and transfer status

The DS2431 uses three address registers: TA1, TA2, and E/S (see Figure 4) to access. These registers are common in many other 1-Wire devices, but their usage differs slightly from the DS2431. Registers TA1 and TA2 must be loaded the target memory address for data write or read operations. Register E/S is a read-only transfer status register used to verify the integrity of the input data for the write operation. The E2:E0 bits of ES are loaded with the T2:T0 bits input by the Write Scratchpad command, incrementing by 1 for each byte data input. This is essentially a byte -end offset counter within an 8-byte register. The 5th bit of the E/S register, called PF, is to logic 1 if the register data is invalid due to a power failure or if the data sent by the host fails to fill the entire register as required. For the written register to be valid, the T2:T0 bits must be 0, and the host must send a full 8 bytes of data. Bits 3, 4, 6 have no defined function and always read as 0. The most significant bit of the E/S register, called AA or Authorization, serves as a flag indicating that the data has been copied to the target memory address; writing data to the register will clear this bit.

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Target address TA1	T7	T6	T5	T4	T3	T2	T1	T0
Target address TA2	T15	T14	T13	T12	T11	T10	T9	T8
Communication status E/S	AA	0	PF	0	0	E2	E1	E0

Figure 4. DS2431 Address Register

Write operation with verification

When writing data to the DS2431 memory, the register must be used as an intermediate storage. First, the host sends the Scratchpad command and specifies the target memory address, then sends the data to be written to the register. Note that the Copy Scratchpad command must be executed when an 8- boundary is reached. That is, the lower 3 bits (T2..T0) of the target address must equal 000b. If T2~T is a non-zero value, the copy command will be aborted. Under certain conditions (see Write Scratchpad write register command), the host will receive an inverted CRC16 checksum which is used to verify the command, the address (the actually sent address), and the data located at the end of the Write Scratchpad command sequence. After receiving this CRC checksum the host compares it with its own calculated result to determine whether the communication was successful, and decides whether to continue executing the Copy Scratchpad command. If the host does not receive the16 code, it should send a Read Scratchpad command to verify the integrity of the data. Before echoing the register data, the DS2431 first sends the target TA1 and TA2, as well as the E/S register value.

If the PF flag is set, it indicates that the data was not correctly delivered to the register or a power failure occurred after the last register write. this case, the host does not need to continue reading data; it can restart writing data to the register. Similarly, if the AA flag is set and the PF flag is cleared it indicates that the device failed to acknowledge the write command. If everything is normal, both flags are cleared. At this point, the host can continue reading and verifying each data. After the host completes the data verification, it can send the Copy Scratchpad command. This command must be immediately followed by the data in the three address registers: TA1,2, and E/S. The host should obtain the contents of these registers by reading them.

CRC generator

CRC8

CRC8 is stored in memory as part of the 64-bit ROM of DS2431. The CRC8 code is calculated from the 56 bits of the ROM and is included in the critical byte of the ROM. The CRC is calculated from the data stored in memory, so when the data in memory changes, the value CRC8 also changes accordingly.
CRC8 allows the bus controller to perform data verification when reading the DS2431. To verify whether the data has been read correctly, the controller must calculate a CRC8 value from the received data and compare it with the value stored in the 64-bit ROM of the DS2431 (when reading ROM) or the 8-bit CRC8 value calculated internally by the DS2431 (when reading register 1). If the calculated CRC8 value matches the read8 value, the data has been transmitted without error. The comparison of the CRC8 value and whether to proceed to the next operation is entirely determined by the bus controller. The calculation for CRC8 is as follows:

$$CRC8 = X^8 + X^5 + X^4 + 1$$

The single-bus CRC8 can be generated by a polynomial generator consisting of a shift register and XOR gates, as shown in Figure 5. This circuit a shift register and several XOR gates, with each bit of the shift register initialized to 0. Starting from the least significant bit in the ROM or the 0th byte of register, one bit at a time is shifted into the register. After 56 bits of data from the ROM have been transmitted or the most significant bit of the 7th of the register has been shifted in, the CRC8 value is stored in the shift register. Next, the CRC8 value must be shifted in cyclically. At this point, the calculated CRC8 is correct, the shift register will reset to 0.

CRC16

The CRC16 checksum is used to quickly verify the data transmitted when reading and writing registers. Unlike the 8-bit CRC8 checksum, the 6-bit CRC16 checksum is always transmitted in inverted form. The host determines whether to continue an operation or re-read the data part with an incorrect CRC16 checksum comparing the CRC16 checksum read from the slave with the CRC16 checksum calculated using the received data, Figure 5. The calculation formula for CRC16 is as follows:

$$CRC16 = X^{16} + X^{15} + X^{2} + 1$$

In the Write Scratchpad command, first clear the CRC16 generator, then shift in the command code, target addresses TA1 and TA2, and all bytes sent by the host. The DS2431 only sends the CRC checksum when E2:E0 = 111b.
In the Read Scratchpad command, first clear the CRC16 generator, then shift in the command code, target addresses TA1 and TA2, the/S byte, and the register data sent by the DS2431. The DS2431 only sends the CRC16 checksum when register data is read continuously until end.

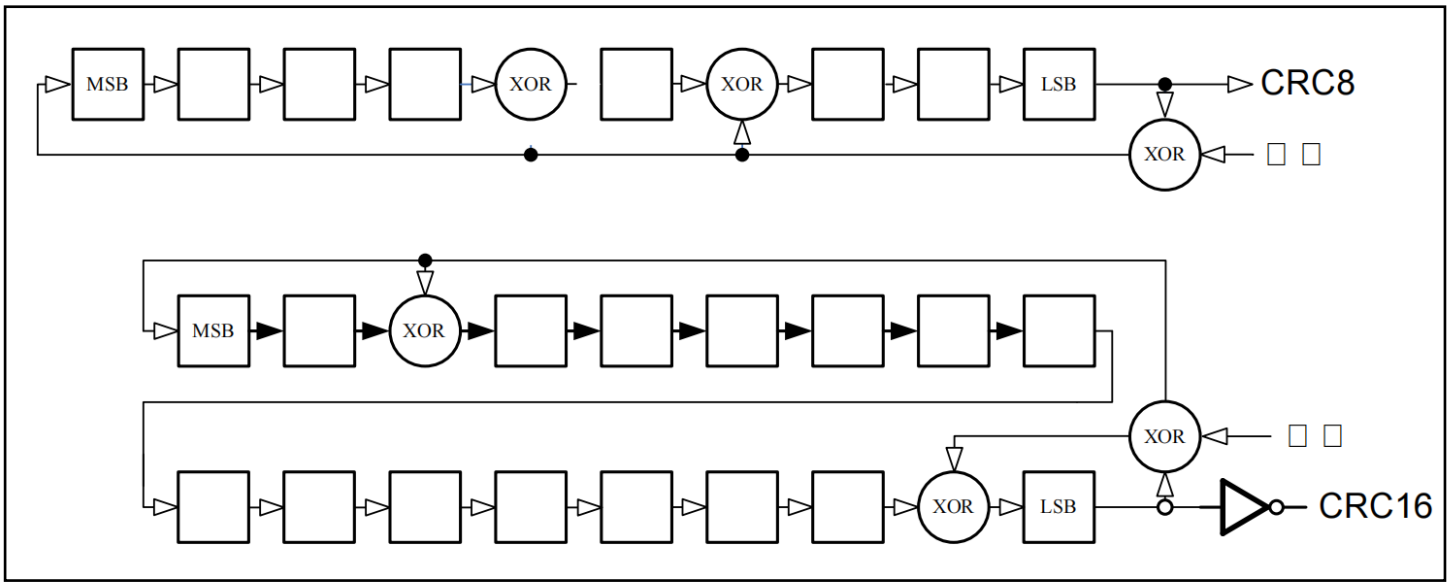


Figure 5. CRC generator

Single bus system

A single-bus system uses a single-bus controller to control one or more slave devices. The DS2431 always acts as a slave. only one slave is connected to the bus, the system is called a " single-point" system; if multiple slaves are connected to the bus, the system is called a "multi-" system.

All data and instructions are transmitted via a single-wire bus starting from the least significant bit. The single-wire bus system is discussed in three aspects: hardware, execution sequence, and single-wire bus signals (signal types and timing). Finally, an example of single-wire bus communication is appended.

Hardware structure

A single-bus system has only one defined signal line, and every device on the bus (master or slave) must be open-drain or tri- output. This mechanism allows every device on the bus that is not transmitting data to release the bus for use by other devices. The single-bus port (DQ pin) of the2431 is open-drain, and its internal equivalent circuit is shown in Figure 6.
The single-wire bus requires an external pull-up resistor of about 1kΩ; the idle state of the single-wire bus is high. a transmission needs to be paused for some reason and you want to resume it later, the bus must remain in the idle state. During the recovery period, if the single-wire is in the inactive (high) state, the recovery time between bits can be infinitely long. If the bus remains at a low level for more than 480us, all on the bus will be reset.

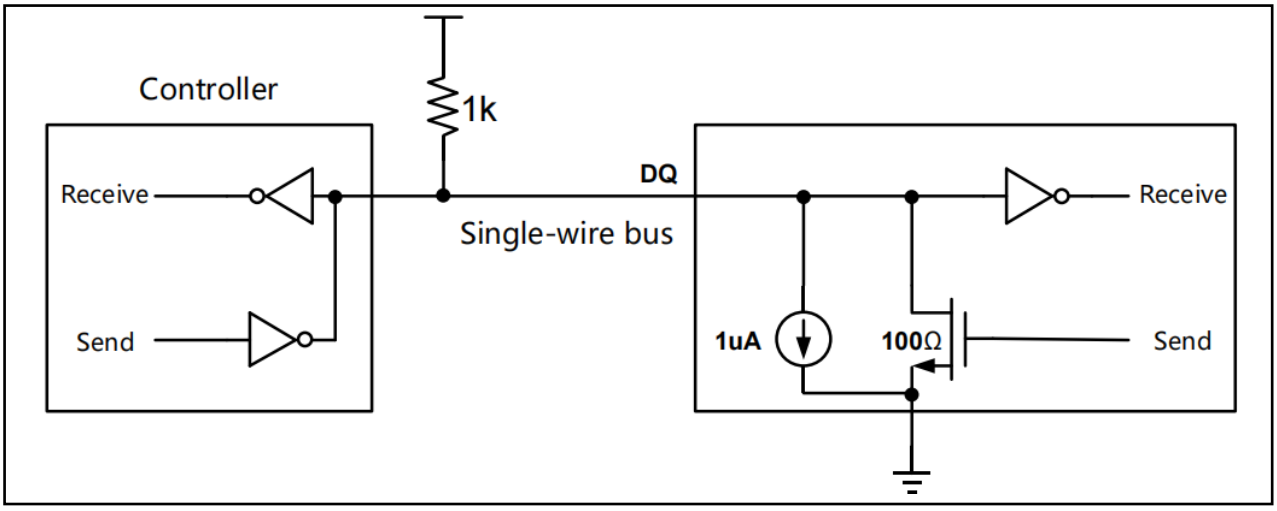


Figure 6. Hardware structure diagram

Execution sequence

The execution sequence for accessing the DS2431 via the 1-Wire bus is as follows:
Step 1: Initialization
Step 2 ROM command
Step 3: Function command
Every operation of the DS2431 must satisfy the above steps; if any step is missing or the sequence is out of, the device will not return a value.

(1) Initialization

All operations performed over the 1-Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse issued the bus controller and a subsequent presence pulse issued by the slave. The presence pulse lets the bus controller know that the DS2431 is on the bus and ready for operation see the Bus Signals section for details.

(2) ROM Commands

Once the bus controller detects a presence pulse, it issues a ROM command, as shown in Table 2. multiple DS2431 devices are connected to the bus, these commands operate based on the unique 64-bit ROM sequence code of each device, allowing the bus controller select the specific device to be operated. These commands can also enable the bus controller to identify how many and what types of devices are connected to the bus. There are 7 commands, all 8 bits in length. The bus controller issues a ROM command before initiating a DS2431 function command. The ROM command operation diagram is shown in Figure7.

ROM command	Send command	Function	Return value
Read ROM	0x33	(Single chip only)	64-bit ROM
Match ROM	0x55		N/A
Search ROM	0xF0	Chips on the search bus	
Continue ROM	0xA5		
Skip ROM	0xCC		N/A
(Accelerate) Skip ROM	0x3C		
(Accelerate) Match ROM	0x69		

Table 2. ROM Command List

Read ROM [33h]

This command can only be used when there is a single DS2431 on the bus. This command the bus controller to read the 64-bit serial number of the slave without using the Search ROM command. If this command is used when there is more than one slave on bus, a data conflict will occur when all slaves attempt to transmit signals simultaneously.

Match ROM [55h]

The MATCH ROM command is followed by a 64bit ROM serial number, which the bus controller uses to locate a specific slave device on a multipoint bus. Only the DS2431 that exactly matches the 64bit ROM serial number can respond to subsequent memory operation commands; all slaves that do not match the 64-bit ROM serial number will wait for the next reset pulse.

Skip ROM [CCh]

This command allows the bus controller to use function commands without providing a 64-bit ROM code.: A function command can only be issued after a Skip ROM command when there is only one slave on the bus. This saves the time required to send the 64-bit code. If there is more than one slave on the bus, issuing a Skip ROM command followed by a read register command will cause a data conflict on the bus because multiple slaves will transmit simultaneously.

Search ROM [F0h]

During system power-up initialization, the bus controller must identify all ROM sequence codes on the bus to determine the number and model of the. The bus controller repeatedly searches for ROM codes using the Search ROM command to identify all slave devices. If there is only one slave on the bus, the Search ROM command can be by a simpler Read ROM command.

Resume [A5h]

To maximize data throughput in a multi-point environment, the system provides a Resume function. This function checks the status the RC bit; if set, a function command can be sent directly afterwards, similar to the Skip ROM command. The RC bit can only be set by successfully executing a Match ROM Search ROM, or Overdrive Match ROM command. Once the RC bit is set, the Resume command can be used to repeatedly access this device. Accessing other devices on the bus clear the RC bit to prevent two or more slaves from responding to the Resume command simultaneously.

Overdrive-Skip ROM [3Ch]

This command is used when there is only one slave on the single bus. The master can functional commands without providing a 64-bit ROM address code, thereby saving time. Unlike the usual Skip ROM command, the Overdrive Skip ROM command sets the DS2431 to high-speed mode (OD = 1). All subsequent communications after this command are in high-speed mode until a reset pulse with a minimum duration of 48μs resets all devices on the bus to the standard rate (OD = 0). If this command is sent on a multipoint bus, all devices on the bus that support highspeed mode are set to high-speed mode. Subsequently, to address a specific high-speed mode device, a high-speed mode reset pulse must be issued, followed by the ROM or Search ROM command. This can accelerate the search process. If there are multiple slaves on the bus that support high-speed mode, and the Overdrive Skip ROM command followed by a Read command, a data conflict will occur because multiple slaves send data simultaneously.

Overdrive-Match ROM [69h]

The Overdrive Match ROM command, followed by a 64-bit ROM sent in highspeed mode, allows the bus master to access a specific DS2431 on a multi-point bus while simultaneously setting it to high-speed mode. Only the DS2431 that correctly matches the 64-bit ROM will respond to subsequent function commands. Slaves that have been successfully set to high-speed mode by a preceding Overdrive or Overdrive Match command will remain in high-speed mode. All slaves supporting high-speed mode will return to the standard rate after the next reset pulse with a minimum duration of480μs. The Overdrive Match ROM command is applicable to situations with a single or multiple devices on the bus.

(3) Function Commands

After the bus controller uses a ROM command to identify the DS2431 it wishes to communicate with, the host can issue a DS2431 function command. These commands allow the bus controller to read and write the DS2431's registers and perform memory operations. The DS2431 function commands are detailed below, summarized in Table 3, and their flow is shown in Figure 8.

FUNCTION command	Send command	Write value	Return value	Other
WRITE SCRATCHPADWrite register	0x0F	See operation examples 1 and 2 for details.		
READ SCRATCHPADRead register	0xAA			
COPY SCRATCHPADWrite register value to EEPROM	0x55			
Read MemoryRead EE	0xF0			

Table 3. List of storage function commands

Note 1: For the DS2431 in parasite power mode, a strong pull-up must be provided to the 1-Wire bus writing data to the EEPROM, and there must be no other activity on the bus during this period.
Note 2: The bus controller can abort data transmission at any time issuing a reset signal.
Note 3: Complete the data write to the register before the reset signal is initiated.

Write Scratchpad [0Fh]

The Write Scratchpad command is applicable to writable addresses in the memory and register pages. To ensure that data in the registers can be correctly copied to the memory array, the user must ensure that the 8 data bytes in the Write Register command start at a valid row boundary. The Scratchpad command accepts invalid addresses and incomplete memory rows, but subsequent Copy Scratchpad commands will be blocked.
After issuing the Write Scratchpad command, the host must first send the -byte target address, followed by the data to be written to the registers. The starting byte offset of the data written to the registers is T2:T0. The E2E0 bits of ES load the starting byte offset, and increment by 1 for each subsequent data byte received. The final result of E2:E0 is the offset of last complete byte written to the registers. Only complete data bytes are accepted.

When the Write Scratchpad command is executed, the internal CRC16 generator of the DS2431 calculates the CRC16 checksum of the entire data stream as the host transmits, starting from the command code and ending at the last data byte. This CRC16 checksum is generated by the CRC16 polynomial. During, the CRC16 generator is first cleared, and then the Write Scratchpad command code (0Fh), the target address (TA1 and TA2), and all data bytes shifted in sequentially. It should be noted that the CRC16 calculation uses the TA1, TA2, and data bytes actually transmitted by the host. The host can terminate the Scratchpad command at any time. However, if the written data reaches the register limit (E2:E0 = 111b), the host can send 16 time slots and receive the CRC16 checksum generated by the DS2431.
If the Write Scratchpad command attempts to write to a write-protected area, the register will load the original data from the memory instead of the data sent the host. Similarly, if the target address page is in EPROM mode, the register will load the result of a bitwise AND operation between the original memory data and the data by the host.

Read Scratchpad [AAh]
The Read Scratchpad command can be used to verify the integrity of the target address and register data. The starts reading data after sending the command code. The first two bytes are the target address, the next byte is the end offset/data status byte (E/S), followed by register data, which may differ from the original data sent by the host. This is particularly important when the target address is located in the register page or in the write-protected orPROM mode page. For detailed information, see the Write Scratchpad command description. The host should first read all data in the register (E2:E0 - T2:0 1 byte), and then it can receive the inverted CRC16, which is generated based on the data sent by the DS2431. If the host to read data after receiving the CRC16 code, all data read will be logic 1.

Copy Scratchpad [55h]
The Copy Scratchpad command is used to copy data from the registers to a writable memory area. issuing the Copy Scratchpad command, the host must provide a 3-byte authorization pattern, which should be obtained through the Read Scratchpad command immediately preceding this command. This -byte pattern data must correctly match the data in the three address registers (TA1, TA2, and E/S, respectively). The copy operation can only begin if the code matches, the target address is valid, the PF flag is not set, the target memory is not write-protected, and the AA (Authorization Allowed) flag is set. 8 bytes of data in the registers are copied to the target memory. The internal data transfer of the device requires a maximum of tPROG, during which the voltage on the-wire bus must be guaranteed to be no lower than 2.8V. After the data copy is completed, a sequence of alternating "0" and "1" signals be sent until the host sends a reset pulse. If the PF flag is set or the target memory is in write-protected mode, the copy operation will not be executed and the AA will not be set.

Read Memory [F0h]

The Read Memory command is typically used to read data from the DS2431. After issuing the command, host needs to provide a 2-byte target address. Following these two bytes, the host begins reading data starting from the target address, and can read continuously up to address 08Fh. If reading continues, the read result will be a logic 1. The internal TA1, TA2, E/S, and register contents of the are not affected by the Read Memory command.

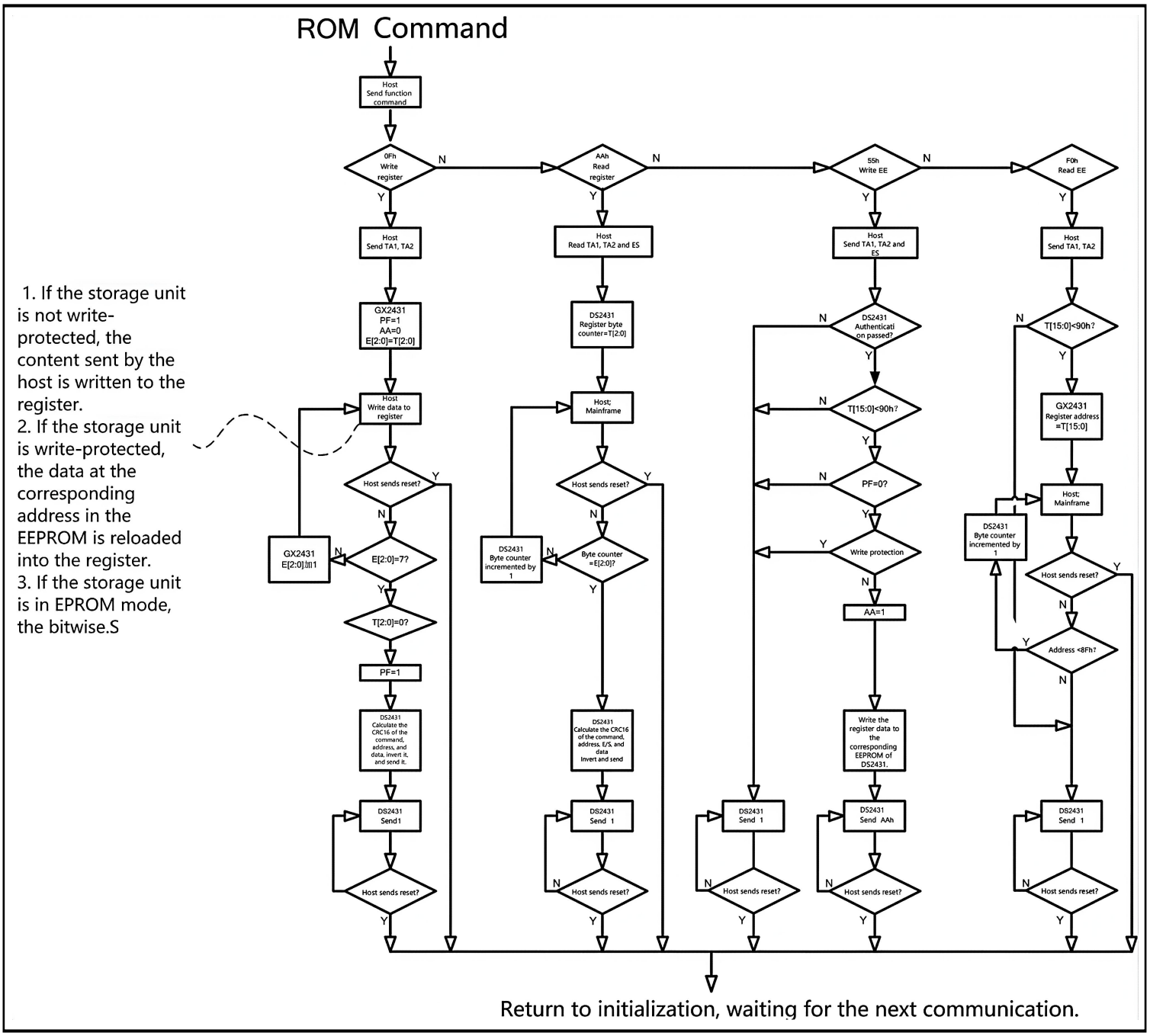


Figure 7. Functional instruction flowchart

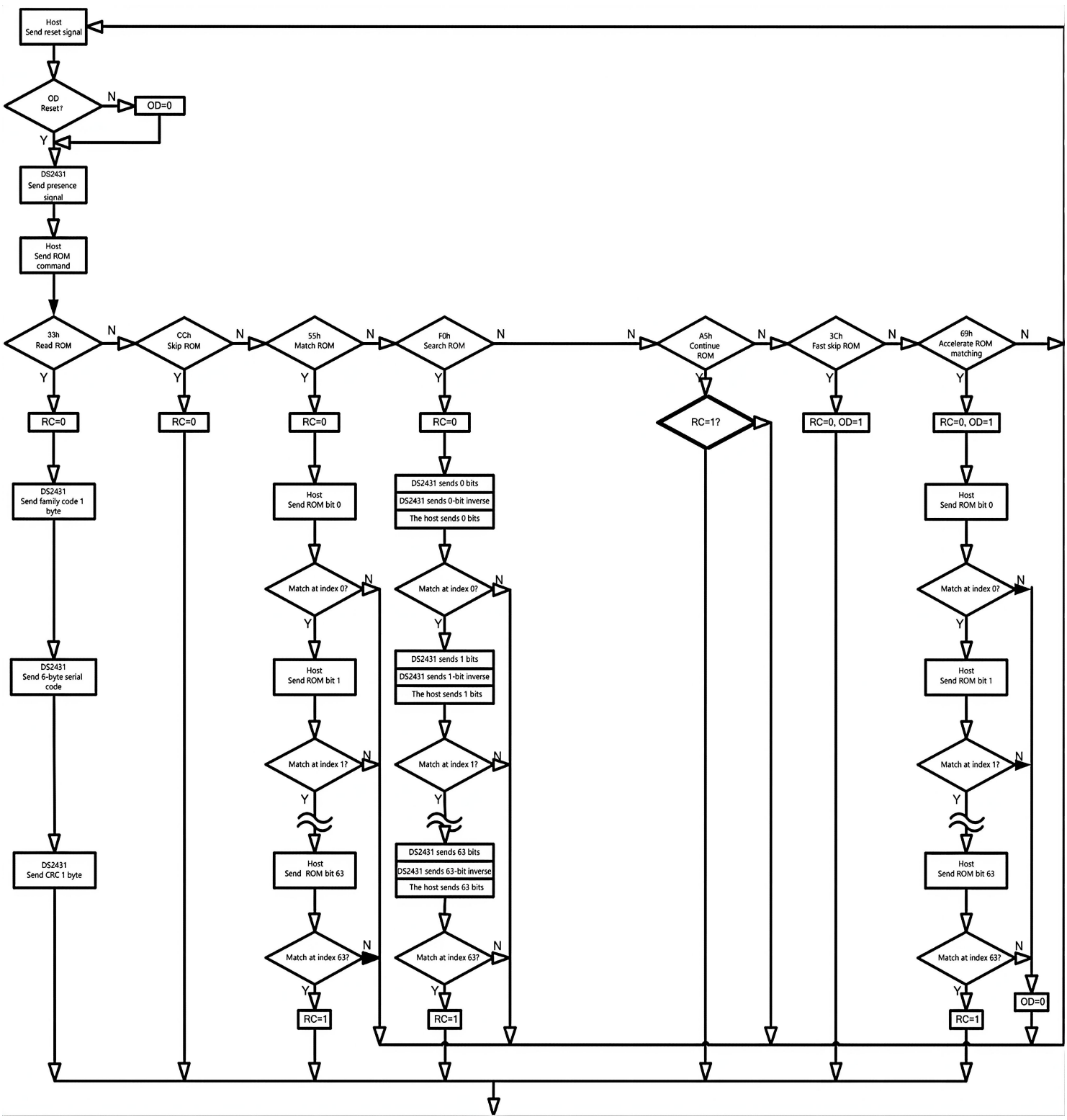


Figure 8. ROM instruction flow

Single bus signal

The DS2431 must adhere to a strict 1-Wire protocol to ensure data integrity. The protocol defines several types of 1-Wire: reset pulse, presence pulse, write 0, write 1, read 0, and read 1. All of these signals, except for the presence pulse, are issued the bus controller.

(1) Reset sequence: reset pulse and presence pulse
All communication with the DS2431 begins with an initialization sequence, as shown in Figure9. A reset pulse followed by a presence pulse indicates that the DS2431 is ready to transmit and receive data.
During the initialization sequence, the bus controller pulls bus low and holds it for 480us to transmit (TX) a reset pulse signal, then releases the bus and enters the receive state (RX). When the bus released, a 1kΩ pull-up resistor pulls the bus to a high level. When the DS2431 detects a rising edge on the IO pin, it for 15-60us, and then transmits a presence pulse consisting of a 60-240us low-level signal

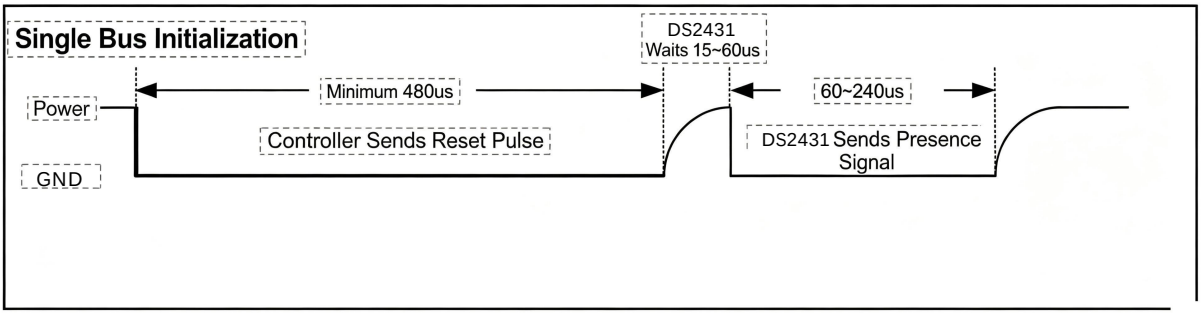


Figure 9. Initialization timing diagram

(2) Read/Write Timing
Data read and write operations of the DS2431 are implemented via timing sequences for information exchange, with one bit of data transmitted per timing cycle.

Write Timing

The DS2431 supports two types of write timing: write 1 timing and write 0 timing. The bus controller transmits a logic 1 using the write 1 timing, and a logic 0 using the write 0 timing. Each write timing must last for a minimum of 60 μs, and a recovery time of at least 5 μs is required between two consecutive write cycles. A write timing starts when the bus controller pulls the data line from logic high level to low level (see Figure 10).
To generate a write 1 timing, the bus controller shall pull the data line low and then release the bus within 15 μs. After the bus is released, the pull-up resistor pulls the bus back to high level.
To generate a write 0 timing, the bus controller shall pull the data line low and keep it in this state for no less than 60 μs.
After the bus controller initiates a write timing, the DS2431 samples the signal line within a time window ranging from 15 μs to 60 μs. A high level on the line is identified as a logic 1, while a low level is identified as a logic 0.

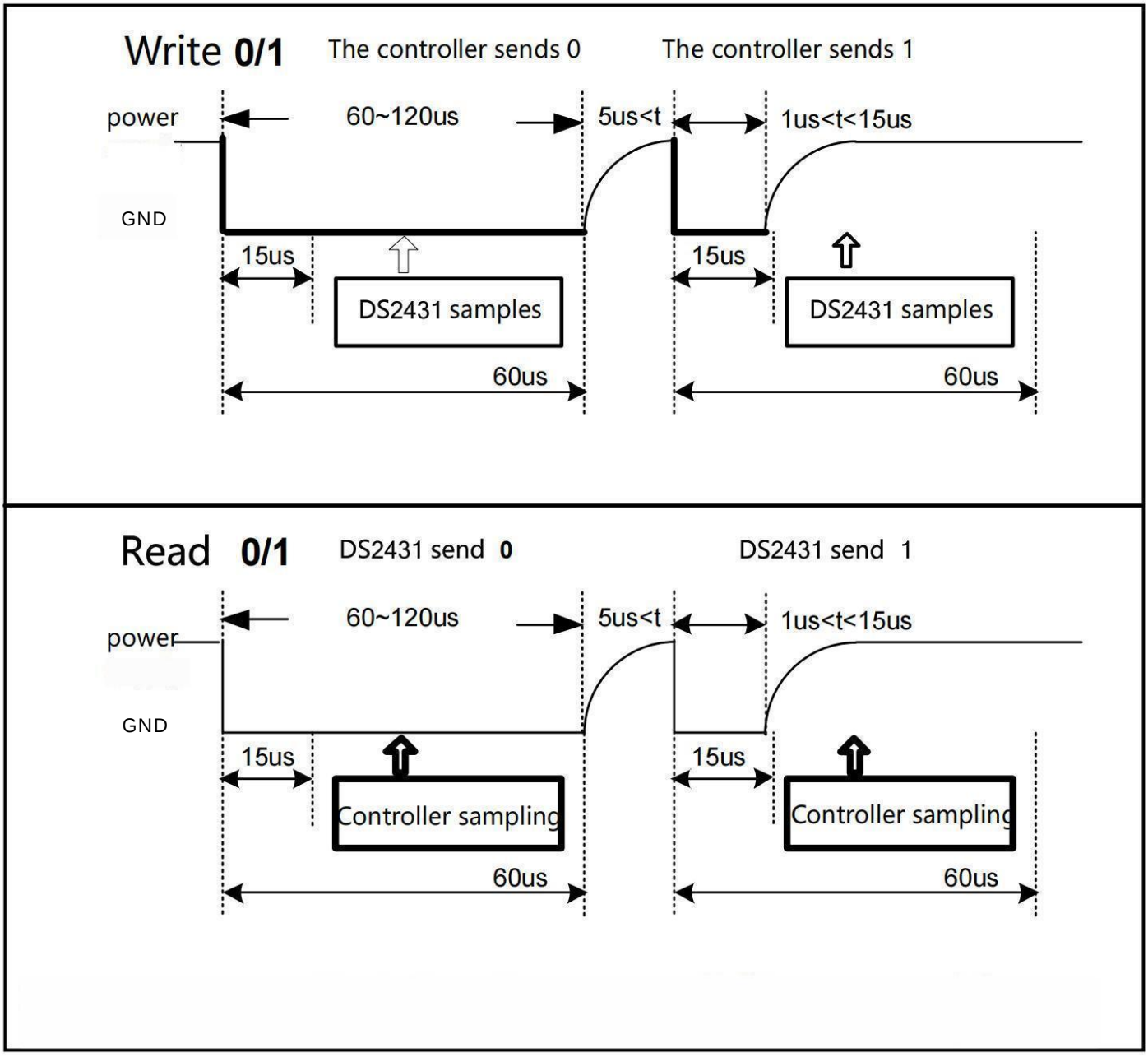


Figure 10. Read/Write Timing

Read Timing

When the bus controller initiates a read timing, the DS2431 is only used to transmit data to the controller., the bus controller must immediately start the read timing after issuing the read register command, so that the DS2431 can provide the requested data.

All read timings must at least 60us, including a recovery time of at least 5us between two read cycles. When the bus controller pulls the data line from a high level to a level, the read timing begins, the data line must be held for at least 1us, and then the bus is released (see Figure 10). After the bus issues the read timing, the DS2431 transmits 1 or 0 by pulling the bus high or low. When the transmission of 0 ends, the bus will released and return to the high-level idle state through a pull-up resistor. The data output by the DS2431 is valid within 15us after the edge of the read timing appears. Therefore, the bus controller releases the bus within 15us after the read timing starts and then samples the bus state to read the state of data line.
Figure 11 indicates that the sum of TINIT, TRC, and TSAMPLE must be less than 15us. Figure 12 indicates the system time can be maximized by the following method: keep the hold time of TINIT and TRC as short as possible, and place the controller sampling time at the end of 15us cycle.

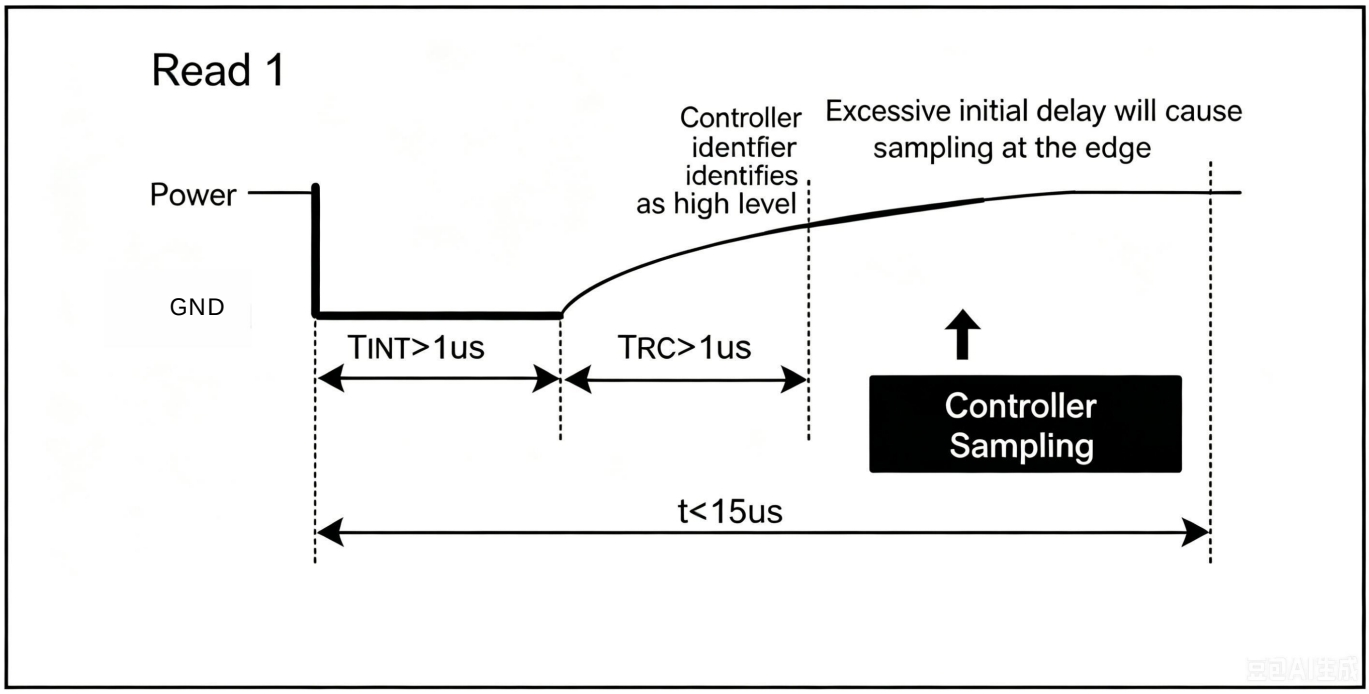


Figure 11. Detailed timing of controller read 1

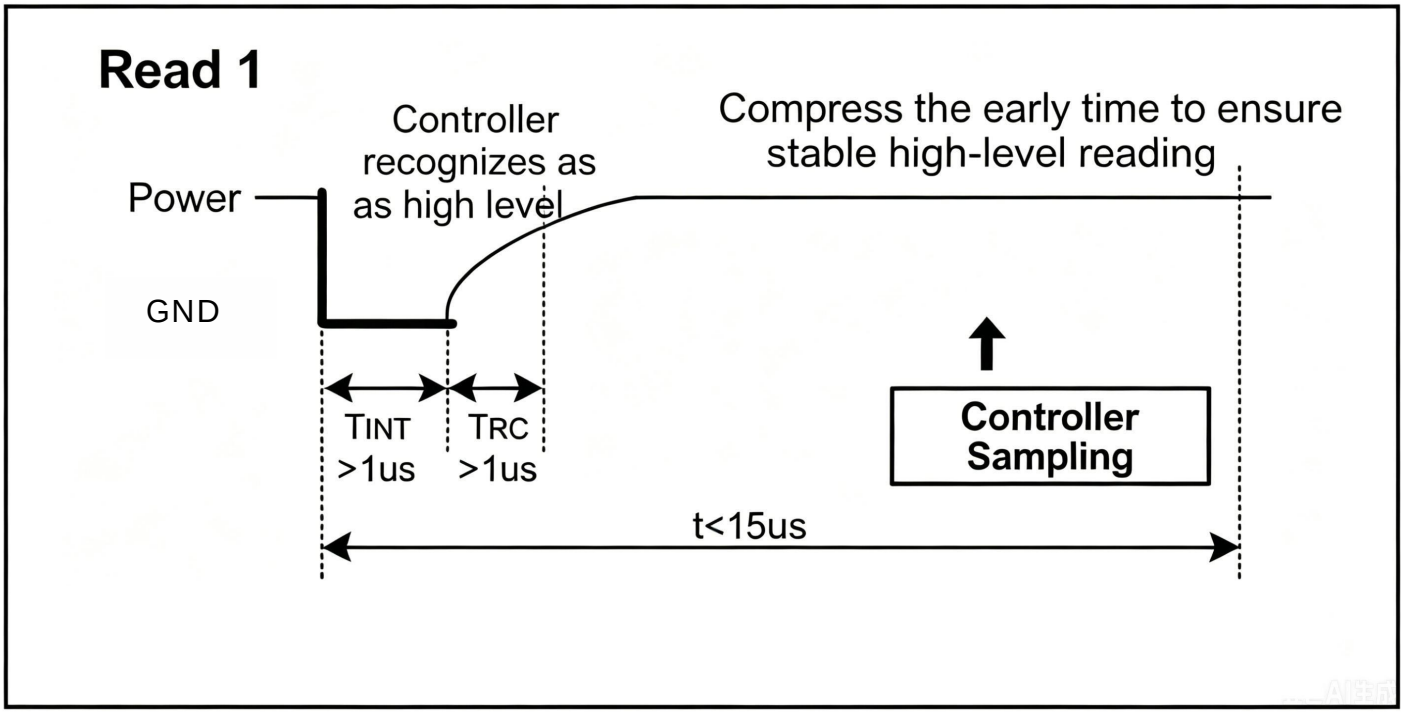


Figure 12. Recommended Controller 1 Timing

Operation Example 1

Write register	Reset	Signal exists	ROM command	Write register	TA	8-TA[2:0] byte data	CRC16 reverse	FF
Read register	Reset	Signal exists	ROM command	Read register	TA-E/S	8-TA[2:0] byte data	CRC16 reverse	FF
Write EE (Success)	Reset	Signal exists	ROM command	Write EE	TA-E/S	programming	AA	
Write EE (Failed)	Reset	Signal exists	ROM command	Write EE	TA-E/S	FF		
Read EE (Success)	Reset	Signal exists	ROM command	Read EE	TA	Data ending with EE	FF	
Read EE (Failed)	Reset	Signal exists	ROM command	Read EE	TA	FF		

Figure 13. Schematic diagram of memory operation

Operation Example 2

Write the first 8 bytes to page 1 of the memory. Read the entire memory. Only a single DS2431 is connected to the host the bus, and the communication process is as follows:

Host Mode	Data (LSB First)	Description
TX	(R eset)	Reset Pulse
RX	(Presence)	Acknowledge Pulse
TX	CCh	Send "Skip ROM" Command
TX	0Fh	Send "Write Scratchpad" Command
TX	20h	TA1, Start Offset = 20h
TX	00h	TA2, Address = 0020h
TX	<8 data bytes>	Write 8 bytes of data to the register
RX	<2 bytes CRC16\>	Read CRC16 code to check data integrity
TX	(R eset)	Reset Pulse
RX	(Presence)	Acknowledge Pulse
TX	CCh	Send "Skip ROM" Command
TX	AAh	Send the "Read Scratchpad" command
RX	20h	Read TA1, start offset=20h
RX	00h	Read TA2, address=0020h
RX	07h	Read E/S, end offset=111b, AA, PF=0
RX	<8 data bytes>	Read register data and verify
RX	<2 bytes CRC16l>	Read CRC 16 code to data integrity
TX	(R eset)	Reset Pulse
RX	(Presence)	Acknowledge Pulse
TX	CCh	Send "Skip ROM" Command
TX	55h	Send the "Copy Scratchpad" command
TX	20h	TA1TA2E/S (Authorization Code)
TX	00h	
TX	07h	

Host Mode	Data (LSB First)	Description
----	<1-Wire idle high>	Wait for tpRoGmax, complete the copy operation
RX	AAh	Read copy status, AAh = success
TX	(R eset)	Reset Pulse
RX	(Presence)	Acknowledge Pulse
TX	CCh	Send "Skip ROM" Command
TX	FOh	Send "Read Memory" command
TX	00h	TA1, start offset=00h
TX	00h	TA2, address=0000h
RX	<144 data bytes>	Read all memory
TX	(R eset)	Reset Pulse
RX	(Presence)	Acknowledge Pulse

Extreme operating conditions

Voltage range of each pin to ground	-0.5V to+6.0V
Operating temperature range	-55℃ to+125℃
Storage range	-55℃ to +150℃
Soldering temperature range	300℃(10S)

The above specifies the environmental conditions required for normal operation of the devices. Long-term operation under extreme conditions may compromise device reliability.

DC characteristics

Test conditions: (-55℃~ 125℃; VDD = 2.5V~5.5V

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit |	Remarks
Supply Voltage	V_{PU}	Parasitic Power	+2.5		+5.5	V	12
Input Low Level	V_{IL}		-0.3		+0.8	V	1,3,4
Input High Level	V_{IH}	Parasitic Power	0.7*VDD		the lower of 5.5 or VDD 0.3	V	16
Sink Current	I_L	VI/O=0.4V	4.0			mA	1
Standby Current	I_{DDS}			0.75	1	uA	67
Dynamic Current	I_{DD}	VDD=5V			0.8	mA	8

NOTE:
(1)All voltages are referenced to ground potential.
(2)The pull-up voltage is obtained as follows: assuming the pull-up device is ideal, the pull-up high level should be equal to VPU. meet the VIH specification of the DS2431, the actual transistor pull-up supply must include the limit of the voltage drop; therefore:VPU_ACTUAL = VPU_IDEAL + VTRANSISTOR。
(3)Logic 0 level is measured at a sink current of 4 mA.
(4)In parasitic power mode under low voltage conditions, to ensure the presence of pulses, VILMAX may need to be reduced to 0.5V
(5)Logic 1 level is measured at a source current of 1 mA.
(6)Standby current is specified at 70 ℃.
(7)To reduce IDDS, the scope of DQ is as follows:GND≦DQ≦GND+0.3V or VDD-0.3V≦DQ ≦VDD.
(8)Dynamic current applies to EEPROM write operations.

AC Characteristics-Non-Volatile Memory

Test conditions: (-55℃~ 125℃; VDD = 2.5V~5.5V)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	Notes
Non-Volatile Write Cycle Time	twR			8	10	ms	
EEPROM Write	NEEWR	25℃	200k			writes	
		85℃	50k			writes	
EEPROM Data Retention	tEEDR	-55℃ to +85℃	40			years	

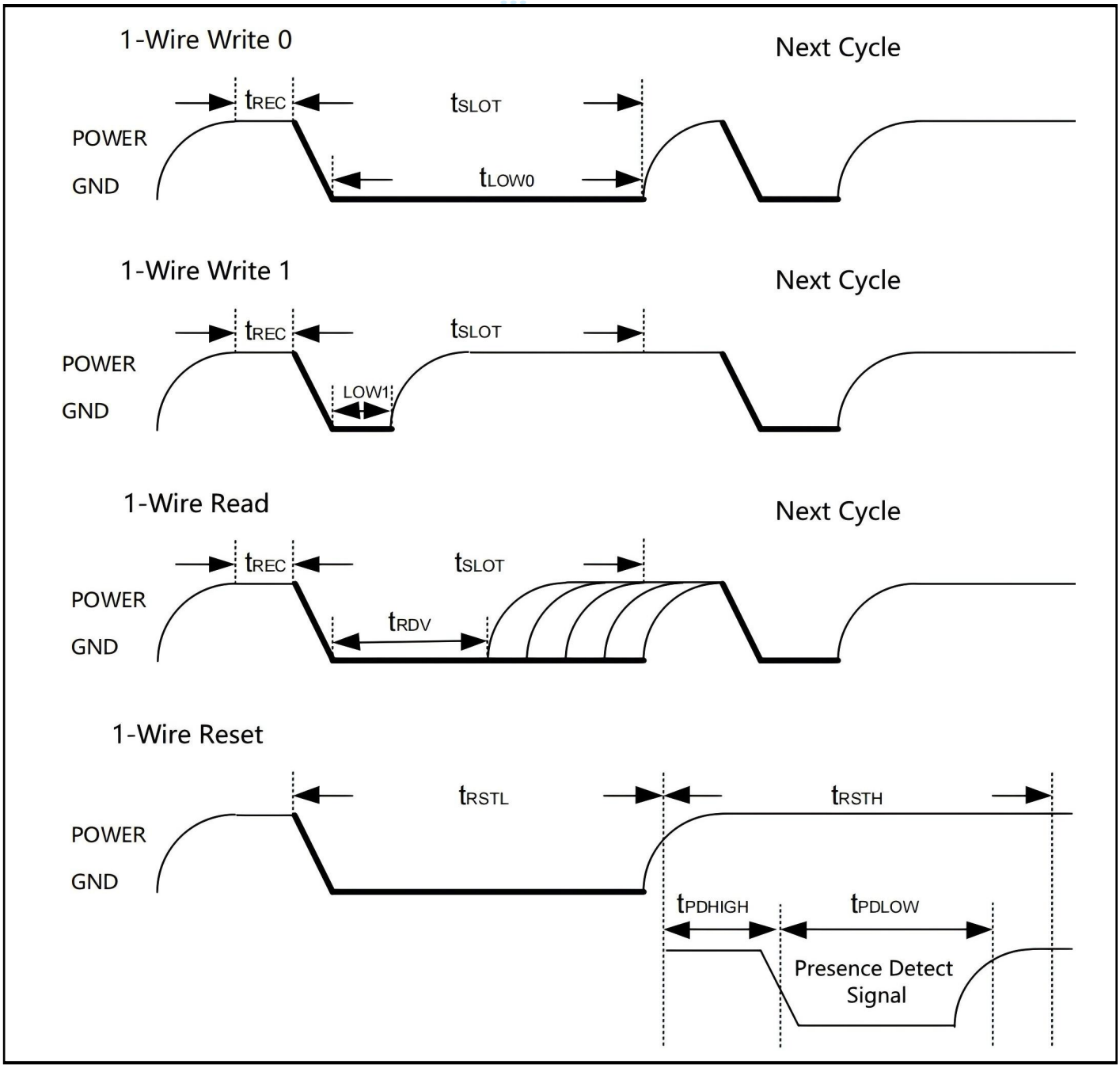
AC Characteristics

Test conditions: (-55℃~ 125℃; VDD = 2.5V~5.5V)

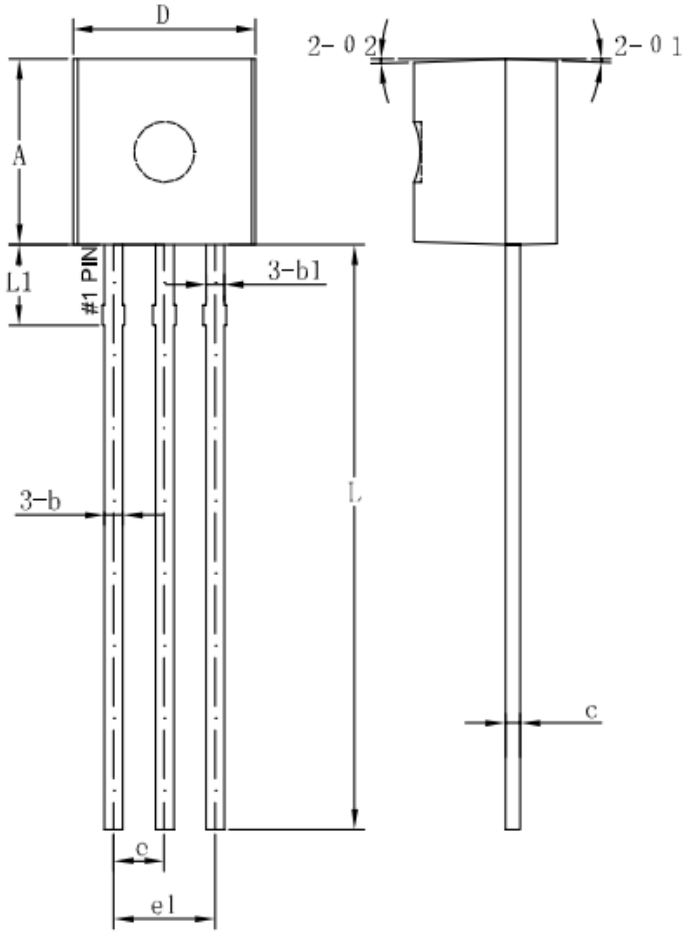
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Time slot	tsLOT		60		120	μs	1
Recovery time	tREC		5			μs	1
Low-level time for writing 0	tLowo		60		120	μs	1
Low-level time for writing 1	tLow1		1		15	μs	1
Data read valid time	tRDV				15	μs	1
High-level reset time	tRSTH		480			μs	1
Low-level reset time	tRSTL		480		640	μs	1
High-level presence detection time	tPDHIGH		15		60	μs	1
Low-level presence detection time	tpDLOW		60		240	μs	1
Capacitance	CIN/OUT				25	pF	

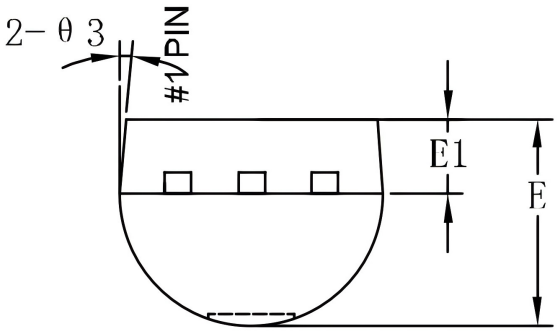
High-speed Mode: (-55℃ ~ +125℃; VDD = 2.5V ~ 5.5V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Time slot	tsLOT		8			μs	1
Recovery time	tREC		5			μs	1
Low-level time for writing 0	tLowo		7		15.5	μs	1
Low-level time for writing 1	tLow1		1		2	μs	1
Data read valid time	tRDV				2	μs	1
High-level reset time	tRSTH		48			μs	1
Low-level reset time	tRSTL		48		80	μs	1
High-level presence detection time	tPDHIGH		2		6	μs	1
Low-level presence detection time	tPDLOW		8		24	μs	1
Capacitance	CINOUT				25	pF	


1-Wire Write 0
Next Cycle
tREC
tSLOT
POWER
GND
tLOW0
1-Wire Write 1
Next Cycle
tREC
tSLOT
POWER
GND
LOW1
1-Wire Read
Next Cycle
tREC
tSLOT
POWER
GND
tRDV
1-Wire Reset
tRSTL
tRSTH
POWER
GND
tPDHIGH
tPDLOW
Presence Detect
Signal

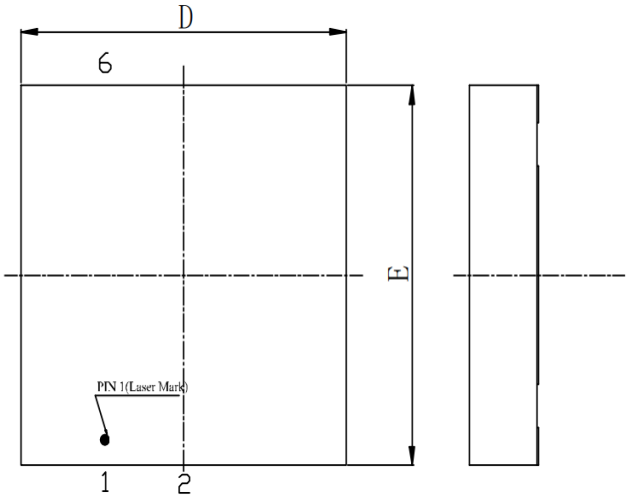
Package TO92

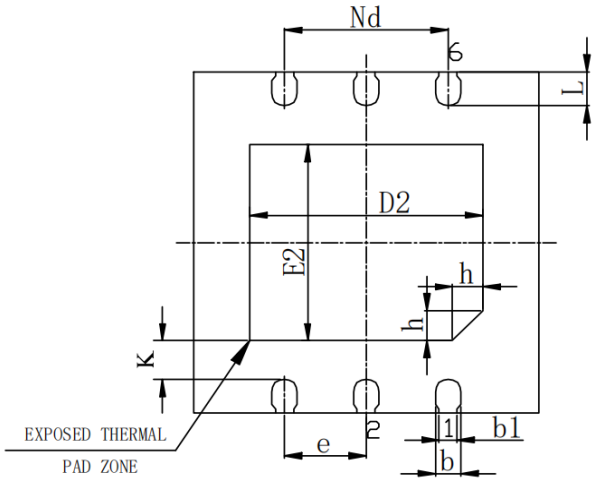


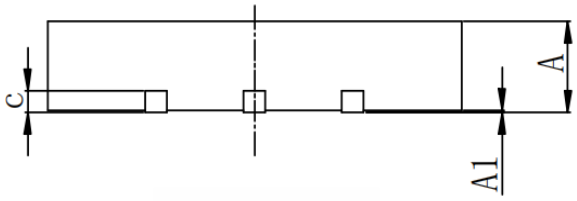


Symbol	Mechanical Dim./mm		
	Min.	Typ.	Max.
A	4.5	4.6	4.7
b	0.38	0.45	0.56
b1		0.45	
C	0.36	0.38	0.51
D	4.5	4.6	4.7
E	3.45	3.6	3.75
E1	1.2	1.3	1.4
e		1.27	
e1		2.54	
L	13.5	14.5	15.3
L1		1.96	
θ1		2°	
θ2		2°	
θ3		5°	

Package DFN6 4.0*4.0*0.75-0.95

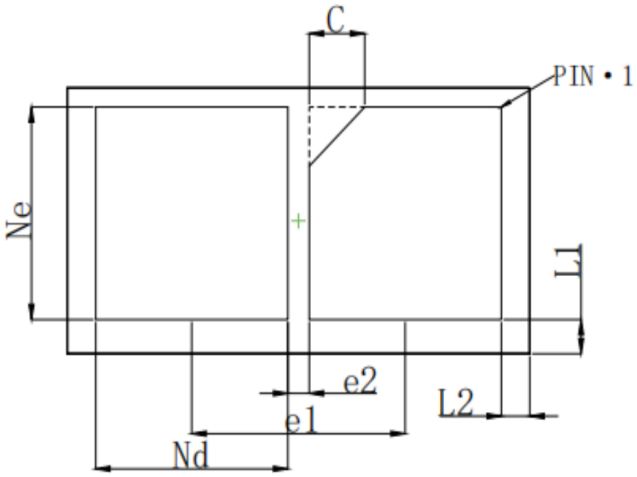


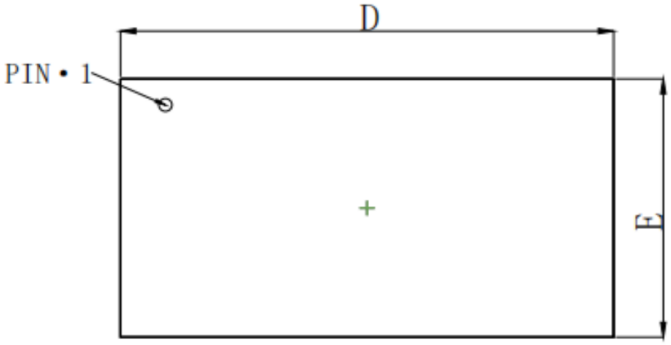


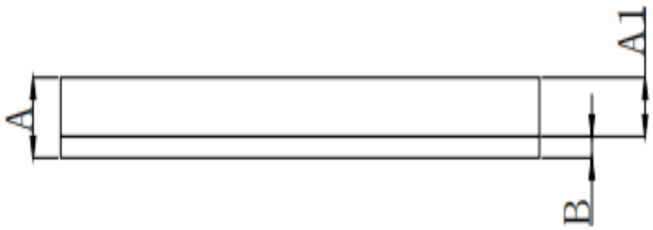


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90
	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.25	0.30	0.35
b1	0.21REF		
c	0.203REF		
D	3.90	4.00	4.10
D2	2.60	2.70	2.80
e	0.95BSC		
Nd	1.90BSC		
E	3.90	4.00	4.10
E2	2.20	2.30	2.40
L	0.35	0.40	0.45
h	0.30	0.35	0.40
K	0.45REF		

Package SFN2 3.5*6.5*0.73

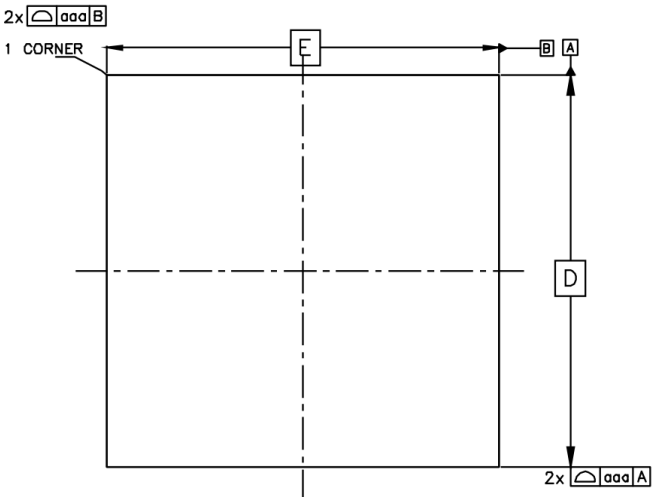


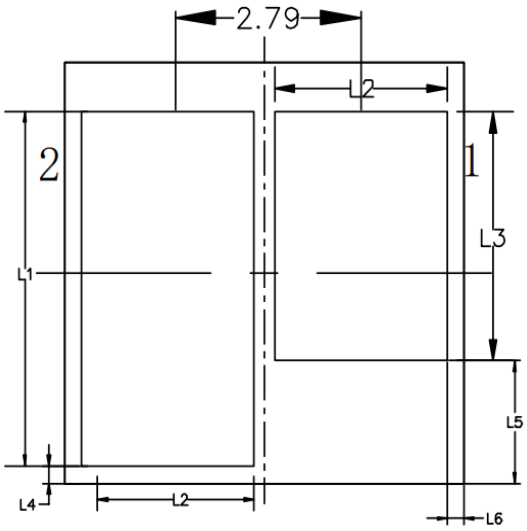


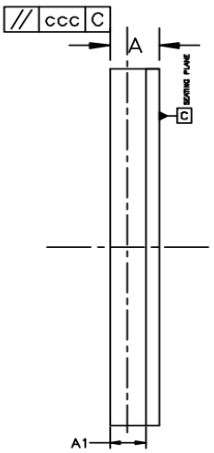


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	6.4	6.5	6.6
E	3.4	3.5	3.6
Ne	2.8 RISIC		
Nd	2.7 BASIC		
el	3.0 BASIC		
e2	0.3 BSI		
A	0.67	0.75	0.83
Al	0.50	0.55	0.60
B	0.17	0.20	0.23
C	0.75	0.78	0.81
L1	0.40	0.45	0.50
L2	0.35	0.40	0.45

Package SFN2 6.0*6.0*0.73







SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.65	0.73	0.81
C	0.16	0.20	0.24
D	5.90	6.00	6.10
E	5.90	6.00	6.10
aaa	0.10		
ccc	0.25		
L1	5.05 REF		
L2	2.600 REF		
L3	3.550 BASIC		
e	0.310 BASIC		
A1	0.48	0.53	0.58
L4	0.250 BASIC		
L5	1.750 BASIC		
L6	0.245 BASIC		

ORDERING INFORMATION

Order Number	Package	Package Quantity	Marking On The park	Temperature
DS2431+-TUDI	TO92	Bag,2000	TD2431	-55℃ to 125℃
DS2431Q-TUDI	DFN6(4*4)	Tape,Reel,2500	TD2431	
DS2431G-TUDI	SFN2(6*6)	Tape,Reel,2500	TD2431G	
DS2431GA-TUDI	SFN2(3.5*6.5)	Tape,Reel,2500	TD2431GA	

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