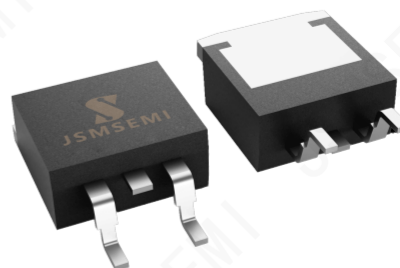


Product Summary

- V_{DS} 150V
- I_D 50A
- $R_{DS(ON)}$ (at $V_{GS}=10V$) $<40m\Omega$
- 100% EAS Tested
- 100% ∇V_{DS} Tested

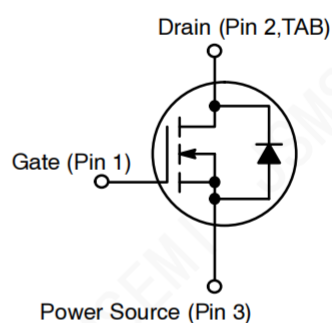


General Description

- Vertical Double-diffused MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Power switching application
- Uninterruptible power supply
- DC-DC convertor
- Motor drivers



Absolute Maximum Ratings $T_C = 25^\circ C$, unless otherwise noted

Parameter	Symbol	Value	Unit
		TO-263	
Drain-Source Voltage	V_{DSS}	150	V
Continuous Drain Current	I_D	50	A
Pulsed Drain Current (note2)	I_{DM}	200	A
Gate-Source Voltage	V_{GSS}	± 20	V
Single Pulse Avalanche Energy (note2)	E_{AS}	1700	mJ
Avalanche Current (note1)	I_{AR}	6.5	V/ns
Repetitive Avalanche Energy (note1)	E_{AR}	368	mJ
Power Dissipation ($T_C = 25^\circ C$)	P_D	300	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ C$

Ordering Information

Order number	Package	Marking	Operation Temperature Range	MSL Grade	Ship, Quantity	Green
IRF3415STRLPBF-JSM	TO-263	F3415S	-55 to 150 $^\circ C$	1	T&R,800	Rohs

Thermal Resistance

Parameter	Symbol	Value	Unit
		TO-263	
Thermal Resistance, Junction-to-Case	R_{thJC}	0.4	°C/W
Thermal Resistance, Junction-to-Ambient	R_{thJA}	55	

Specifications $T_J = 25^{\circ}\text{C}$, unless otherwise noted

Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	150	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 150V, V_{GS} = 0V, T_J = 25^{\circ}C$	--	--	1	μA
Gate-Source Leakage	I_{GSS}	$V_{GS} = +20V, V_{DS}=0V$	--	--	100	nA
		$V_{GS}=-20V, V_{DS}=0V$	--	--	-100	
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	2.0	--	4.0	V
Drain-Source On-Resistance (Note3)	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 20A$	--	30	40	m Ω
Dynamic						
Input Capacitance	C_{iss}	$V_{GS} = 0V,$ $V_{DS} = 25V,$ $f = 1.0MHz$	--	3005	--	pF
Output Capacitance	C_{oss}		--	357	--	
Reverse Transfer Capacitance	C_{rss}		--	35	--	
Total Gate Charge	Q_g	$V_{DD}=150V, I_D = 20A,$ $V_{GS} = 0 \text{ to } 10V$	--	50	--	nC
Gate-Source Charge	Q_{gs}		--	13	--	
Gate-Drain Charge	Q_{gd}		--	18	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD} = 100V, I_D = 20A,$ $V_{GS}= 10V R_G = 10\Omega$	--	36	--	ns
Turn-on Rise Time	t_r		--	39	--	
Turn-off Delay Time	$t_{d(off)}$		--	75	--	
Turn-off Fall Time	t_f		--	22	--	
Drain-Source Body Diode Characteristics						
Continuous Body Diode Current	I_S	$T_C = 25^{\circ}C$	--	--	50	A
Pulsed Diode Forward Current	I_{SM}		--	--	200	
Body Diode Voltage	V_{SD}	$T_J = 25^{\circ}C, I_{SD} = 25A, V_{GS} = 0V$	--	--	1.5	V
Reverse Recovery Time	t_{rr}	$V_{GS} = 0V, I_S = 25A,$ $di_F/dt = 100A/\mu s$	--	208	--	ns
Reverse Recovery Charge	Q_{rr}		--	2.04	--	μC

- Notes**
1. Repetitive Rating: Pulse width limited by maximum junction temperature
 2. $I_{AS} = 30A, V_{DD} = 30V, R_G = 25\Omega$, Starting $T_J = 25^{\circ}\text{C}$
 3. Pulse Test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 1\%$

Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

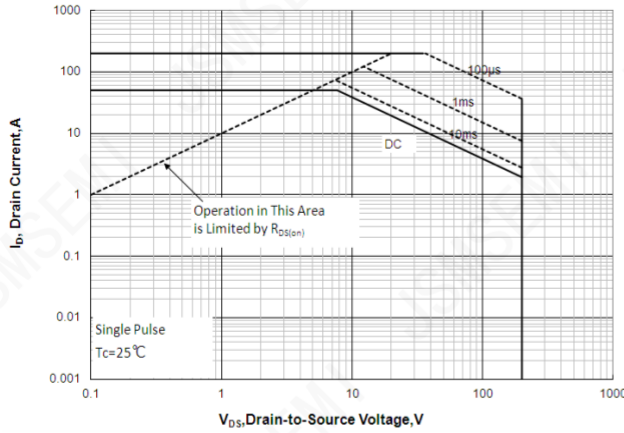


Figure 1 Maximum Forward Bias Safe Operating Area

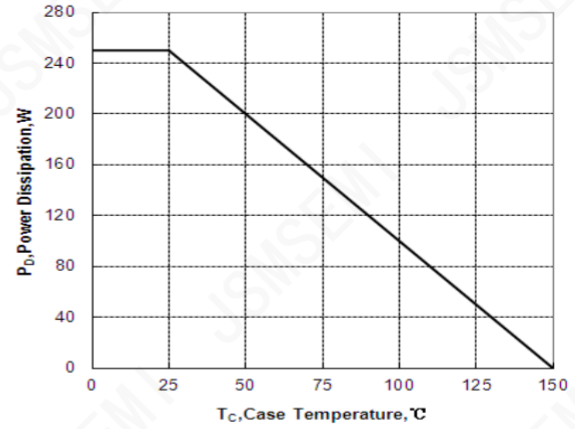


Figure 2 Maximum Power dissipation vs Case Temperature

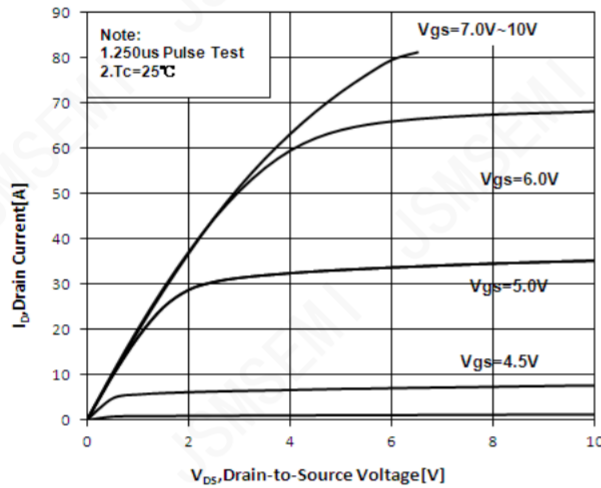


Figure 3 Maximum Continuous Drain Current vs Case Temperature

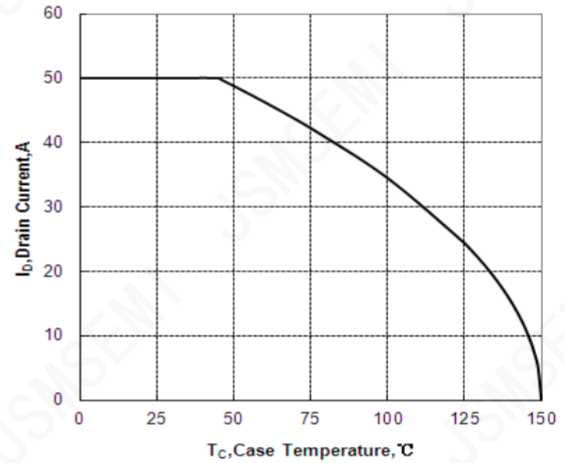


Figure 4 Typical Output Characteristics

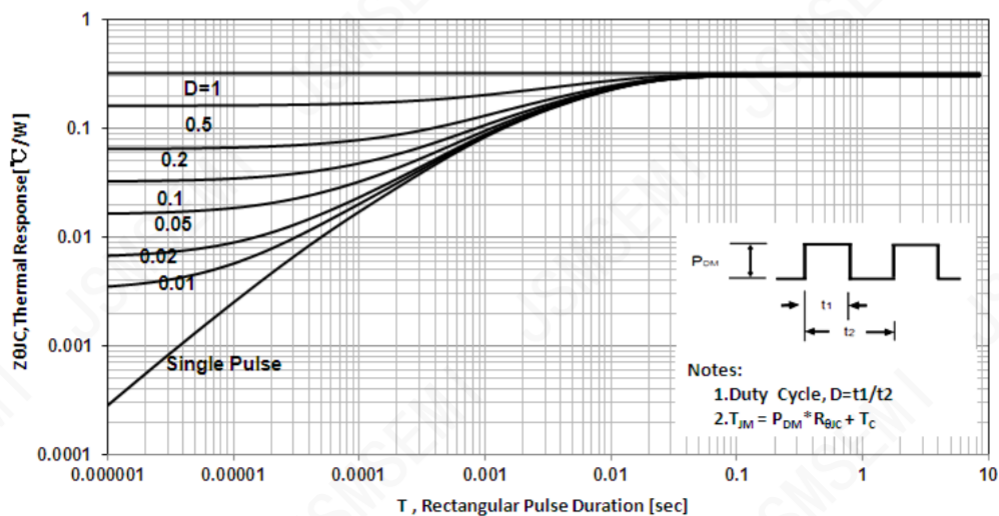


Figure 5 Maximum Effective Thermal Impedance, Junction to Case

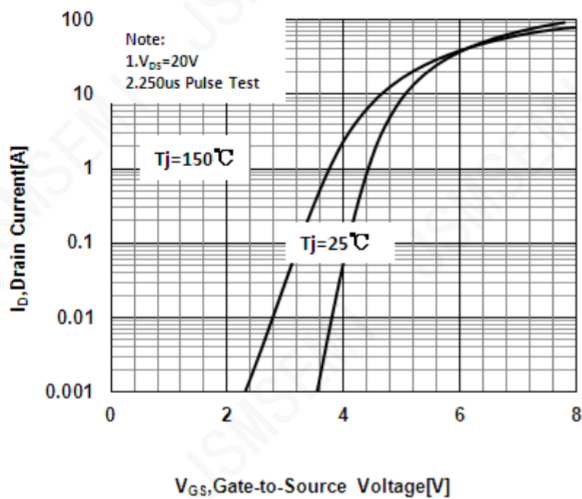


Figure 6 Typical Transfer Characteristics

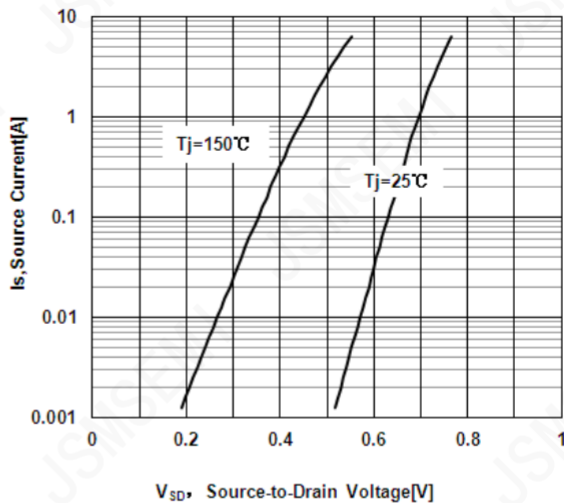


Figure 7 Typical Body Diode Transfer Characteristics

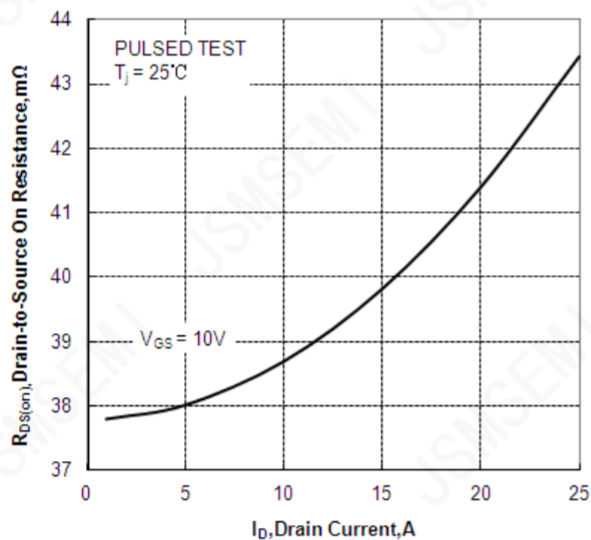


Figure 8 Typical Drain to Source ON Resistance vs Drain Current

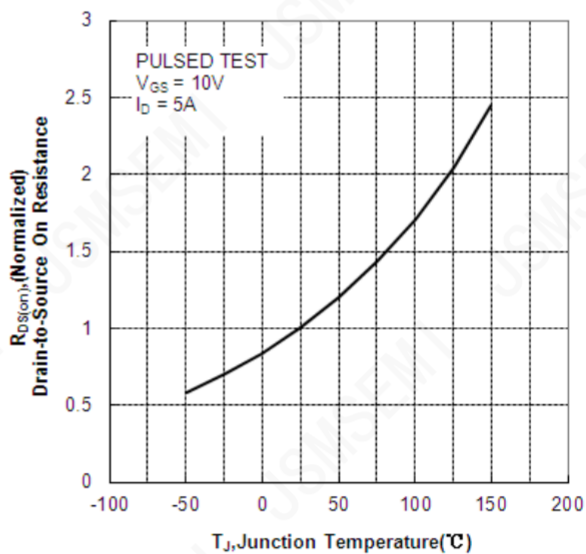


Figure 9 Typical Drain to Source on Resistance vs Junction Temperature

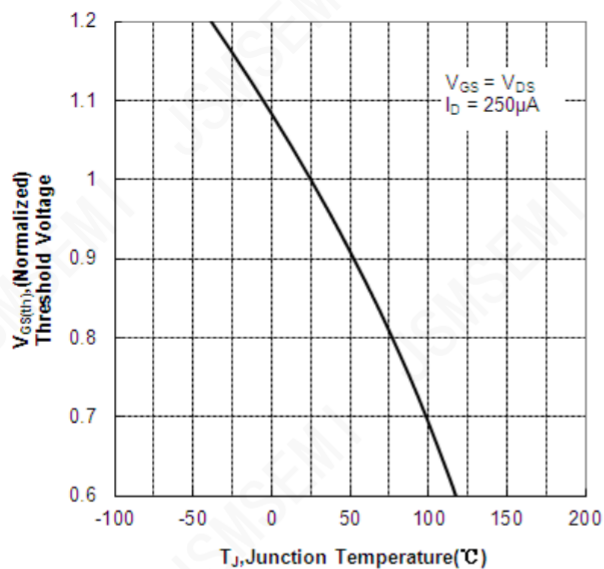


Figure 10 Typical Theshold Voltage vs Junction Temperature

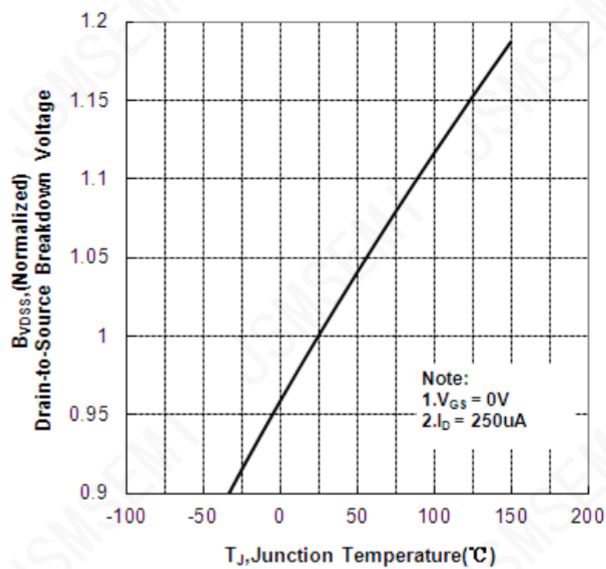


Figure 11 Typical Breakdown Voltage vs Junction Temperature

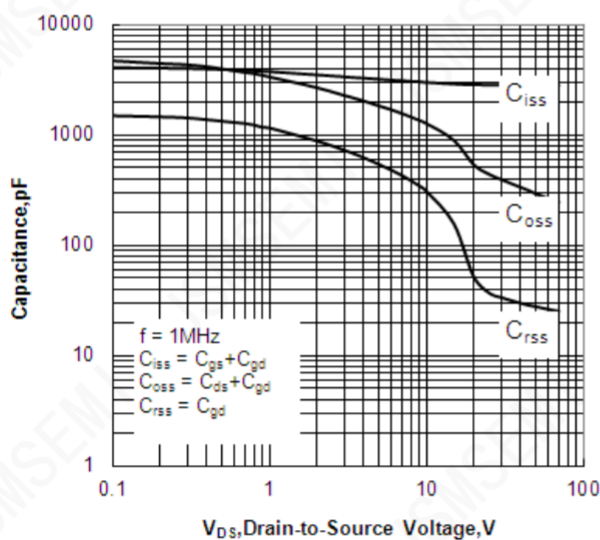


Figure 12 Typical Capacitance vs Drain to Source Voltage

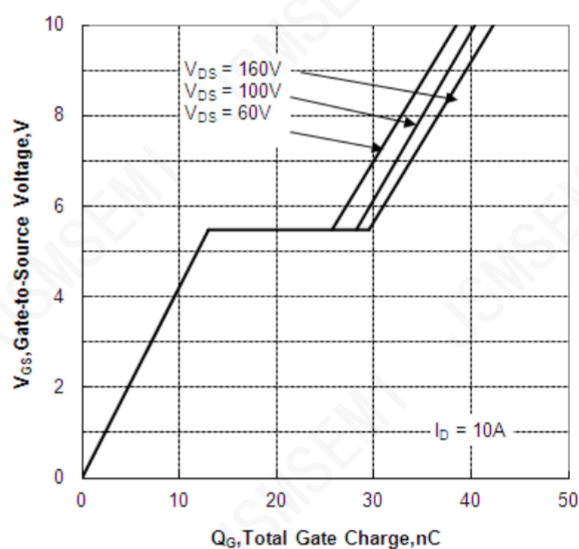


Figure 13 Typical Gate Charge vs Gate to Source Voltage

Figure A: Gate Charge Test Circuit and Waveform

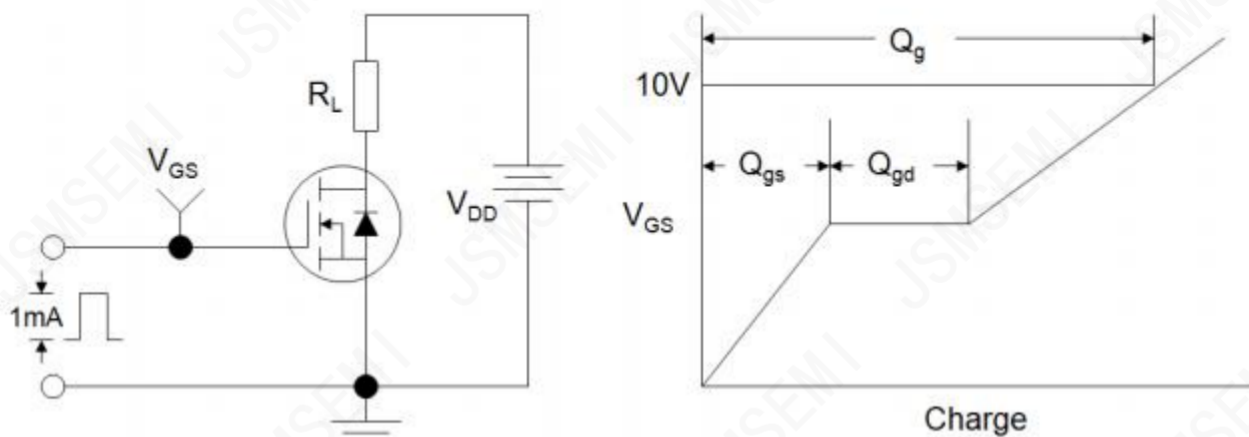


Figure B: Resistive Switching Test Circuit and Waveform

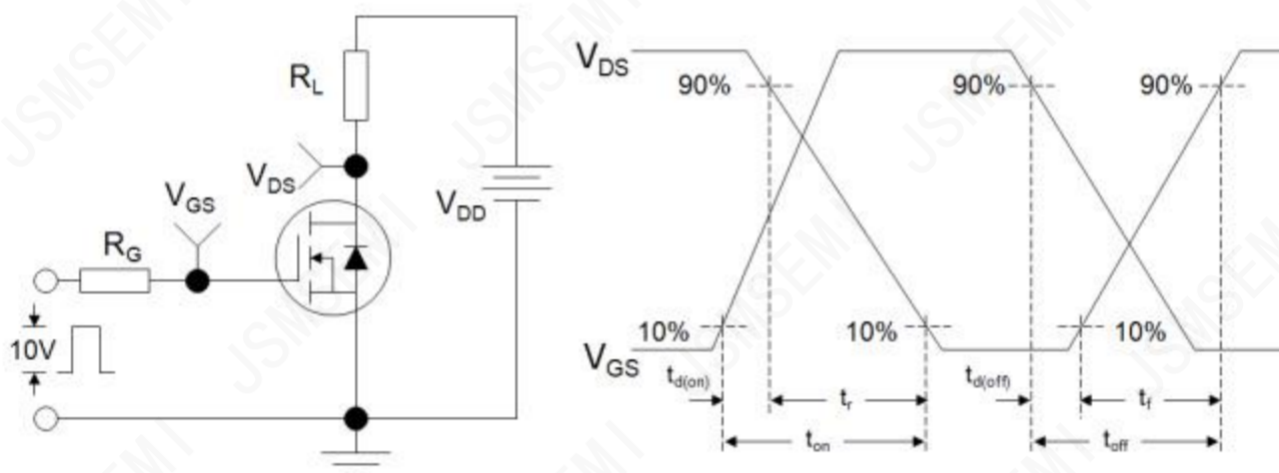
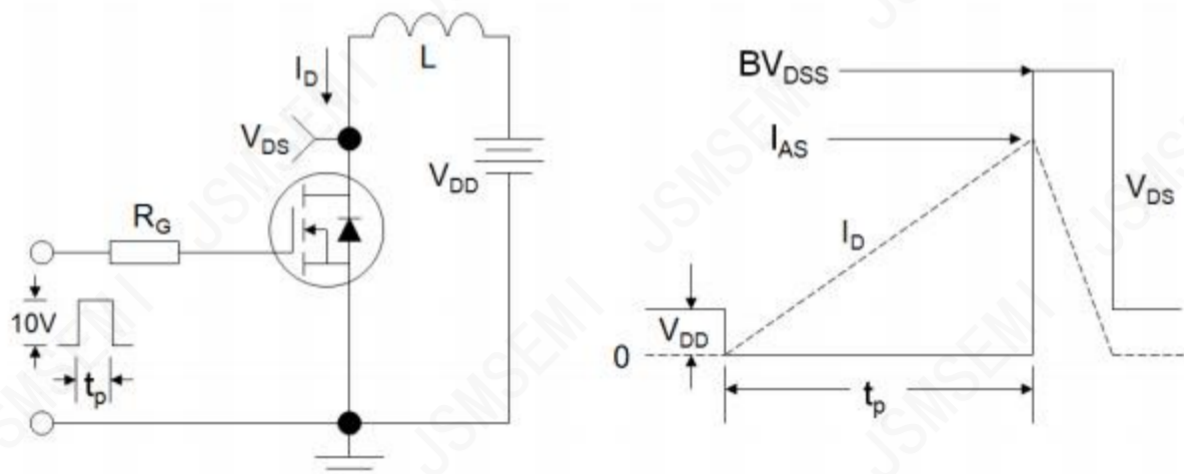
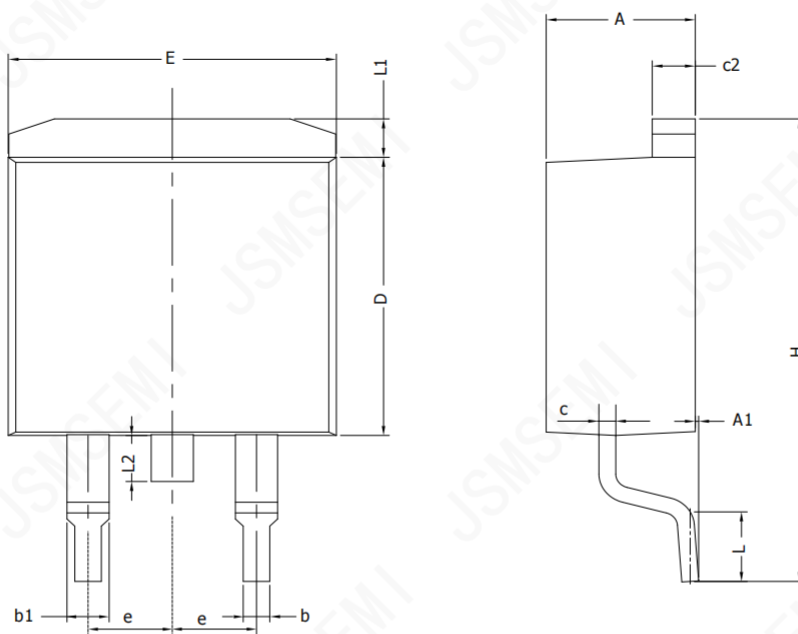


Figure C: Unclamped Inductive Switching Test Circuit and Waveform



Package Information



SYMBOL	MIN	NOM	MAX
A	4.30	4.57	4.72
A1	0	0.10	0.25
b	0.71	0.81	0.91
c	0.30	---	0.60
c2	1.17	1.27	1.37
D	8.50	---	9.35
E	9.80	---	10.45
e	2.54BSC		
H	14.70	---	15.75
L	2.00	2.30	2.74
L1	1.12	1.27	1.42
L2	---	---	1.75

Revision History

Rev.	Change	Date
V1.0	Initial version	6/27/2021

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