Features

- 50 kΩ maximum switch on resistance
- On or off chip clock
- On-chip row pull-up devices
- 2 key roll-over
- Key bounce elimination with single capacitor
- Last key register at outputs
- 3-STATE output LPTTL compatible
- Wide supply range: 3V to 15V
- Low power consumption

DIP-20

SOP-20W

DIP-18

Ordering Information

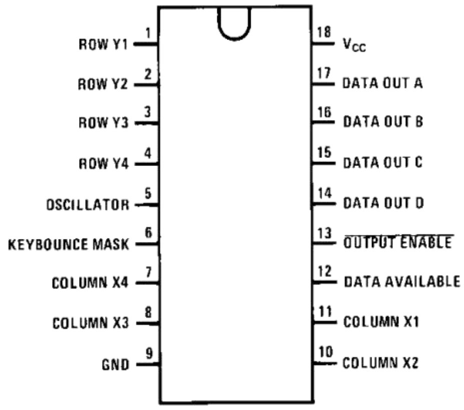
DEVICE	Package Type	MARKING	Packing	Packing Qty
74C922WN	DIP-18	74C922W	TUBE	800pcs/box
74C922WM/TR	SOP-20W	74C922W	REEL	2000pcs/reel
74C922WM	SOP-20W	74C922W	TUBE	35pcs/tube
74C923WN	DIP-20	74C923W	TUBE	720pcs/box
74C923WM/TR	SOP-20W	74C923W	REEL	2000pcs/reel
74C923WM	SOP-20W	74C923W	TUBE	35pcs/tube

General Description

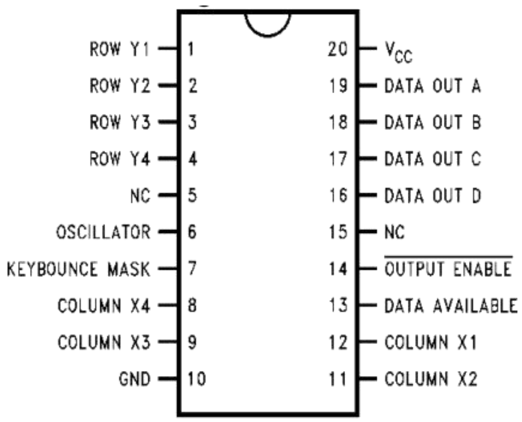
The 74C922 and 74C923 CMOS key encoders provide all the necessary logic to fully encode an array of SPST switches. The keyboard scan can be implemented by either an external clock or external capacitor. These encoders also have on-chip pull-up devices which permit switches with up to 50 kΩ on resistance to be used. No diodes in the switch array are needed to eliminate ghost switches. The internal debounce circuit needs only a single external capacitor and can be defeated by omitting the capacitor. A Data Available output goes to a high level when a valid keyboard entry has been made. The Data Available output returns to a low level when the entered key is released, even if another key is depressed. The Data Available will return high to indicate acceptance of the new key after a normal debounce period; this two-key roll-over is provided between any two switches.

An internal register remembers the last key pressed even after the key is released. The 3-STATE outputs provide for easy expansion and bus operation and are LPTTL compatible.

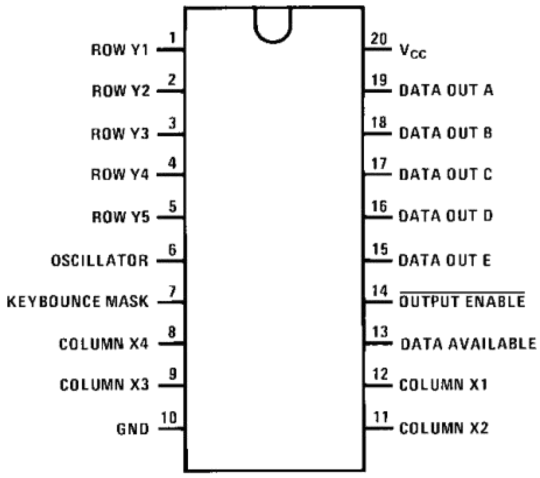
Connection Diagrams



DIP-18 74C922N



SOP-20W 74C922WM



SOP-20W/DIP-20 74C923

Truth Tables

(Pins 0 through 11)

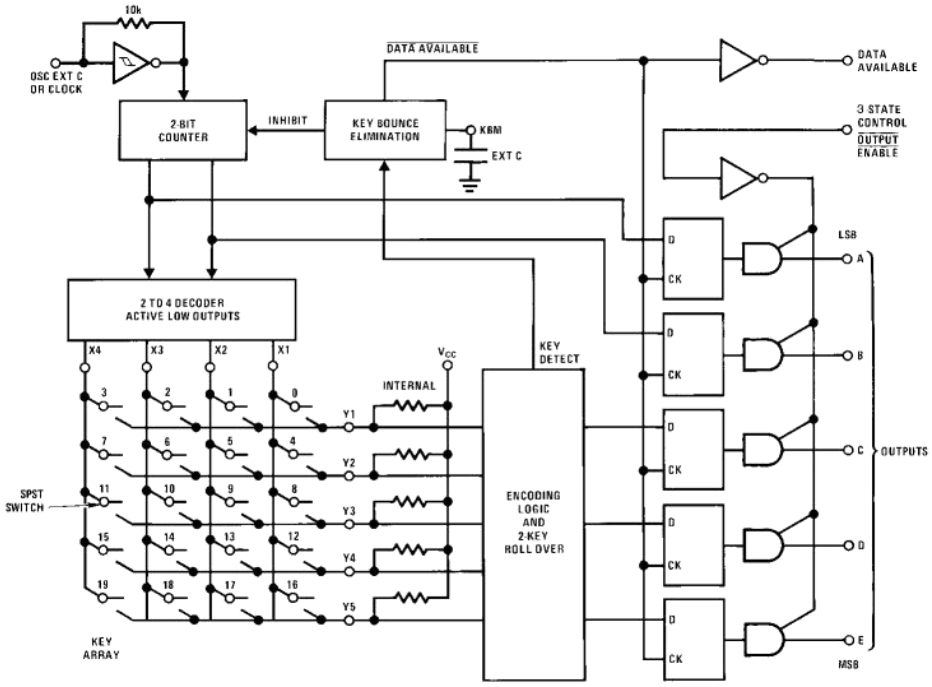
Switch Position		**0 Y1,X1**	**1 Y1,X2**	**2 Y1,X3**	**3 Y1,X4**	**4 Y2,X1**	**5 Y2,X2**	**6 Y2,X3**	**7 Y2,X4**	**8 Y3,X1**	**9 Y3,X2**	**10 Y3,X3**	**11 Y3,X4**
D													
A	**A**	0	1	0	1	0	1	0	1	0	1	0	1
T	**B**	0	0	1	1	0	0	1	1	0	0	1	1
A	**C**	0	0	0	0	1	1	1	1	0	0	0	0
O	**D**	0	0	0	0	0	0	0	0	1	1	1	1
U	**E (Note 1)**	0	0	0	0	0	0	0	0	0	0	0	0
T													

(Pins 12 through 19)

Switch Position		**12 Y4,X1**	**13 Y4,X2**	**14 Y4,X3**	**15 Y4,X4**	**16 Y5(Note1),X1**	**17 Y5(Note1),X2**	**18 Y5(Note1),X3**	**19 Y5(Note1),X4**
D									
A	**A**	0	1	0	1	0	1	0	1
T	**B**	0	0	1	1	0	0	1	1
A	**C**	1	1	1	1	0	0	0	0
O	**D**	1	1	1	1	0	0	0	0
U	**E (Note 1)**	0	0	0	0	1	1	1	1
T									

Note 1: Omit for 74C922

Block Diagram



Absolute Maximum Ratings

Characteristic		Symbol	Value	Unit
Voltage at Any Pin		VCC	0.3	V
Operating free-air temperature		T_A	-40 to 85	℃
Storage Temperature Range		T_{STG}	-65 to 150	℃
Power Dissipation (P D)	Dual-In-Line	P_D	700	mW
	Small Outline	P_D	500	mW
Operating VCC Range		V_{CC}	3 to 15	V
Lead Temperature(Soldering, 10 seconds)		T_L	260	℃

Note 2: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Dc Electrical Characteristics

Min/Max limits apply across temperature range unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
V_T	Positive-Going Threshold Voltage at Osc and KBM Inputs	V_{CC} = 5V, $I_{IN} \geq$ 0.7 mA V_{CC} = 10V, $I_{IN} \geq$ 1.4 mA V_{CC} = 15V, $I_{IN} \geq$ 2.1 mA	3.0 6.0 9.0	3.6 6.8 10	4.3 8.6 12.9	V
V_T	Negative-Going Threshold Voltage at Osc and KBM Inputs	V_{CC} = 5V, $I_{IN} \geq$ 0.7 mA V_{CC} = 10V, $I_{IN} \geq$ 1.4 mA V_{CC} = 15V, $I_{IN} \geq$ 2.1 mA	0.7 1.4 2.1	1.4 3.2 5	2.0 4.0 6.0	V
$V_{IN(1)}$	Logical "1" Input Voltage, Except Osc and KBM Inputs	V_{CC} = 5V V_{CC} = 10V V_{CC} = 15V	3.5 8.0 12.5	4.5 9 13.5		V
$V_{IN(0)}$	Logical "0" Input Voltage, Except Osc and KBM Inputs	V_{CC} = 5V V_{CC} = 10V V_{CC} = 15V		0.5 1 1.5	1.5 2 2.5	V
I_{rp}	Row Pull-Up Current at Y1, Y2, Y3, Y4 and Y5 Inputs	V_{CC} = 5V, V_{IN} = 0.1 V_{CC} V_{CC} = 10V V_{CC} = 15V		-2 -10 -22	-5 -20 -45	μA
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 5V, I_O =- 10μA V_{CC} = 10V, I_O =- 10μA V_{CC} = 15V, I_O =- 10μA	4.5 9 13.5			V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5V, I_O = 10μA V_{CC} = 10V, I_O = 10μA V_{CC} = 15V, I_O = 10μA			0.5 1 1.5	V
R_{on}	Column "ON" Resistance at X1, X2, X3 and X4 Outputs	V_{CC} = 5V, V_O = 0.5V V_{CC} = 10V, V_O = 1V V_{CC} = 15V, V_O = 1.5V		500 300 200	1400 700 500	
I_{CC}	Supply Current Osc at 0V, (one Y low)	V_{CC} = 5V V_{CC} = 10V V_{CC} = 15V		0.55 1.1 1.7	1.1 1.9 2.6	mA
$I_{IN(1)}$	Logical "1" Input Current at Output Enable	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current at Output Enable	V_{CC} = 15V, V_{IN} = 0V	1.0	0.005		μA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Except Osc and KBM Inputs	V_{CC} = 4.75V	V_{CC}-1.5			V
$V_{IN(0)}$	Except Osc and KBM Inputs	V_{CC} = 4.75V			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	I_O = 360μA V_{CC} = 4.75V I_O = 360μA	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	I_O = 360 μA V_{CC} = 4.75V I_O = 360μA			0.4	V

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OUTPUT DRIVE (See Family Characteristics Data Sheet) (Short Circuit Current)						
I_{SOURCE}	Output Source Current (P-Channel)	V_{CC} = 5V, V_{OUT} = 0V, T_A = 25℃	-1.75	-3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V, T_A = 25℃	-8	-15		mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 5V, V_{OUT} = V_{CC}, T_A = 25℃	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC}, T_A = 25℃	8	16		mA

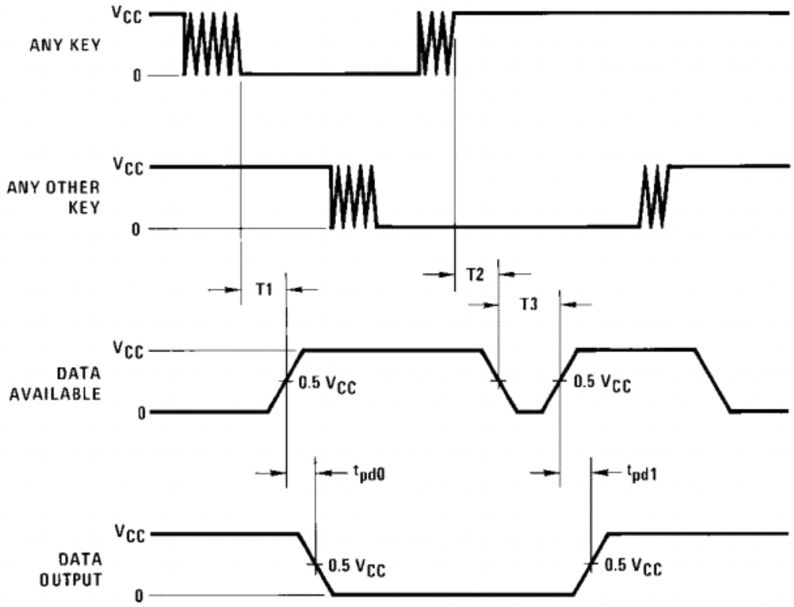
AC Electrical Characteristics(Note 3)
T_A = 25℃, C_L= 50 pF, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}, t_{pd1}	Propagation Delay Time to Logical "0" or Logical "1" from D.A.	CL = 50 pF (Figure 1) VCC = 5V VCC = 10V VCC = 15V		60 35 25	150 80 60	ns
t_{0H}, t_{1H}	Propagation Delay Time from Logical "0" or Logical "1" into High Impedance State	RL = 10k, CL = 10pF (Figure 2) VCC = 5V, RL = 10k VCC = 10V, CL = 10 pF65150ns VCC = 15V		80 50	200 110	ns
t_{H0}, t_{H1}	Propagation Delay Time fromHigh Impedance State to a Logical "0" or Logical "1"	RL = 10k, CL = 50 pF (Figure 2) VCC = 5V, RL = 10k VCC = 10V, CL = 50 pF VCC = 15V		100 55 40	250 125 90	ns
C_{IN}	Input Capacitance	Any Input (Note 4)		5	7.5	pF
C_{OUT}	3-STATE Output Capacitance	Any Output (Note 4)		10		pF

Note 3: AC Parameters are guaranteed by DC correlated testing.

Note 4: Capacitance is guaranteed by periodic testing.

Switching Time Waveforms



T1 ≈ T2 ≈ RC, T3 ≈ 0.7 RC, where R ≈ 10k and C is external capacitor at KBM input.

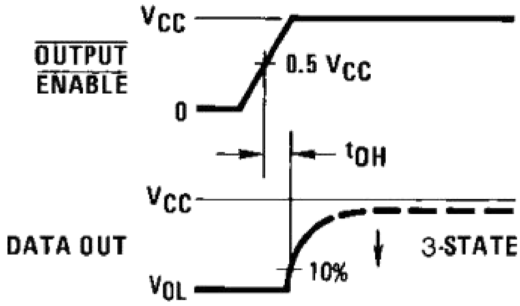


FIGURE 1.

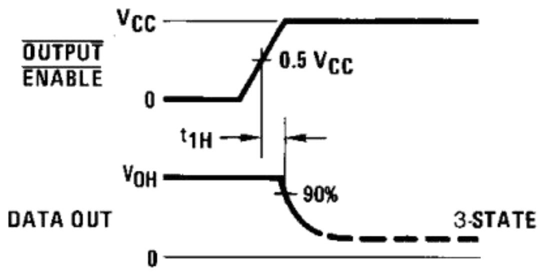
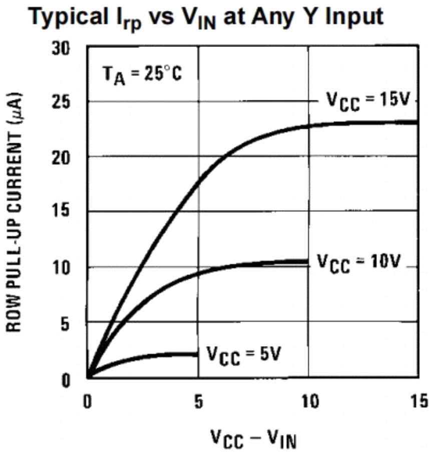
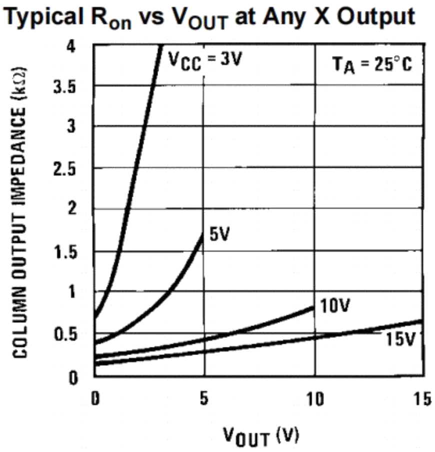
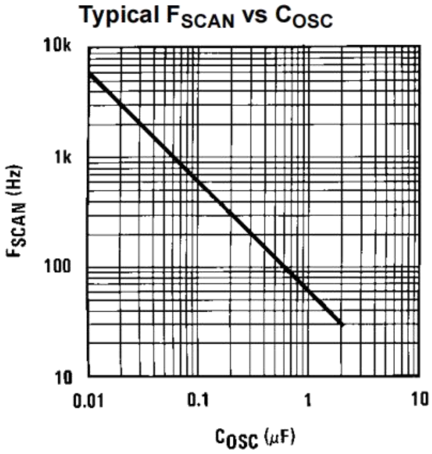


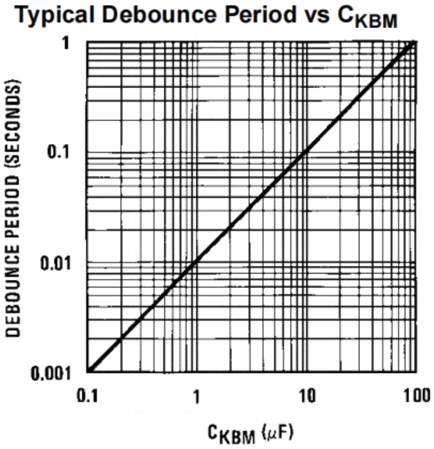
FIGURE 2.

Typical Performance Characteristics



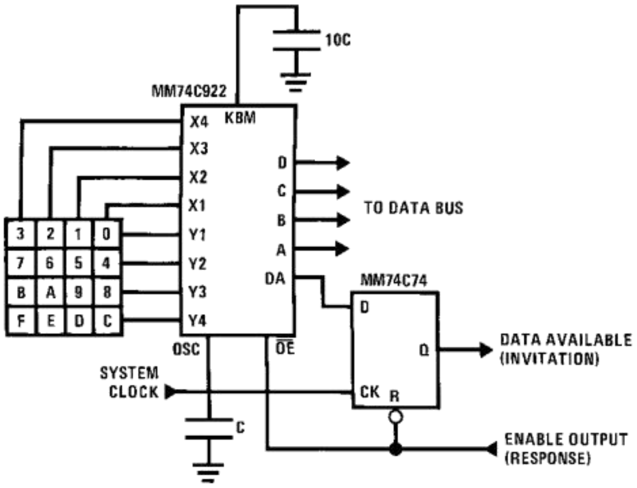




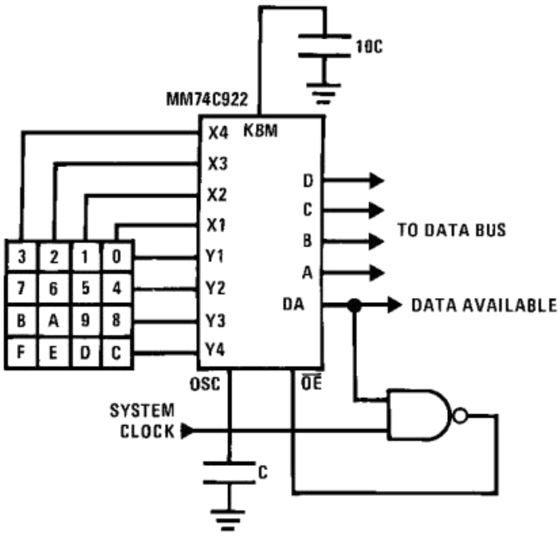


Typical Applications

Synchronous Handshake(74C922)
Synchronous Data Entry Onto Bus(74C922)



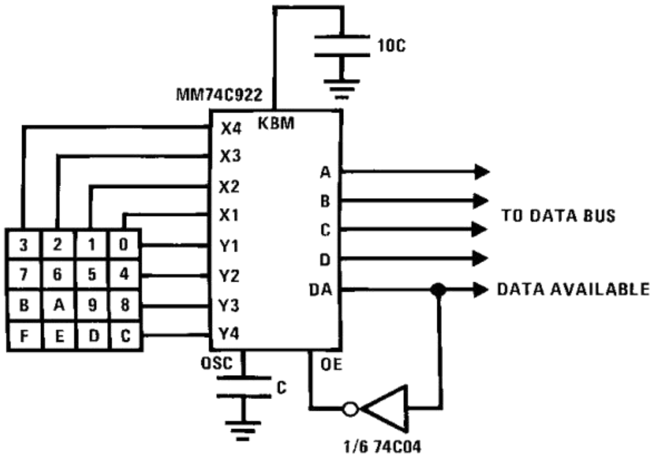
The keyboard may be synchronously scanned by omitting the capacitor at osc. and driving osc. directly if the system clock rate is lower than 10 kHz



Outputs are enabled when valid entry is made and go into 3-STATE when key is released.

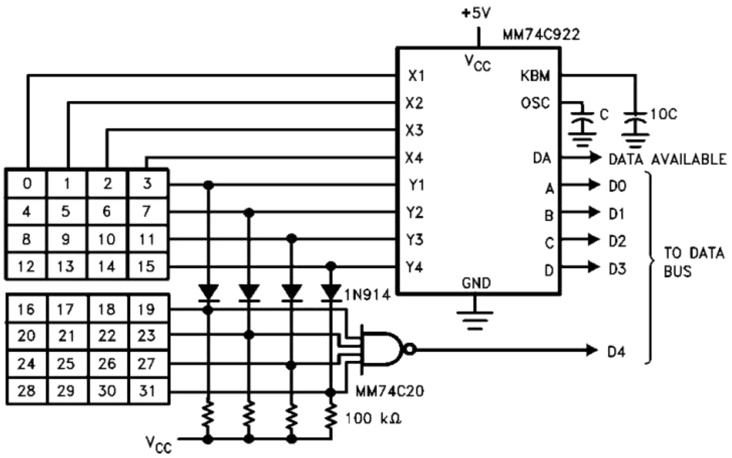
The keyboard may be synchronously scanned by omitting the capacitor at osc. and driving osc. directly if the system clock rate is lower than 10 kHz

Asynchronous Data Entry Onto Bus (74C922)



Outputs are in 3-STATE until key is pressed, then data is placed on bus. When key is released, outputs return to 3-STATE.

Expansion to 32 Key Encoder (74C922)



Theory of Operation

The 74C922/74C923 Keyboard Encoders implement all the logic necessary to interface a 16 or 20 SPST key switch matrix to a digital system. The encoder will con vert a key switch closer to a 4(74C922) or 5(74C923) bit nibble. The designer can control both the keyboard scan rate and the key debounce period by alter ing the oscillator capacitor, COSE, and the key bounce mask capacitor, CMSK . Thus, the 74C922/74C923's performance can be optimized for many keyboards.

The keyboard encoders connect to a switch matrix that is 4 rows by 4 columns (74C922) or 5 rows by 4 columns (74C923). When no keys are depressed, the row inputs are pulled high by internal pull-ups and the column outputs sequentially output a logic "0". These outputs are open drain and are therefore low for 25% of the time and other wise off. The column scan rate is controlled by the oscilla tor input, which consists of a Schmitt trigger oscillator, a 2- bit counter, and a 2–4-bit decoder.

When a key is depressed, key 0, for example, nothing will happen when the X1 input is off, since Y1 will remain high. When the X1 column is scanned, X1 goes low and Y1 will go low. This disables the counter and keeps X1 low. Y1going low also initiates the key bounce circuit timing and locks out the other Y inputs. The key code to be output is a combination of the frozen counter value and the decoded Y inputs. Once the key bounce circuit times out, the data is latched, and the Data Available (DAV) output goes high.

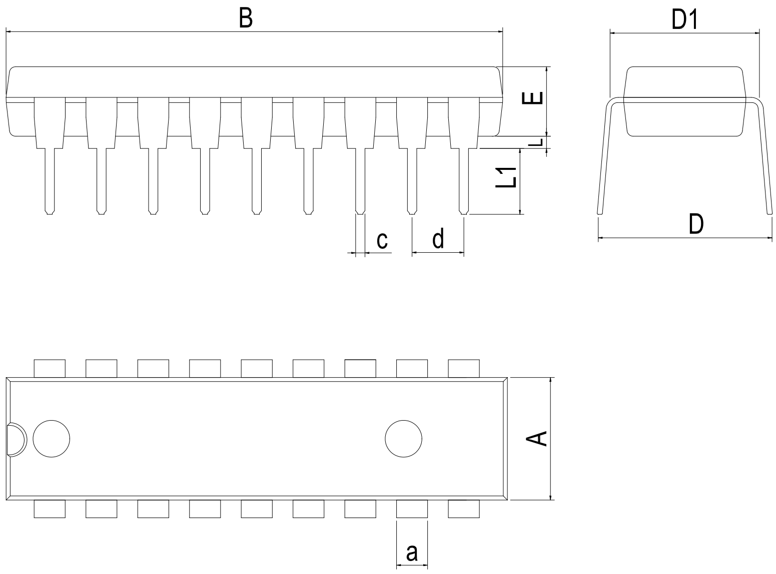
If, during the key closure the switch bounces, Y1 input will go high again, restarting the scan and resetting the key bounce circuitry. The key may bounce several times, but as soon as the switch stays low for a debounce period, the closure is assumed valid and the data is latched.

A key may also bounce when it is released. To ensure that the encoder does not recognize this bounce as another key closure, the debounce circuit must time out before another closure is recognized.

The two-key roll-over feature can be illustrated by assuming a key is depressed, and then a second key is depressed. Since all scanning has stopped, and all other Y inputs are disabled, the second key is not recognized until the first key is lifted and the key bounce circuitry has reset. The output latches feed 3-STATE, which is enabled when the Output Enable (OE) input is taken low.

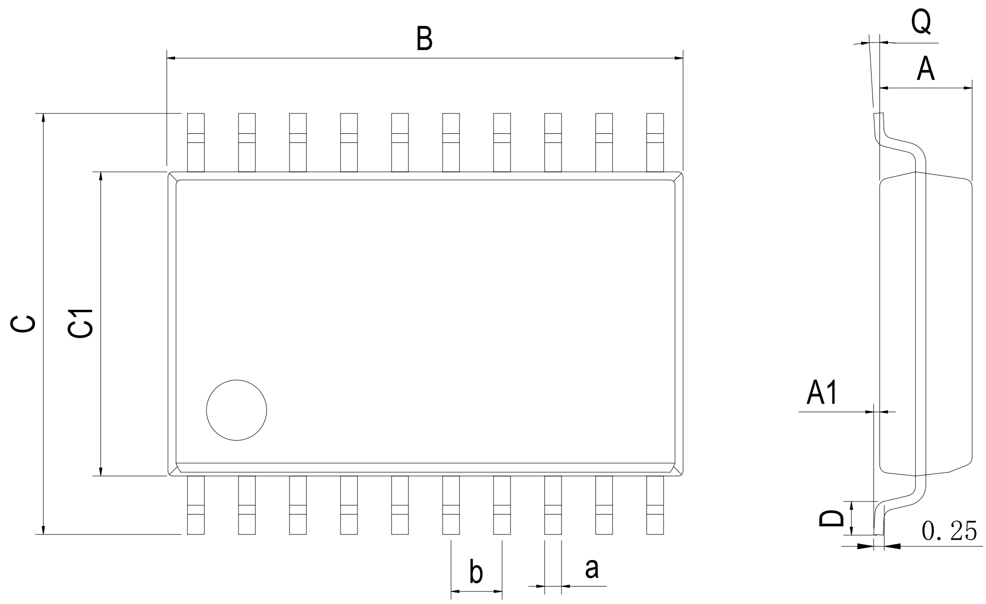
Physical Dimensions

DIP-18



Dimensions In Millimeters(DIP-18)										
Symbol:	A	B	D	D1	E	L	L1	a	c	d
Min:	6.10	22.24	8.10	7.42	3.10	0.50	3.00	1.50	0.40	2.54 BSC
Max:	6.68	23.24	10.9	7.82	3.55	0.70	3.60	1.55	0.50	

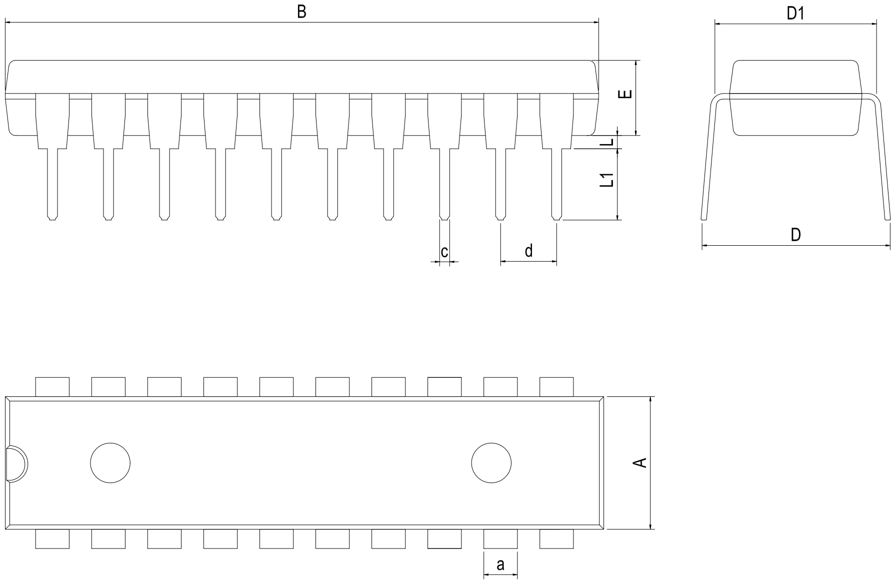
SOP-20W



Dimensions In Millimeters(SOP-20W)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	2.10	0.05	12.50	10.21	7.40	0.45	0°	0.35	1.27 BSC
Max:	2.50	0.25	13.00	10.61	7.60	1.25	8°	0.45	

Physical Dimensions

DIP-20



Dimensions In Millimeters(DIP-20)										
Symbol:	A	B	D	D1	E	L	L1	a	c	d
Min:	6.10	24.95	8.10	7.42	3.10	0.50	3.00	1.50	0.40	2.54 BSC
Max:	6.68	26.55	10.9	7.82	3.55	0.70	3.60	1.55	0.50	

Revision History

REVISION NUMBER	DATE	REVISION	PAGE
V1.0	2015-8	New	1-15
V1.1	2023-8	Update encapsulation type、Updated DIP-18、DIP-20 dimension	1、12、13
V1.2	2024-11	Update packages model SOP-20W、Update Lead Temperature	1、4
V1.3	2025-9	Update important statements	15

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