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74HC595PW-TP

8-Bit Shift Registers With Latched 3-State Outputs

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Features

- Input levels:CMOS level
- 8-bit serial input
- 8-bit serial or parallel output
- Shift register with direct clear
- Specified from -40℃to +85℃
- Storage register with 3-state outputs
- Packaging: TSSOP-16

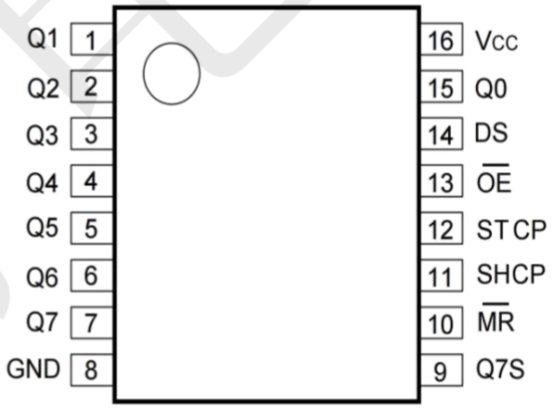
General Description

The devices contain and 8-bit, serial-in, parallel-out shift register that feeds an 8-bit D-type latch with parallel 3-state outputs. Separate clocks are provided for both the shift register and latch. The shift register has a direct overriding clear input, serial input, and serial outputs for cascading. This device also has an asynchronous reset for the shift register.

Applications

- Servers
- LED Displays
- Network Switches
- Power Infrastructure
- Serial-to-parallel data conversion
- Remote control holding register
- Shift register counter
- Sequential pulse generator

PIN CONFIGURATIONS (Top view)



TSSOP-16

PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION	PIN NO.	PIN NAME	DESCRIPTION
1	Q1	Parallel Data Q1 Output	9	Q7S	Serial Data Output
2	Q2	Parallel Data Q2 Output	10	$\overline{MR}$	Shift Register Reset Input(active LOW)
3	Q3	Parallel Data Q3 Output	11	SHCP	Shift Register Clock Input
4	Q4	Parallel Data Q4 Output	12	STCP	Parallel Latch Clock Input
5	Q5	Parallel Data Q5 Output	13	$\overline{OE}$	Output Enable(active LOW)
6	Q6	Parallel Data Q6 Output	14	DS	Serial Data Input
7	Q7	Parallel Data Q7 Output	15	Q0	Parallel Data Q0 Output
8	GND	Ground	16	VCC	Positive Power Supply

Function Table

Control				Input	Output		Function
SHCP	STCP	$\overline{OE}$	$\overline{MR}$	DS	Q7S	Qn	
X	X	L	L	X	L	NC	a LOW-level on $\overline{MR}$ only affects the shift registers
X	↑	L	L	X	L	L	empty shift register loaded into storage register
X	X	H	L	X	L	Z	shift register clear; parallel outputs in high - impedance OFF-state
↑	X	L	H	H	Q6S	NC	logic HIGH-level shifted into shift register stage 0. Contents of all shift register stages shifted through, e.g. previous state of stage 6 (internal Q6S) appears on the serial output(Q7S)
X	↑	L	H	X	NC	QnS	contents of shift register stages (internal QnS) are transferred to the storage register and parallel output stages
↑	↑	L	H	X	Q6S	QnS	contents of shift register shifted through; previous contents of the shift register is transferred to the storage register and the parallel output stages

Note: H=HIGH voltage level; L=LOW voltage level; Z=high-impedance OFF-state;↑=LOW-to-HIGH transition; X=don't care; NC=no change.

BLOCK DIAGRAM

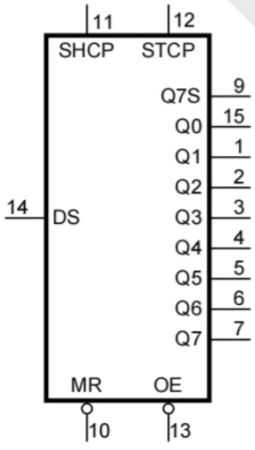


Figure 1. Logic symbol

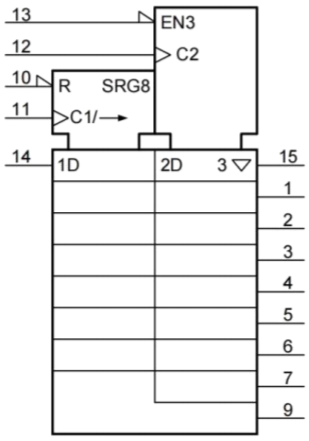


Figure 2. IEC logic symbol

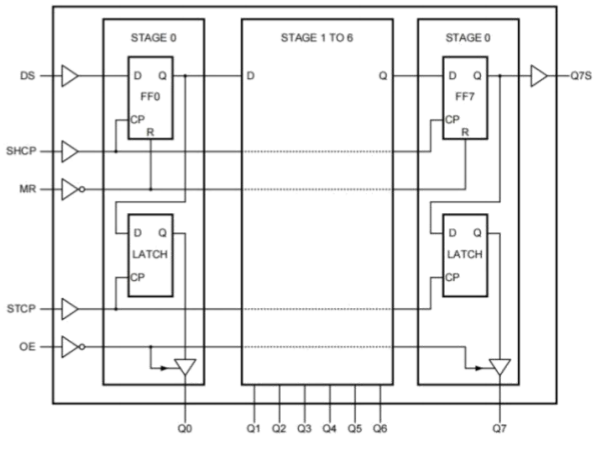


Figure 3. Logic diagram

Functional diagram

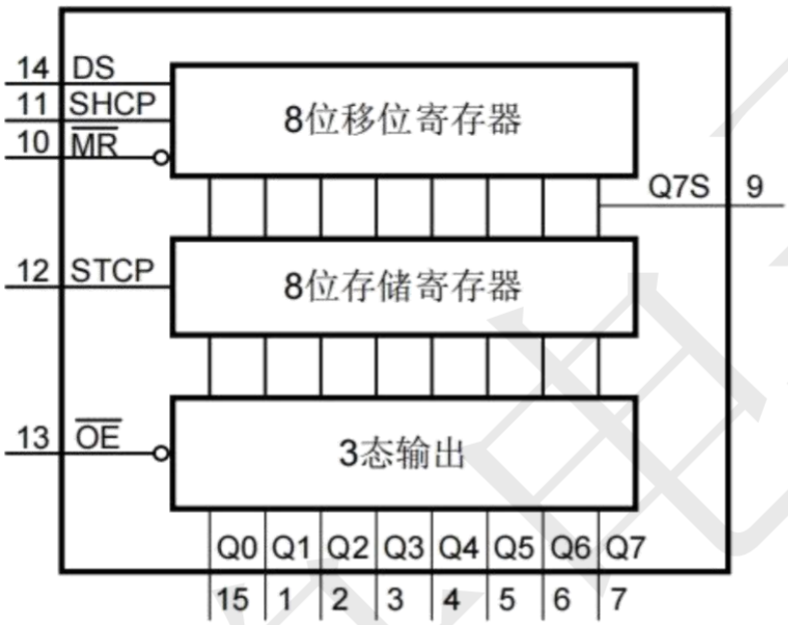
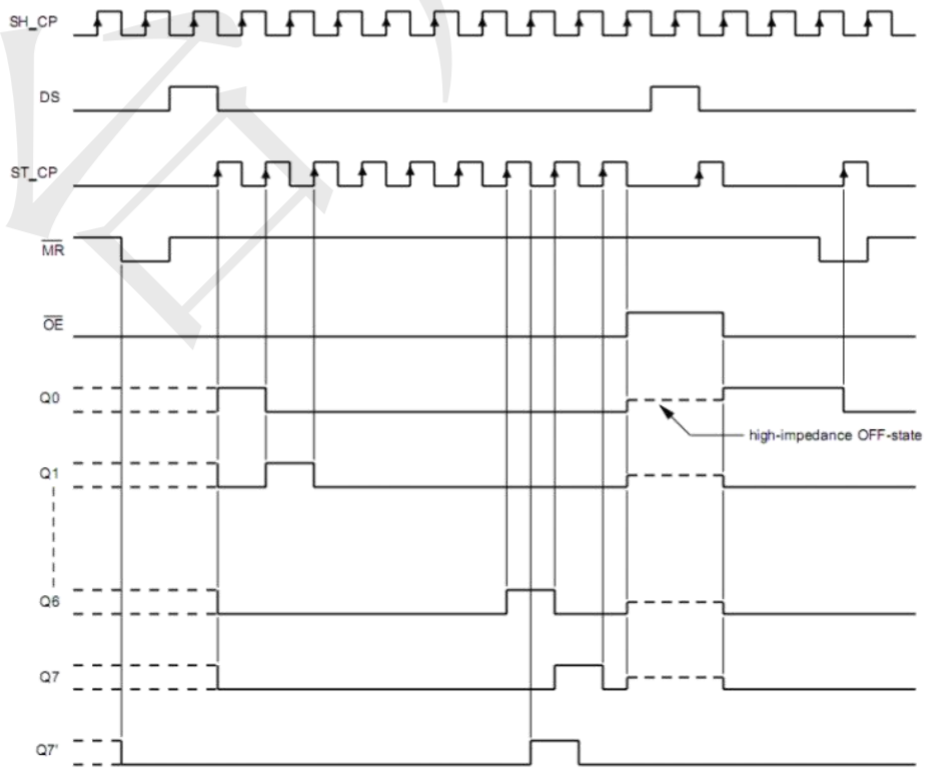


Figure 4. Functional diagram

Timing Table



ABSOLUTE MAXIMUM RATINGS

(Voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min	Max	Unit
supply voltage	V_{CC}			-0.5	+7.0	V
input clamping current	I_{IK}	V_I < -0.5V or V_I > V_{CC}+0.5V		--	±20	mA
output clamping current	I_{OK}	V_O < -0.5V or V_O > V_{CC}+0.5V		--	±20	mA
output current	I_O	V_O= -0.5V to (V_{CC}+0.5V)	pin Q7S	--	±25	mA
			pins Qn	--	±35	mA
supply current	I_{CC}	--		--	70	mA
ground current	I_{GND}	--		-70	--	mA
storage temperature	T_{stg}	--		-65	+150	℃
total power dissipation	P_{tot}	--		--	500	mW
soldering temperature	T_L	10s		260		℃

Note: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{CC}	--	2.0	5.0	6.0	V
Input voltage	V_I	--	0	--	V_{CC}	V
Output voltage	V_O	--	0	--	V_{CC}	V
Ambient temperature	T_{amb}	--	-40	--	+85	℃

DC ELECTRICAL CHARACTERISTICS 1

(T_{amb}=-40℃to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
HIGH-level input voltage	V_{IH}	V_{CC}=2.0V		1.5	1.2	--	V
		V_{CC}=4.5V		3.15	2.4	--	V
		V_{CC}=6.0V		4.2	3.2	--	V
LOW-level input voltage	V_{IL}	V_{CC}=2.0V		--	0.8	0.5	V
		V_{CC}=4.5V		--	1.35	1.0	V
		V_{CC}=6.0V		--	1.8	1.5	V
HIGH-level output voltage	V_{OH}	V_I= V_{IH} or V_{IL}	all outputs;I_O=-20uA; V_{CC}=2.0V	1.9	2.0	--	V
			all outputs;I_O=-20uA; V_{CC}=4.5V	4.4	4.5	--	V
			all outputs;I_O=-20uA; V_{CC}=6.0V	5.9	6.0	--	V
			Q7S output;I_O=-4.0mA; V_{CC}=4.5V	3.84	4.32	--	V
			Q7S output;I_O=-5.2mA; V_{CC}=6.0V	5.34	5.81	--	V
			Qn bus driver outputs; I_O=-6.0mA; V_{CC}=4.5V	3.84	4.32	--	V
			Qn bus driver outputs; I_O=-7.8mA; V_{CC}=6.0V	5.34	5.81	--	V
LOW-level output voltage	V_{OL}	V_I= V_{IH} or V_{IL}	all outputs; I_O=20uA; V_{CC}=2.0V	--	0	0.1	V
			all outputs; I_O=20uA; V_{CC}=4.5V	--	0	0.1	V
			all outputs; I_O=20uA; V_{CC}=6.0V	--	0	0.1	V
			Q7S output; I_O=4.0mA; V_{CC}=4.5V	--	0.15	0.33	V
			Q7S output; I_O=5.2mA; V_{CC}=6.0V	--	0.16	0.33	V
			Qn bus driver outputs; I_O=6.0mA; V_{CC}=4.5V	--	0.15	0.33	V
			Qn bus driver outputs; I_O=7.8mA; V_{CC}=6.0V	--	0.16	0.33	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=6.0V		--	--	±1.0	uA
OFF-state output current	I_{OZ}	V_I=V_{IH} or V_{IL}; V_{CC}=6.0V; V_O=V_{CC} or GND		--	--	±5.0	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		--	--	80	uA
input capacitance	C_I			--	3.5	--	pF

DC ELECTRICAL CHARACTERISTICS 2

(T_{amb}=-40℃to +125℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
HIGH-level input voltage	V_{IH}	V_{CC}=2.0V		1.5	-	-	V
		V_{CC}=4.5V		3.15	-	-	V
		V_{CC}=6.0V		4.2	-	-	V
LOW-level input voltage	V_{IL}	V_{CC}=2.0V		-	-	0.5	V
		V_{CC}=4.5V		-	-	1.0	V
		V_{CC}=6.0V		-	-	1.5	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}	all outputs;I_O=-20uA; V_{CC}=2.0V	1.9	-	-	V
			all outputs;I_O=-20uA; V_{CC}=4.5V	4.4	-	-	V
			all outputs;I_O=-20uA; V_{CC}=6.0V	5.9	-	-	V
			Q7S output;I_O=-4.0mA; V_{CC}=4.5V	3.7	-	-	V
			Q7S output;I_O=-5.2mA; V_{CC}=6.0V	5.2	-	-	V
			Qn bus driver outputs; I_O=-6.0mA; V_{CC}=4.5V	3.7	-	-	V
			Qn bus driver outputs; IO=-7.8mA; VCC=6.0V	5.2	-	-	V
LOW-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}	all outputs; I_O=20uA; V_{CC}=2.0V	-	-	0.1	V
			all outputs; I_O=20uA; V_{CC}=4.5V	-	-	0.1	V
			all outputs; I_O=20uA; V_{CC}=6.0V	-	-	0.1	V
			Q7S output; I_O=4.0mA; V_{CC}=4.5V	-	-	0.4	V
			Q7S output; I_O=5.2mA; V_{CC}=6.0V	-	-	0.4	V
			Qn bus driver outputs; I_O=6.0mA; V_{CC}=4.5V	-	-	0.4	V
			Qn bus driver outputs; I_O=7.8mA; V_{CC}=6.0V	-	-	0.4	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±1.0	uA
OFF-state output current	I_{OZ}	V_I=V_{IH} or V_{IL}; V_{CC}=6.0V; V_O=V_{CC} or GND		-	-	±10	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	160	uA

AC Electronics Characteristics 1

(T_{amb}=25℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min	Typ[1]	Max	Unit
propagation delay	t_{PLH}, t_{PHL}	SHCP to Q7S; see Figure 6	V_{CC}=2.0V	--	75	160	ns
			V_{CC}=4.5V	--	19	32	ns
			V_{CC}=6.0V	--	15	27	ns
		STCP to Qn; see Figure 7	V_{CC}=2.0V	--	85	175	ns
			V_{CC}=4.5V	--	20	35	ns
			V_{CC}=6.0V	--	16	30	ns
HIGH to LOW propagation delay	t_{PHL}	$\overline{MR}$ to Q7S; see Figure 9	V_{CC}=2.0V	--	47	175	ns
			V_{CC}=4.5V	--	17	35	ns
			V_{CC}=6.0V	--	14	30	ns
$\overline{OE}$ to Qn enable time	t_{PZH}, t_{PZL}	see Figure 10	V_{CC}=2.0V	--	47	150	ns
			V_{CC}=4.5V	--	17	30	ns
			V_{CC}=6.0V	--	14	26	ns
$\overline{OE}$ to Qn disable time	t_{PLZ}, t_{PHZ}	see Figure 10	V_{CC}=2.0V	--	41	150	ns
			V_{CC}=4.5V	--	15	30	ns
			V_{CC}=6.0V	--	12	27	ns
pulse width	t_W	SHCP HIGH or LOW; see Figure 6	V_{CC}=2.0V	75	17	--	ns
			V_{CC}=4.5V	15	6	--	ns
			V_{CC}=6.0V	13	5	--	ns
		STCP HIGH or LOW; see Figure 7	V_{CC}=2.0V	75	11	--	ns
			V_{CC}=4.5V	15	4	--	ns
			V_{CC}=6.0V	13	3	--	ns
		$\overline{MR}$ LOW; see Figure 9	V_{CC}=2.0V	75	17	--	ns
			V_{CC}=4.5V	15	6	--	ns
			V_{CC}=6.0V	13	5	--	ns
set-up time	t_{su}	DS to SHCP; see Figure 8	V_{CC}=2.0V	50	11	--	ns
			V_{CC}=4.5V	10	4	--	ns
			V_{CC}=6.0V	9	3	--	ns
		SHCP to STCP; see Figure 7	V_{CC}=2.0V	75	22	--	ns
			V_{CC}=4.5V	15	8	--	ns
			V_{CC}=6.0V	13	7	--	ns

AC Electronics Characteristics 1

(T_{amb}=25℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min	Typ[1]	Max	Unit
DS to SHCP hold time	t_h	see Figure 8	V_{CC}=2.0V	3	-6	--	ns
			V_{CC}=4.5V	3	-2	--	ns
			V_{CC}=6.0V	3	-2	--	ns
$\overline{MR}$ to SHCP recovery time	t_{rec}	see Figure 9	V_{CC}=2.0V	50	-19	--	ns
			V_{CC}=4.5V	10	-7	--	ns
			V_{CC}=6.0V	9	-6	--	ns
maximum frequency	f_{max}	SHCP or STCP; see Figure 6 and Figure 7	V_{CC}=2.0V	9	--	--	MHz
			V_{CC}=4.5V	30	--	--	MHz
			V_{CC}=6.0V	35	--	--	MHz

Note:[1] Typical values are measured at nominal supply voltage.

AC Electronics Characteristics 2

(T_{amb}=-40℃to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
propagation delay	t_{PLH}, t_{PHL}	SHCP to Q7S; see Figure 6	V_{CC}=2.0V	--	--	200	ns
			V_{CC}=4.5V	--	--	40	ns
			V_{CC}=6.0V	--	--	34	ns
		STCP to Qn; see Figure 7	V_{CC}=2.0V	--	--	220	ns
			V_{CC}=4.5V	--	--	44	ns
			V_{CC}=6.0V	--	--	37	ns
HIGH to LOW propagation delay	t_{PHL}	$\overline{MR}$ to Q7S; see Figure 9	V_{CC}=2.0V	--	--	220	ns
			V_{CC}=4.5V	--	--	44	ns
			V_{CC}=6.0V	--	--	37	ns
$\overline{OE}$ to Qn enable time	t_{PZH}, t_{PZL}	see Figure 10	V_{CC}=2.0V	--	--	190	ns
			V_{CC}=4.5V	--	--	38	ns
			V_{CC}=6.0V	--	--	33	ns
$\overline{OE}$ to Qn disable time	t_{PLZ}, t_{PHZ}	see Figure 10	V_{CC}=2.0V	--	--	190	ns
			V_{CC}=4.5V	--	--	38	ns
			V_{CC}=6.0V	--	--	33	ns
pulse width	t_W	SHCP HIGH or LOW; see Figure 6	V_{CC}=2.0V	95	--	--	ns
			V_{CC}=4.5V	19	--	--	ns
			V_{CC}=6.0V	16	--	--	ns

AC Electronics Characteristics 2

(T_{amb}=-40℃to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
pulse width	t_W	STCP HIGH or LOW; see Figure 7	V_{CC}=2.0V	95	--	--	ns
			V_{CC}=4.5V	19	--	--	ns
			V_{CC}=6.0V	16	--	--	ns
		$\overline{MR}$ LOW; see Figure 9	V_{CC}=2.0V	95	--	--	ns
			V_{CC}=4.5V	19	--	--	ns
			V_{CC}=6.0V	16	--	--	ns
set-up time	t_{su}	DS to SHCP; see Figure 8	V_{CC}=2.0V	65	--	--	ns
			V_{CC}=4.5V	13	--	--	ns
			V_{CC}=6.0V	11	--	--	ns
		SHCP to STCP; see Figure 7	V_{CC}=2.0V	95	--	--	ns
			V_{CC}=4.5V	19	--	--	ns
			V_{CC}=6.0V	16	--	--	ns
DS to SHCP hold time	t_h	see Figure 8	V_{CC}=2.0V	3	--	--	ns
			V_{CC}=4.5V	3	--	--	ns
			V_{CC}=6.0V	3	--	--	ns
$\overline{MR}$ to SHCP recovery time	t_{rec}	see Figure 9	V_{CC}=2.0V	65	--	--	ns
			V_{CC}=4.5V	13	--	--	ns
			V_{CC}=6.0V	11	--	--	ns
maximum frequency	f_{max}	SHCP or STCP; see Figure 6 and Figure 7	V_{CC}=2.0V	4.8	--	--	MHz
			V_{CC}=4.5V	24	--	--	MHz
			V_{CC}=6.0V	28	--	--	MHz

AC Electronics Characteristics 3

(T_{amb}=-40℃to +125℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
propagation delay	t_{PLH}, t_{PHL}	SHCP to Q7S; see Figure 6	V_{CC}=2.0V	--	--	240	ns
			V_{CC}=4.5V	--	--	48	ns
			V_{CC}=6.0V	--	--	41	ns
		STCP to Qn; see Figure 7	V_{CC}=2.0V	--	--	265	ns
			V_{CC}=4.5V	--	--	53	ns
			V_{CC}=6.0V	--	--	45	ns

AC Electronics Characteristics 3

(T_{amb}=-40℃to +125℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
HIGH to LOW propagation delay	t_{PHL}	$\overline{MR}$to Q7S; see Figure 9	V_{CC}=2.0V	--	--	265	ns
			V_{CC}=4.5V	--	--	53	ns
			V_{CC}=6.0V	--	--	45	ns
$\overline{OE}$ to Qn enable time	t_{PZH}, t_{PZL}	see Figure 10	V_{CC}=2.0V	--	--	225	ns
			V_{CC}=4.5V	--	--	45	ns
			V_{CC}=6.0V	--	--	38	ns
$\overline{OE}$ to Qn disable time	t_{PLZ}, t_{PHZ}	see Figure 10	V_{CC}=2.0V	--	--	225	ns
			V_{CC}=4.5V	--	--	45	ns
			V_{CC}=6.0V	--	--	38	ns
pulse width	t_W	SHCP HIGH or LOW;see Figure 6	V_{CC}=2.0V	110	--	--	ns
			V_{CC}=4.5V	22	--	--	ns
			V_{CC}=6.0V	19	--	--	ns
		STCP HIGH or LOW;see Figure 7	V_{CC}=2.0V	110	--	--	ns
			V_{CC}=4.5V	22	--	--	ns
			V_{CC}=6.0V	19	--	--	ns
		$\overline{MR}$ LOW; see Figure 9	V_{CC}=2.0V	110	--	--	ns
			V_{CC}=4.5V	22	--	--	ns
			V_{CC}=6.0V	19	--	--	ns
set-up time	t_{su}	DS to SHCP; see Figure 8	V_{CC}=2.0V	75	--	--	ns
			V_{CC}=4.5V	15	--	--	ns
			V_{CC}=6.0V	13	--	--	ns
		SHCP to STCP; see Figure 7	V_{CC}=2.0V	110	--	--	ns
			V_{CC}=4.5V	22	--	--	ns
			V_{CC}=6.0V	19	--	--	ns
DS to SHCP hold time	t_h	see Figure 8	V_{CC}=2.0V	3	--	--	ns
			V_{CC}=4.5V	3	--	--	ns
			V_{CC}=6.0V	3	--	--	ns
$\overline{MR}$ to SHCP recovery time	t_{rec}	see Figure 9	V_{CC}=2.0V	75	--	--	ns
			V_{CC}=6.0V	13	--	--	ns
maximum frequency	f_{max}	SHCP or STCP; see Figure 6 and Figure 7	V_{CC}=2.0V	4	--	--	MHz
			V_{CC}=4.5V	20	--	--	MHz
			V_{CC}=6.0V	24	--	--	MHz

Testing Circuit

AC Testing Circuit

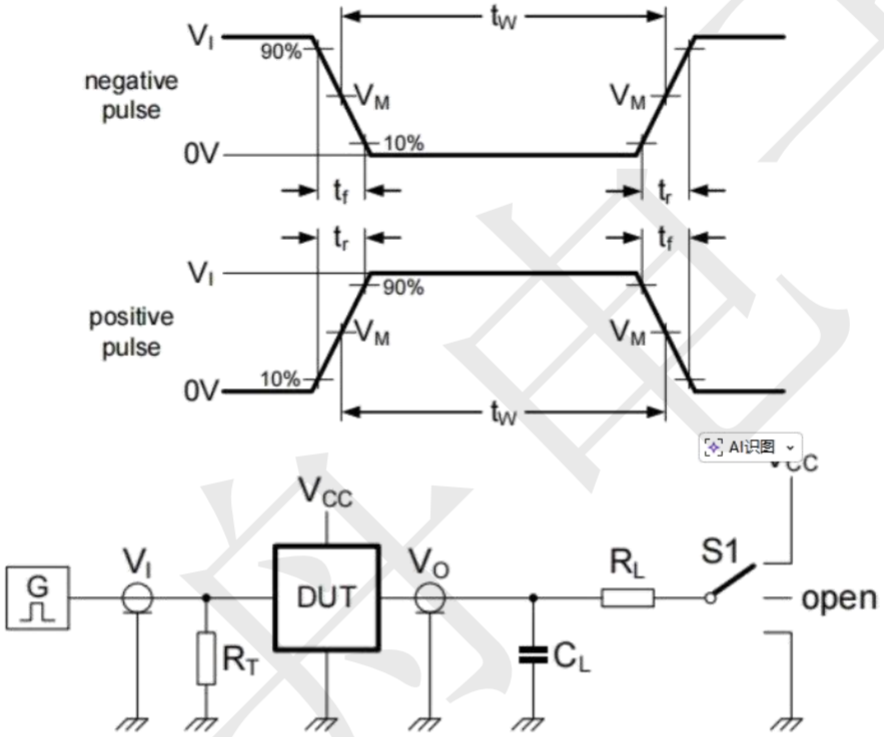


Figure 5. Test circuit for measuring switching times

Definitions for test circuit: R_L=Load resistance.

C_L=Load capacitance including jig and probe capacitance.

R_T=Termination resistance should be equal to the output impedance Z_o of the pulse generator.

S_1=Test selection switch.

AC Testing Waveforms 1

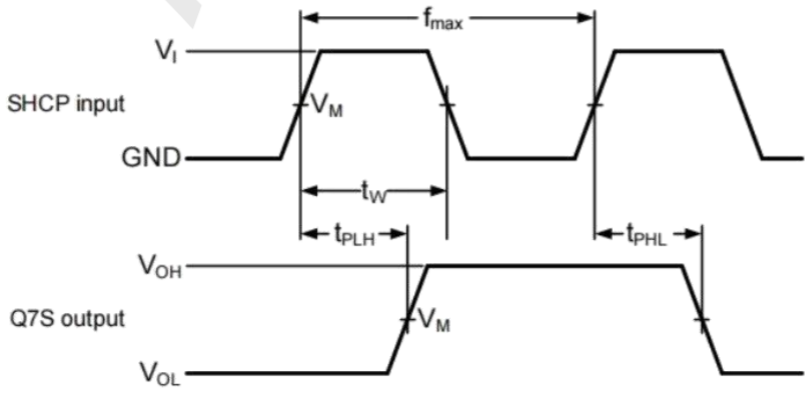


Figure 6. Shift clock pulse, maximum frequency and input to output propagation delays

AC Testing Waveforms 2

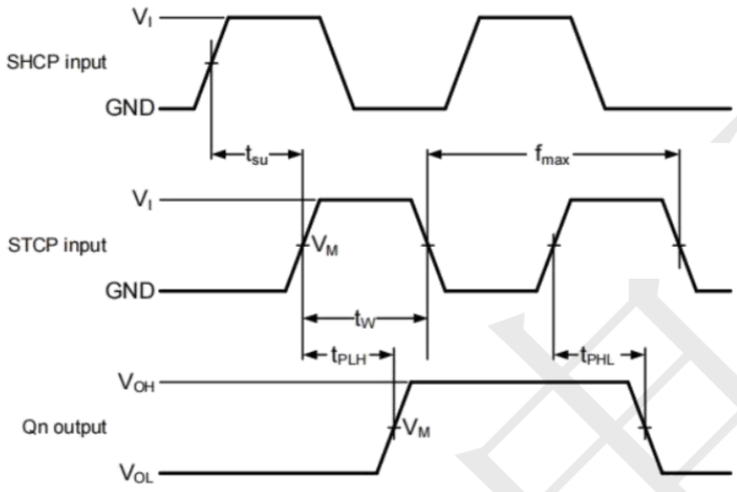


Figure 7. Storage clock to output propagation delays

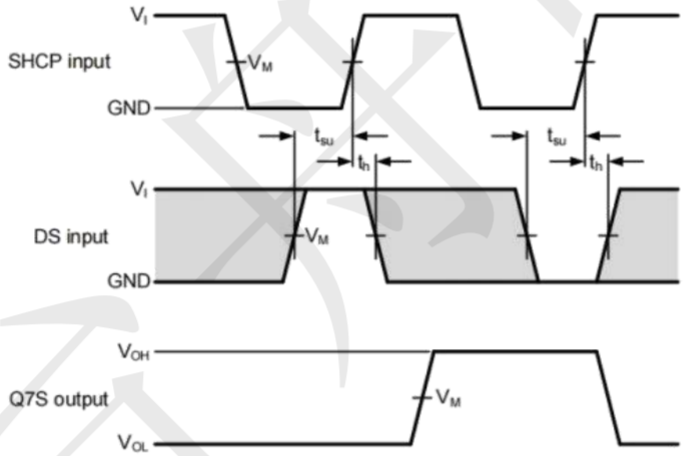


Figure 8. Data set-up and hold times

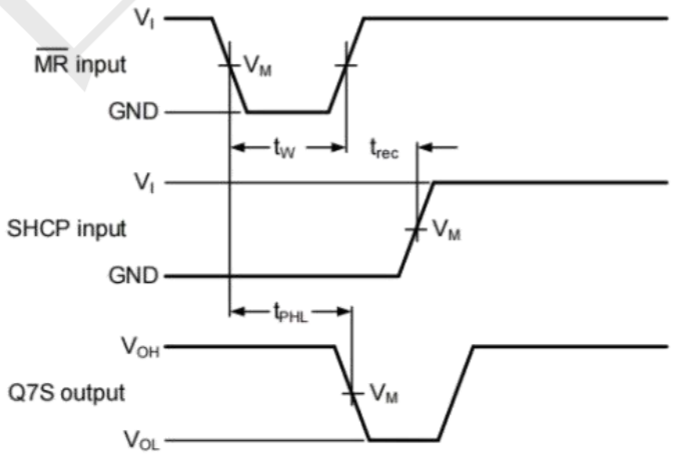


Figure 9. Master reset to output propagation delays

AC Testing Waveforms 3

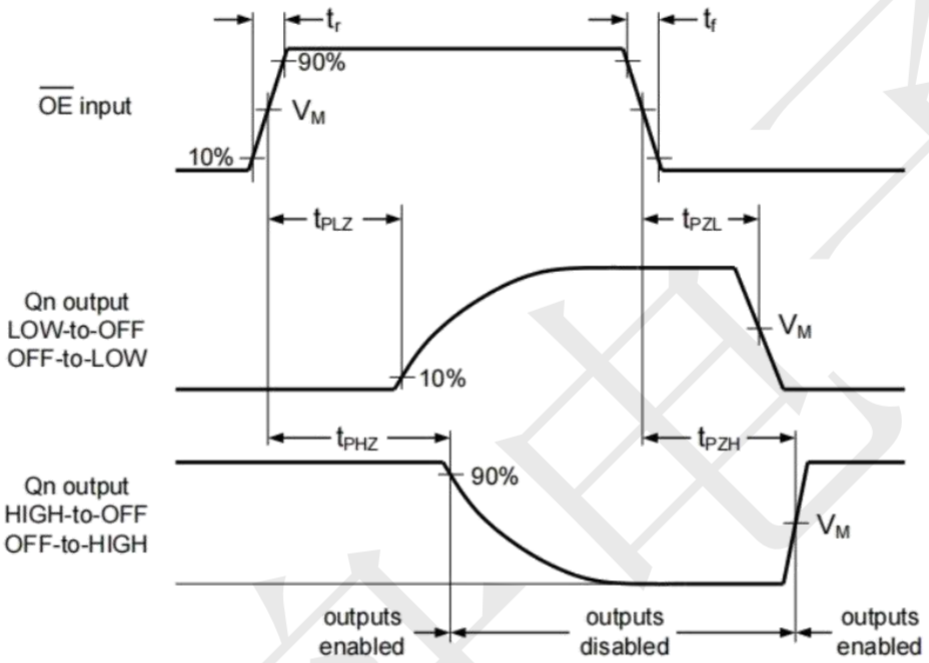


Figure 10. Enable and disable times

Measurement Points

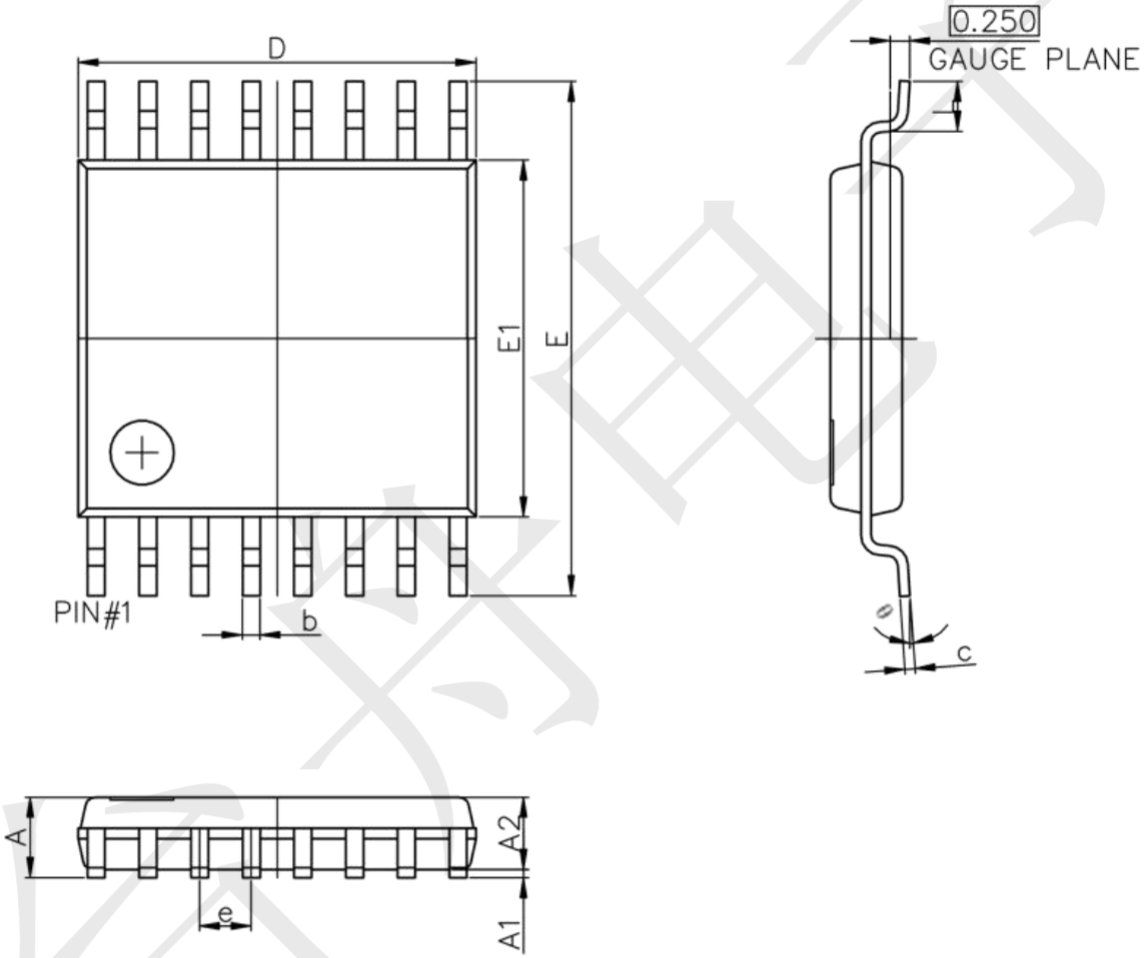
Type	Input	Output
	V_M	V_M
74HC595	0.5×V_{CC}	0.5×V_{CC}

Test Data

Type	Input		Load		S1 position		
	V_I	t_r , t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74HC595	V_{CC}	6ns	50pF	1kΩ	open	GND	V_{CC}

Package informantion

TSSOP-16



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	——	1.200	——	0.047
A1	0.020	0.100	0.001	0.004
A2	0.800	1.000	0.031	0.039
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	4.900	5.100	0.193	0.201
e	0.650(BSC)		0.026(BSC)	
E	6.250	6.550	0.252(BSC)	
E1	4.300	4.500	0.169	0.177
L	0.500	0.700	0.020	0.028
θ	1°	7°	1°	7°