MPQ4334

36V, 0.5A to 4A, Low Quiescent Current, Synchronous Step-Down Converter, AEC-Q100 Qualified

DESCRIPTION

The MPQ4334 is a configurable-frequency (200kHz to 2.5MHz), synchronous, step-down switching regulator with integrated internal high-side and low-side power MOSFETs (HS-FET and LS-FET, respectively). The device provides 0.5A to 4A of highly efficient output current (I_{OUT}) with peak current mode control.

The wide 3V to 36V input voltage (V_{IN}) range and 40V load dump tolerance accommodates a variety of step-down applications in automotive input environments. A 0.5µA shutdown current (I_{SD}) allows the device to be used in battery-powered applications.

High power conversion efficiency across a wide load range is achieved by scaling down the switching frequency (f_{SW}) under light-load conditions to reduce switching and gate driver losses. An open-drain power good (PG) signal indicates whether the output is within 94.5% to 105.5% of its nominal voltage.

Frequency foldback helps prevent inductor current (I_L) runaway during start-up. Thermal shutdown provides reliable, fault-tolerant operation. A high duty cycle and low-dropout (LDO) mode are provided for automotive cold-crank conditions.

The MPQ4334 is available in QFN-12 (2mmx3mm), QFN-12 (3mmx4mm), and QFN-14 (2.5mmx3.5mm) packages, and is AEC-Q100 qualified.

FEATURES

- Designed for Automotive Applications
  - Survives 40V Load Dump
  - Wide 3V to 36V Operating Input Voltage (V_{IN}) Range
  - Supports Cold Crank Down to 3V
  - Low-Dropout Mode with Soft Recovery
  - 0.5A to 4A Continuous Output Current (I_{OUT}) Versions in Pin-Compatible Family
  - 55ns Minimum On Time, 45ns Minimum Off Time
  - Available in AEC-Q100 Grade 1

FEATURES *(continued)*

- Increases Battery Life
  - 0.5µA Shutdown Current (I_{SD})
  - 20µA Sleep Mode Quiescent Current (I_Q)
  - Advanced Asynchronous Modulation (AAM) Mode Increases Light-Load Efficiency
  - Integrated 65mΩ HS-FET, 45mΩ LS-FET
- Optimized for EMC/EMI Reduction
  - CISPR 25 Class 5 Compliant
  - 200kHz to 2.5MHz Configurable f_{SW}
  - Synchronizable to an External Clock
  - Frequency Spread Spectrum (FSS)
  - Symmetric VIN Pinout
  - MeshConnect™ Flip-Chip Package
- Additional Features
  - Power Good (PG) Output
  - Over-Current Protection (OCP) with Hiccup Mode
  - Fixed-Output Options (1): 1V, 1.8V, 2.5V, 3V, 3.3V, 3.8V, or 5V
  - Available in QFN-12 (2mmx3mm), QFN-12 (3mmx4mm), and QFN-14 (2.5mmx3.5mm) Packages
  - Available in a Wettable Flank Package
- Functional Safety System Design Capable
  - MPSafe™ Compatible – Functional Safety Supporting Document Available

MPSafe™ FuSa Compatible

APPLICATIONS

- Automotive Infotainment Systems
- Automotive Clusters
- Advanced Driver-Assistance Systems
- Industrial Power Systems

Note:

1) See the Ordering Information section on page 3 for the exact availability of each fixed-output version. Additional output voltages may be available. Contact MPS for details.

TYPICAL APPLICATION

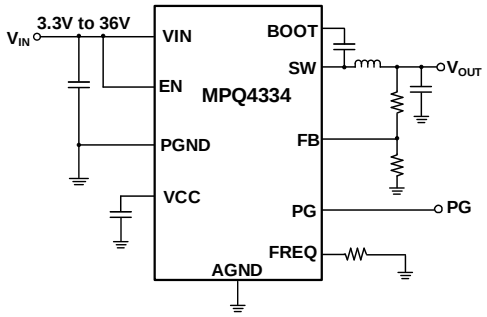


Figure 1: Typical Application (Adjustable Output, Configurable Switching Frequency)

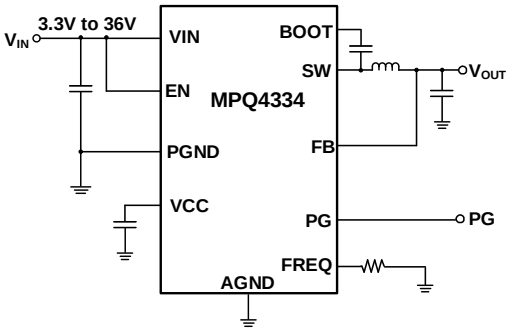


Figure 2: Typical Application (Fixed Output, Configurable Switching Frequency)

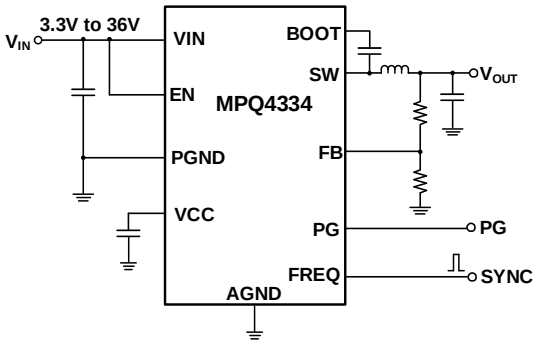


Figure 3: Typical Application (Adjustable Output, FREQ as SYNC)

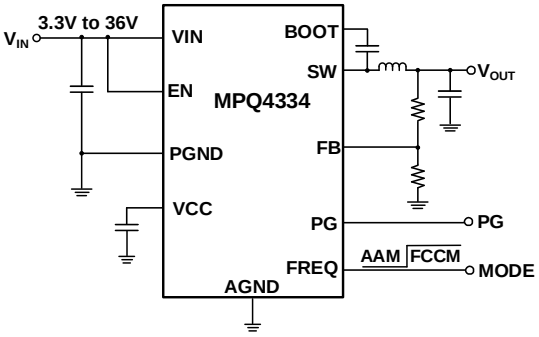
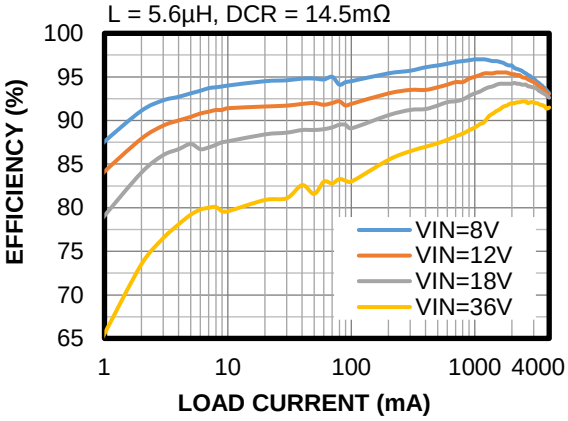


Figure 4: Typical Application (Adjustable Output, FREQ as MODE)

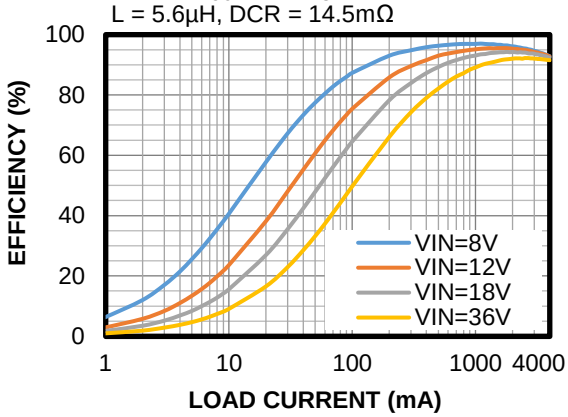
Efficiency vs. Load Current for 4000 Version

AAM mode, V_{OUT} = 5V, f_{SW} = 415kHz, L = 5.6µH, DCR = 14.5mΩ



Efficiency vs. Load Current for 4006 Version

FCCM, V_{OUT} = 5V, f_{SW} = 415kHz, L = 5.6µH, DCR = 14.5mΩ



ORDERING INFORMATION

Part Number (2) (3)*	Package	Top Marking	MSL Rating**
MPQ4334GDE-xxxx-AEC1***	QFN-12 (2mmx3mm)	*See Below*	1
MPQ4334GLE-xxxx-AEC1***	QFN-12 (3mmx4mm)	*See Below*	1
MPQ4334GRHE-xxxx-AEC1***	QFN-14 (2.5mmx3.5mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MPQ4334GDE-xxxx-AEC1-Z).

**Moisture Sensitivity Level Rating

***Wettable Flank

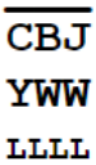
Notes:

2) Part numbers following the naming rules in Table 1 but not included in the Ordering Information table may be also available. Contact MPS for details.
3) The part number can be indicated as MPQ4334-WXYZ, with the naming rules for the four-digit code shown in Table 1.

Table 1: Part Number Digit Code Naming Rule

Digit Code	Naming Rule
W: Defines the supported load current	0: 0.5A
	1: 1A
	2: 2A
	3: 3A
	4: 4A
XY: Defines the output voltage (V_{OUT})	00: Adjustable output
	10: 1V fixed output
	18: 1.8V fixed output
	25: 2.5V fixed output
	30: 3V fixed output
	33: 3.3V fixed output
	38: 3.8V fixed output
	50: 5V fixed output
Z: Defines the control mode	0: Adjustable frequency, advanced asynchronous modulation (AAM) mode, frequency spread spectrum (FSS) on
	1: Internal 400kHz, FREQ as SYNC/MODE, FSS on
	2: Internal 2200kHz, FREQ as SYNC/MODE, FSS on
	3: Adjustable frequency, AAM mode, FSS off
	4: Internal 400kHz, FREQ as SYNC/MODE, FSS off
	5: Internal 2200kHz, FREQ as SYNC/MODE, FSS off
	6: Adjustable frequency, forced continuous conduction mode (FCCM), FSS on
	7: Adjustable frequency, FCCM, FSS off
	8: Internal 470kHz, FREQ as SYNC/MODE, FSS off

TOP MARKING (MPQ4334GDE-xxxx-AEC1)



CBJ: Product code
Y: Year code
WW: Week code
LLLL: Lot number

TOP MARKING (MPQ4334GLE-xxxx-AEC1)

MPYW
4334
LLL
E

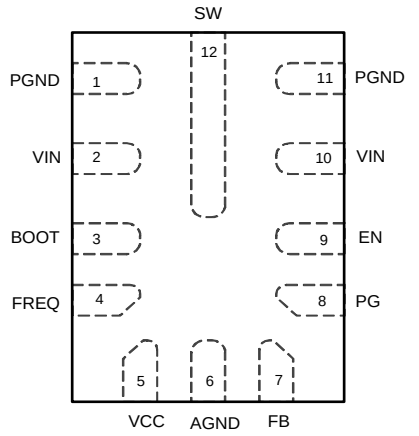
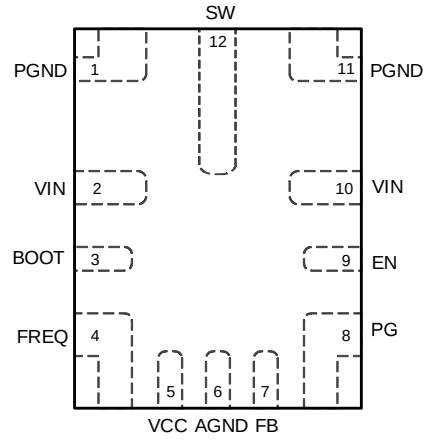
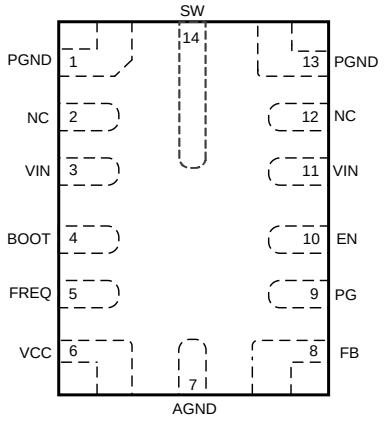
MP: MPS prefix
Y: Year code
W: Week code
4334: Part number
LLL: Lot number
E: Wettable flank

TOP MARKING (MPQ4334GRHE-xxxx-AEC1)

CFR
YWW
LLL

CFR: Product code
Y: Year code
WW: Week code
LLL: Lot number

PACKAGE REFERENCE

TOP VIEW	TOP VIEW	TOP VIEW
		
QFN-12 (2mmx3mm)	**QFN-12 (3mmx4mm)**	**QFN-14 (2.5mmx3.5mm)**

PIN FUNCTIONS

Pin #		Name	Description
QFN-12	QFN-14		
1, 11	1, 13	PGND	**Power ground.** Connect PGND to a large ground plane to ensure good heat dissipation.
2, 10	3, 11	VIN	**Input supply.** The VIN pin supplies power to all of the internal control circuitry and the power MOSFETs connected to SW. The two VIN pins are connected internally. Connect a decoupling capacitor from each VIN pin to PGND, placed as close as possible to the VIN pin, to minimize switching spikes and improve EMI performance.
3	4	BOOT	**Bootstrap.** The BOOT pin is the positive power supply for the high-side MOSFET (HS-FET) driver connected to SW. Connect a bypass capacitor between BOOT and SW.
4	5	FREQ	**Switching frequency configuration.** Depending on the value of "Z" in the four-digit code "XXYZ" (see Table 1 on page 3), the FREQ pin can be configured as FREQ or SYNC/MODE. If this pin is configured as FREQ, connect a resistor from the FREQ pin to ground to set f_{SW}. Table 3 on page 72 shows the detailed relationship between the FREQ resistor and f_{SW}. When configured as FREQ, do not float this pin. If this PIN is configured as SYNC/MODE, pulling this pin below the specified threshold 0.4V for advanced asynchronous modulation (AAM) mode operation or above the specified threshold 1.4V for forced continuous conduction mode (FCCM) operation. Tie this pin to an external 200kHz to 2.5MHz clock source to synchronize the converter with the external clock and operate in FCCM. This pin has one 100kΩ internal pull-down resistor when configured as SYNC/MODE. If this pin left floating when configured as SYNC/MODE, the part will operate in AAM. The AAM/FCCM setting can be changed during operation.
5	6	VCC	**Bias supply.** VCC is the output of the internal regulator that supplies power to the internal control circuit and gate drivers. Connect a minimum 1μF decoupling capacitor from VCC to ground, and place it as close as possible to the VCC pin.
6	7	AGND	**Analog ground.** Connect the AGND pin close to the VCC capacitor.
7	8	FB	**Feedback input.** The FB pin is the negative input of the error amplifier (EA) and sets the output voltage (V_{OUT}). For a fixed-output version, connect FB directly to V_{OUT}. For an adjustable-output version, connect FB to the middle point of the external feedback divider, which is between the output and AGND. The FB divider should be placed close to the FB pin.
8	9	PG	**Power good output.** The PG pin's output is an open drain. If PG is used, it must be connected to a power source through a pull-up resistor. If V_{OUT} is within 94.5% to 105.5% of its nominal voltage, PG goes high. If V_{OUT} exceeds 107% or is below 93% of its nominal voltage, PG goes low. Float the PG pin if it is not used.
9	10	EN	**Enable.** Pull the EN pin below the specified threshold (about 0.85V) to shut down the chip. Pull EN above the specified threshold (about 1.02V) to enable the chip. The EN pin does not have an internal pull-up or pull-down resistor. Do not float the EN pin.
12	14	SW	**Switch node.** The SW pin is the source of the HS-FET and the drain of the low-side MOSFET (LS-FET).
N/A	2, 12	NC	**Not connected.** The NC pin can be tied to PGND.

ABSOLUTE MAXIMUM RATINGS (4)

VIN, EN……..... -0.3V to +40V
SW…… -0.3V to $V_{IN(MAX)}$ + 0.3V
BOOT…….....V_{SW} + 5V
PG……..…-0.3V to + 9V
FB……..….-0.3V to + 6V
All other pins…… ..... -0.3V to +5V
Continuous power dissipation (T_A = 25°C) (5)
QFN-12 (2mmx3mm) …… 3.4W (9)
QFN-12 (3mmx4mm) …… 3.5W (10)
QFN-14 (2.5mmx3.5mm)...……..……3.5W (11)
Operating junction temperature.....+150°C
Lead temperature…….....+260°C
Storage temperature…….. -65°C to +150°C

ESD Ratings

Human body model (HBM) ……..……..Class 2 (6)
Charged device model (CDM).....Class C2b (7)

Recommended Operating Conditions

Supply voltage (V_{IN})……3V to 36V
Minimum V_{IN} for start-up ……3.8V
Minimum V_{IN} after start-up ……..…….....2.7V
Output voltage (V_{OUT})…….....0.8V to 0.95 x V_{IN}
Operating junction temp (T_J) … -40°C to +150°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-12 (2mmx3mm)
JESD51-7 …..….....60.4…...7.1….. °C/W(8)
EVQ4334-D-00A ……...36.8.....°C/W(9)
QFN-12 (3mmx4mm)
JESD51-7…..….....50……..9.4…..°C/W (8)
EVQ4334-L-00A.….....35.4….....°C/W (10)
QFN-14 (2.5mmx3.5mm)
JESD51-7…..….....51.3……..9.5…..°C/W (8)
EVQ4334-RH-00A…....35.6….....°C/W (11)

Ψ_{JT}

QFN-12 (2mmx3mm)
JESD51-7 …..…..……...1.9....°C/W (8)
EVQ4334-D-00A ……..…….....4.3....°C/W (9)
QFN-12 (3mmx4mm)
JESD51-7 …..…..……...3.....°C/W (8)
EVQ4334-L-00A.…….....4.8....°C/W (10)
QFN-14 (2.5mmx3.5mm)
JESD51-7 …..…..……...2.8.....°C/W (8)
EVQ4334-RH-00A…….....4.7....°C/W (11)

Notes:

4) Absolute maximum ratings are rated under room temperature, unless otherwise noted. Exceeding these ratings may damage the device.
5) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the device may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
6) Per AEC-Q100-002.
7) Per AEC-Q100-011.
8) Measured on JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application, the value of θ_{JC} shows the thermal resistance from junction-to-case bottom, and the value of Ψ_{JT} shows the characterization parameter from junction-to-case top.
9) Measured on MPS MPQ4334GDE-xxxx-AEC1 standard EVB, 8.3cmx8.3cm, 2oz copper thickness, 4-layer PCB, and the value of Ψ_{JT} shows the characterization parameter from junction-to-case top.
10) Measured on MPS MPQ4334GLE-xxxx-AEC1 standard EVB, 8.3cmx8.3cm, 2oz copper thickness, 4-layer PCB, and the value of ΨJT shows the characterization parameter from junction-to-case top.
11) Measured on MPS MPQ4334GRHE-xxxx-AEC1 standard EVB, 8.3cmx8.3cm, 2oz copper thickness, 4-layer PCB, and the value of Ψ_{JT} shows the characterization parameter from junction-to-case top.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Supply						
Input voltage (V_{IN}) under-voltage lockout (UVLO) rising threshold	$V_{IN\_UVLO\_RISING}$		3.4	3.6	3.8	V
V_{IN} UVLO falling threshold	$V_{IN\_UVLO\_FALLING}$		2.3	2.5	2.7	V
V_{IN} UVLO hysteresis	$V_{IN\_UVLO\_HYS}$			1100		mV
VIN quiescent current	I_Q	V_{FB} = 0.85V, AAM mode, no load, T_J = 25°C		20	28	µA
		V_{FB} = 0.85V, AAM mode, no load, T_J = -40°C to +125°C (12)			34	µA
		V_{FB} = 0.85V, AAM mode, no load, T_J = -40°C to +150°C			60	µA
VIN quiescent current (switching) (12)	$I_{Q\_SWITCHING}$	Switching, R_{FB1} = 1MΩ, R_{FB2} = 191kΩ, AAM mode, no load		25		µA
VIN active current (non-switching)	I_{Q_ACTIVE}	V_{FB} = 0.85V, FCCM, no load, non-switching		900		µA
VIN shutdown current	I_{SD}	V_{EN} = 0V		0.5	4	µA
V_{IN} over-voltage protection (OVP) rising threshold	$V_{IN\_OVP\_RISING}$		36.5	38.5	40.5	V
V_{IN} OVP falling threshold	$V_{IN\_OVP\_FALLING}$		35.5	37.5	39.5	V
V_{IN} OVP hysteresis	$V_{IN\_OVP\_HYS}$			1		V
Switching Frequency (f_{SW})						
Switching frequency (adjustable)	f_{SW_ADJ}	R_{FREQ} = 48.7kΩ, without FSS	381	415	449	kHz
		R_{FREQ} = 19.1kΩ, without FSS	920	1000	1080	kHz
		R_{FREQ} = 8.45kΩ, without FSS	2002	2200	2398	kHz
Switching frequency (fixed)	f_{SW_FIXED}	Control mode code (Z) = 1 or 4	372	400	428	kHz
		Control mode code (Z) = 8	437	470	503	kHz
		Control mode code (Z) = 2 or 5	2024	2200	2376	kHz
Frequency spread spectrum (FSS) span				±10		%
FSS modulation frequency				7.5		kHz
Minimum on time (12)	t_{ON_MIN}			55	80	ns
Minimum off time (12)	t_{OFF_MIN}			45	65	ns
Maximum duty cycle	D_{MAX}		98	99.5		%
Switch leakage current	I_{SW_LKG}	V_{SW} = V_{BOOT} = 0V or V_{IN}, V_{EN} = 0V, T_J = 25°C		0.5	1	µA
		V_{SW} = V_{BOOT} = 0V or V_{IN}, V_{EN} = 0V, T_J = -40°C to +150°C		0.5	8	µA

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
High-side MOSFET (HS-FET) on resistance	R_{ON_HS}	V_{BOOT} - V_{SW} = 3.3V		65	125	mΩ
Low-side MOSFET (LS-FET) on resistance	R_{ON_LS}	V_{CC} = 3.3V		45	90	mΩ
Output and Regulation						
Feedback (FB) voltage	V_{FB}	T_J = 25°C, adjustable output, f_{SW} = 2.2MHz	0.794	0.8	0.806	V
		T_J = 25°C, adjustable output, f_{SW} = 400kHz	0.790	0.8	0.810	V
		T_J = -40°C to +150°C, adjustable output	0.790	0.8	0.810	V
FB input current	I_{FB}	Adjustable output		0	100	nA
		Fixed output		3		µA
Output voltage accuracy of 3.3V fixed output version	$V_{OUT\_3.3V}$	T_J = 25°C	3250	3300	3350	mV
		T_J = -40°C to +150°C	3234	3300	3366	mV
Output voltage accuracy of 3.8V fixed output version	$V_{OUT\_3.8V}$	T_J = 25°C	3743	3800	3857	mV
		T_J = -40°C to +150°C	3724	3800	3876	mV
Output voltage accuracy of 5V fixed output version	V_{OUT_5V}	T_J = 25°C	4925	5000	5075	mV
		T_J = -40°C to +150°C	4900	5000	5100	mV
V_{OUT} discharge current	$I_{DISCHARGE}$	V_{EN} = 0V, V_{SW} = 0.3V	2	3.2		mA
Bootstrap (BOOT)						
BOOT - SW refresh rising	V_{BOOT_RISING}			2.4	2.9	V
BOOT - SW refresh falling	$V_{BOOT\_FALLING}$			2.2	2.7	V
BOOT - SW refresh hysteresis	V_{BOOT_HYS}			0.2		V
Enable (EN)						
EN rising threshold	V_{EN_RISING}		0.97	1.02	1.07	V
EN falling threshold	$V_{EN\_FALLING}$		0.8	0.85	0.9	V
EN threshold hysteresis	V_{EN_HYS}			170		mV
EN to switching delay (12)	t_{ENSD}			750		µs
EN to PG high delay	t_{ENPD}		5.4	5.7	6.2	ms
Soft Start (SS) and VCC						
Soft-start time	t_{SS}	Internal V_{SS} from 0V to 1.2V	3	4	6	ms
VCC voltage	V_{CC}	I_{VCC} = 0A	3	3.3	3.6	V
VCC regulation		I_{VCC} = 30mA		1		%
VCC current limit	I_{LIMIT_VCC}	V_{CC} = 2.5V	80	120		mA
SYNC/Mode						
SYNC/MODE voltage rising threshold	V_{SYNC_RISING}		1.4			V
SYNC/MODE voltage falling threshold	$V_{SYNC\_FALLING}$				0.4	V

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
SYNC/MODE timeout (12)	t_{MODE}	SYNC/MODE low to DCM			120	µs
SYNCIN clock range (of free-running frequency)	f_{SYNC_400kHz}	Control mode code (Z) = 1 or 4	85%		115%	f_{SW}
	f_{SYNC_470kHz}	Control mode code (Z) = 8	85%		115%	f_{SW}
	$f_{SYNC\_2.2MHz}$	Control mode code (Z) = 2 or 5	90%		110%	f_{SW}
SYNCIN clock locking time	t_{SYNC_LOCK}	SYNC clock locking time			128	cycle
SYNCIN clock duty	D_{SYNC_DUTY}	SYNC clock duty for min input clock edge >40ns	20		80	%
f_{SW} After SYNC		f_{SW} accuracy compares to f_{SYNC}	-5		+5	%
Power Good (PG)						
PG rising threshold	PG_{VTH_RISING}	V_{OUT} rising, V_{FB} / V_{REF}	92.5	94.5	96.5	%
		V_{OUT} falling, V_{FB} / V_{REF}	103.5	105.5	107.5	
PG falling threshold	$PG_{VTH\_FALLING}$	V_{OUT} falling, V_{FB} / V_{REF}	91	93	95	%
		V_{OUT} rising, V_{FB} / V_{REF}	105	107	109	
PG threshold hysteresis	PG_{VTH_HYS}	V_{FB} / V_{REF}		1.5		%
PG output voltage low	V_{PG_LOW}	I_{SINK} = 1mA		0.1	0.3	V
PG rising deglitch time	t_{PG_R}		160	200	260	µs
PG falling deglitch time	t_{PG_F}		160	210	270	µs
Protections						
HS peak current limit	I_{LIMIT_HS}	30% duty cycle, 0.5A version	1	1.35	1.85	A
		30% duty cycle, 1A version	1.5	2	2.6	A
		30% duty cycle, 2A version	2.8	3.4	4	A
		30% duty cycle, 3A version	4.8	5.8	6.8	A
		30% duty cycle, 4A version	5.4	6.5	7.6	A
LS valley current limit	I_{LIMIT_LS}	0.5A version	0.7	1	1.5	A
		1A version	1	1.5	2	A
		2A version	2	2.7	3.8	A
		3A version	3.4	4.4	5.4	A
		4A version	3.9	5	6.1	A
Zero-current detection (ZCD) current	I_{ZCD}	AAM mode	-0.05	0.05	+0.15	A
LS reverse current limit	$I_{LIMIT\_REVERSE}$	FCCM		3		A
Thermal shutdown (12)	T_{SD}		160	175	185	°C
Thermal shutdown hysteresis (12)	T_{SD_HYS}			20		°C

Note:

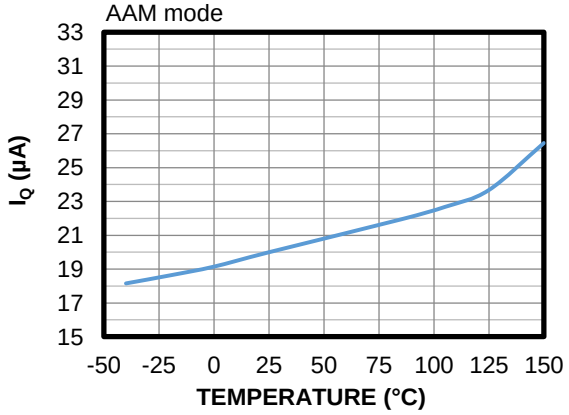
12) Guaranteed by design and characterization. Not tested in production.

TYPICAL CHARACTERISTICS

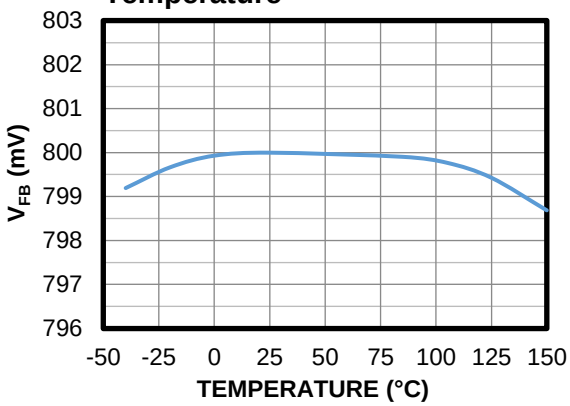
V_{IN} = 12V, unless otherwise noted.

Quiescent Current vs. Temperature

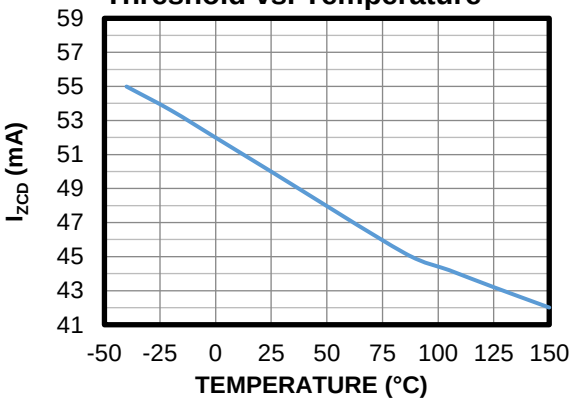
AAM mode



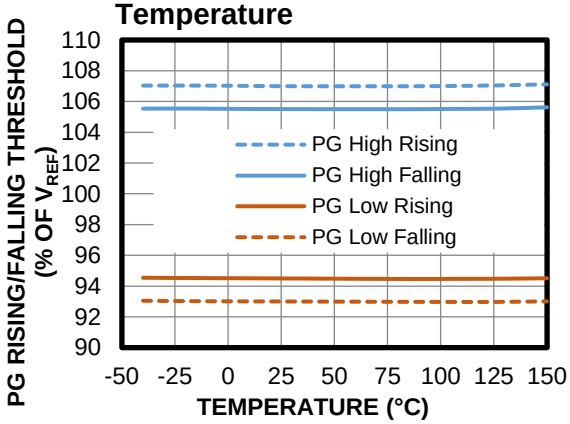
Feedback Voltage vs. Temperature



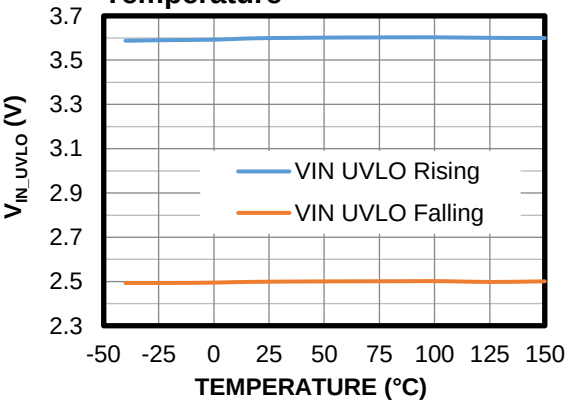
Zero-Current Detection Threshold vs. Temperature



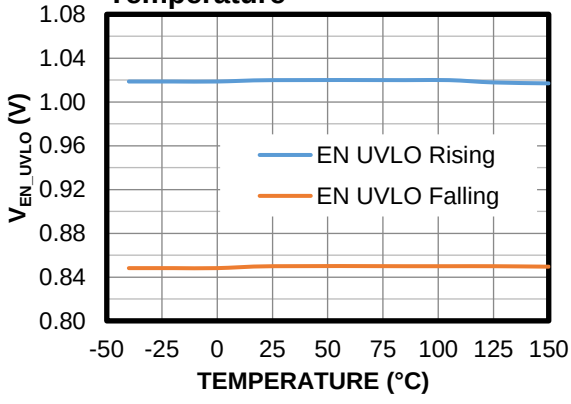
PG Rising/Falling Threshold vs. Temperature



V_{IN} UVLO Threshold vs. Temperature



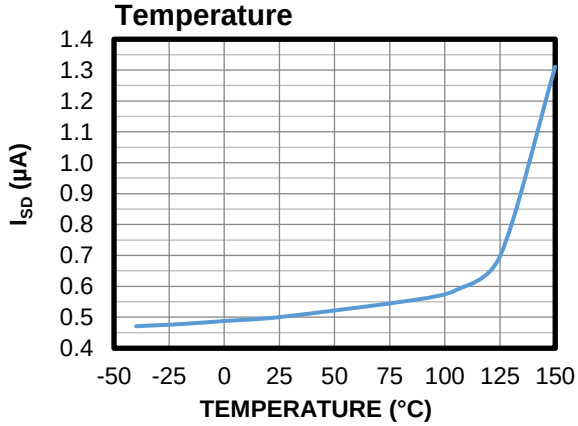
EN UVLO Threshold vs. Temperature



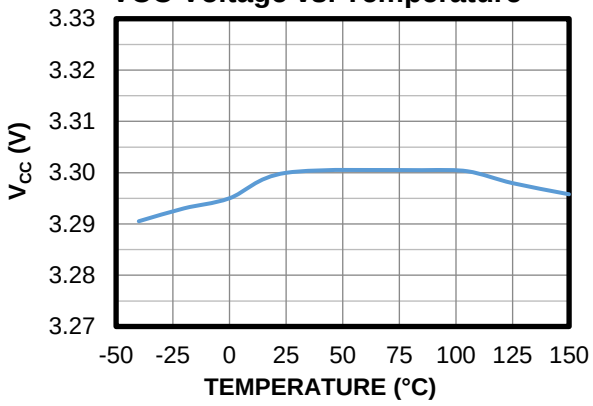
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, unless otherwise noted.

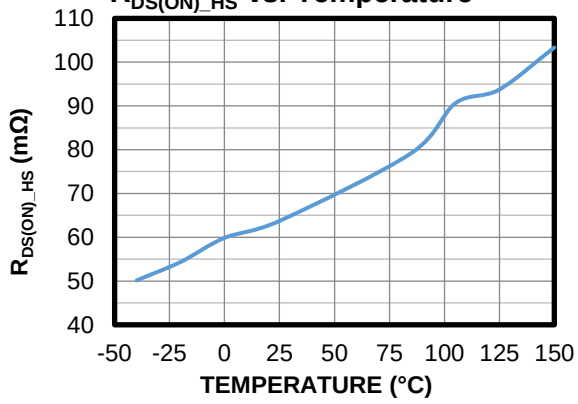
V_{IN} Shutdown Current vs. Temperature



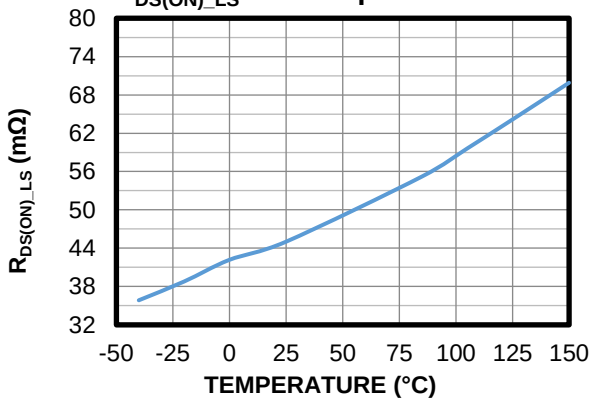
VCC Voltage vs. Temperature



$R_{DS(ON)\_HS}$ vs. Temperature

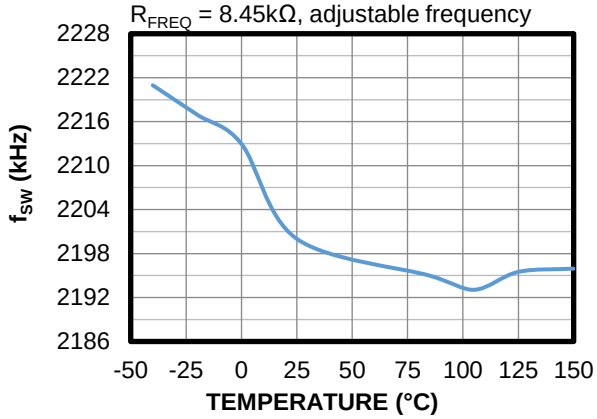


$R_{DS(ON)\_LS}$ vs. Temperature



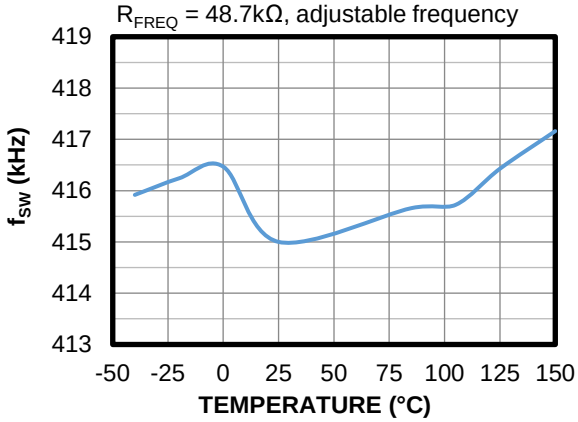
Switching Frequency vs. Temperature

R_{FREQ} = 8.45kΩ, adjustable frequency



Switching Frequency vs. Temperature

R_{FREQ} = 48.7kΩ, adjustable frequency

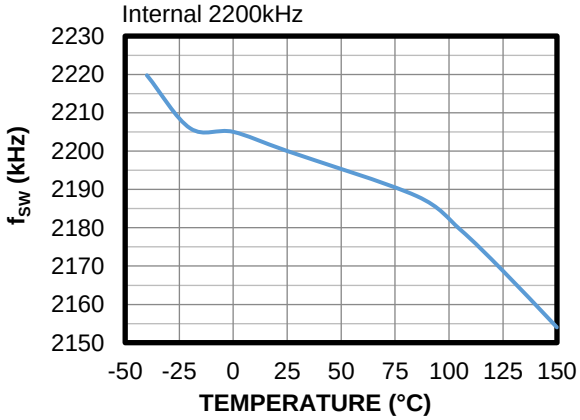


TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, unless otherwise noted.

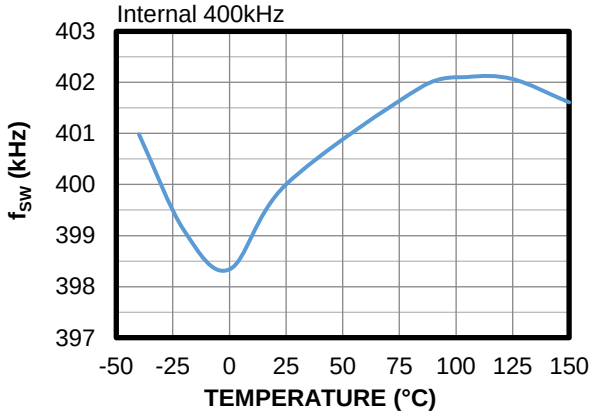
Switching Frequency vs. Temperature

Internal 2200kHz



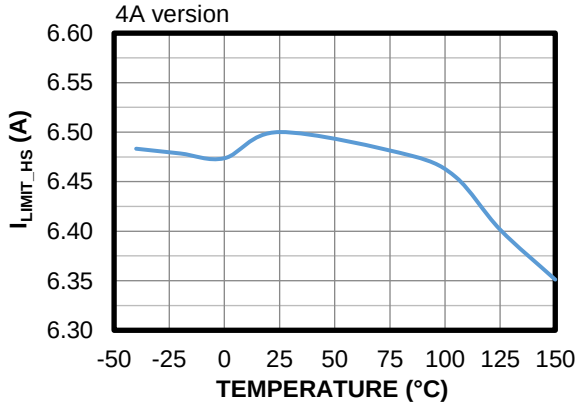
Switching Frequency vs. Temperature

Internal 400kHz



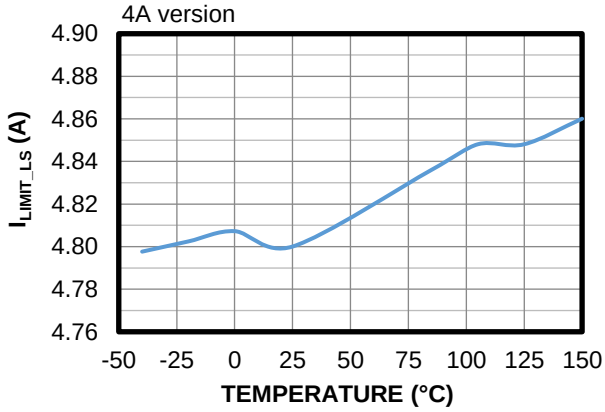
High-Side Peak Current Limit vs. Temperature

4A version



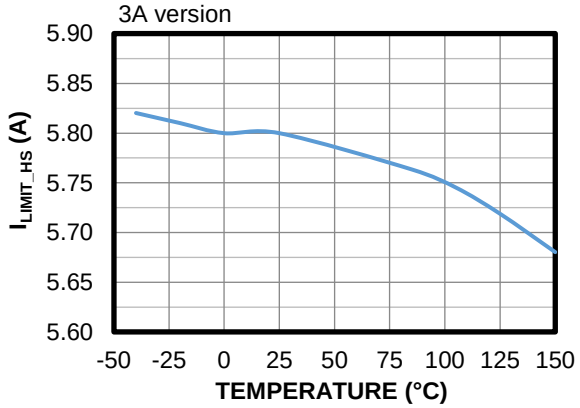
Low-Side Peak Current Limit vs. Temperature

4A version



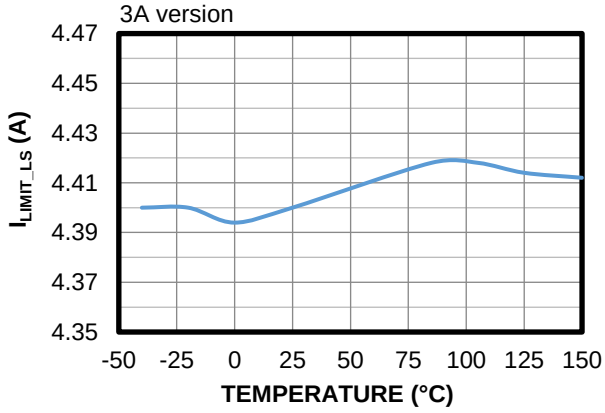
High-Side Peak Current Limit vs. Temperature

3A version



Low-Side Peak Current Limit vs. Temperature

3A version

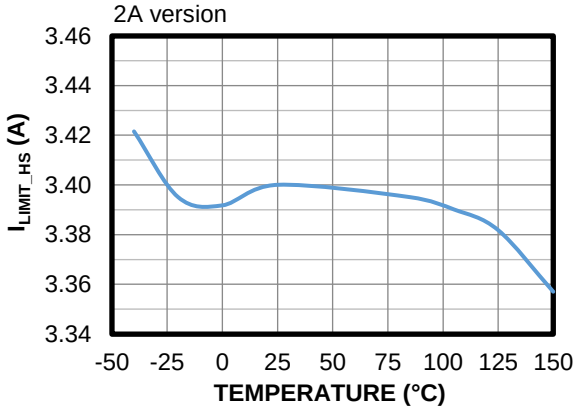


TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, unless otherwise noted.

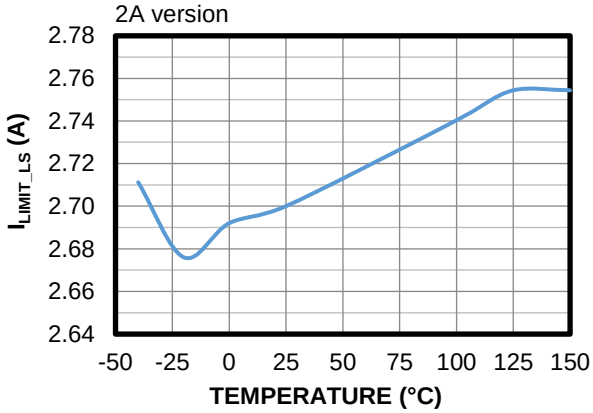
High-Side Peak Current Limit vs. Temperature

2A version



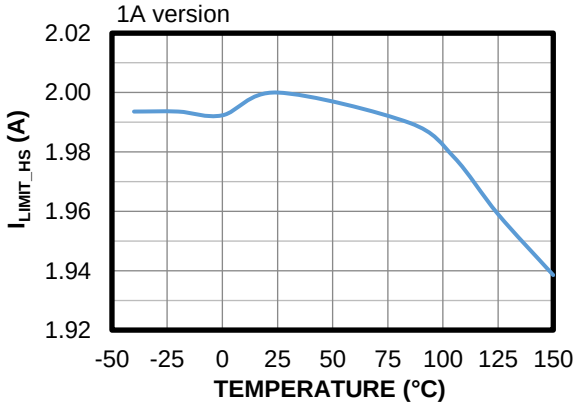
Low-Side Peak Current Limit vs. Temperature

2A version



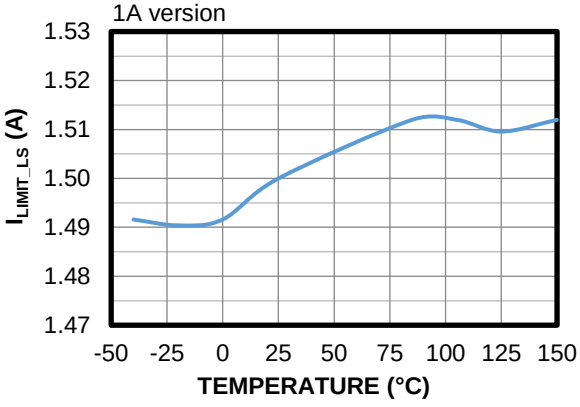
High-Side Peak Current Limit vs. Temperature

1A version



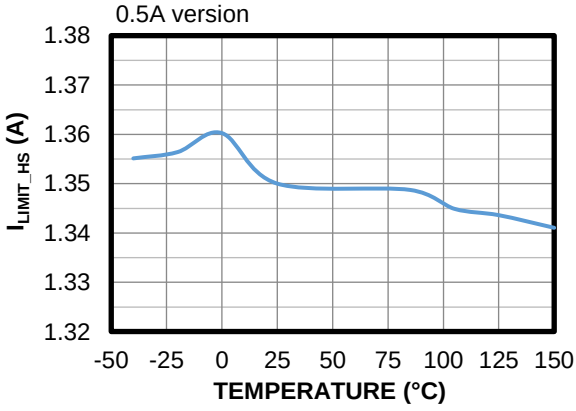
Low-Side Peak Current Limit vs. Temperature

1A version



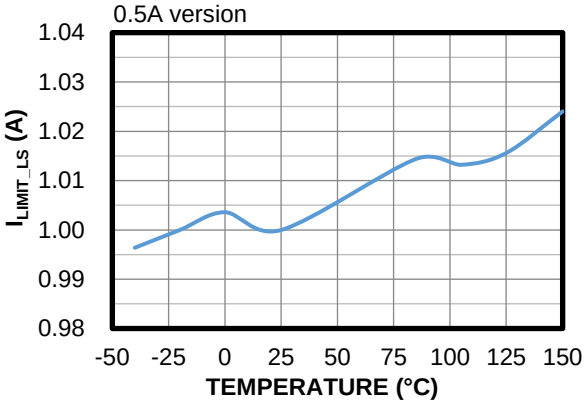
High-Side Peak Current Limit vs. Temperature

0.5A version



Low-Side Peak Current Limit vs. Temperature

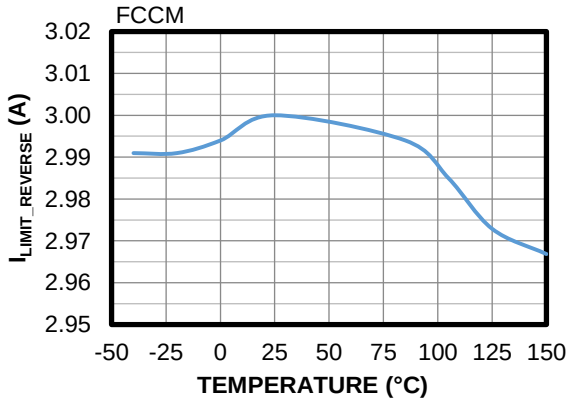
0.5A version



TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, unless otherwise noted.

Reverse Current Limit vs. Temperature

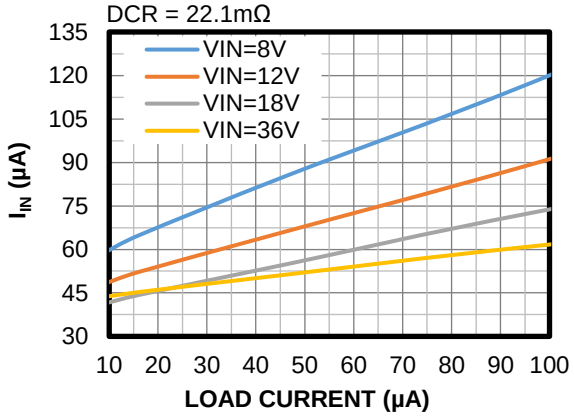


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

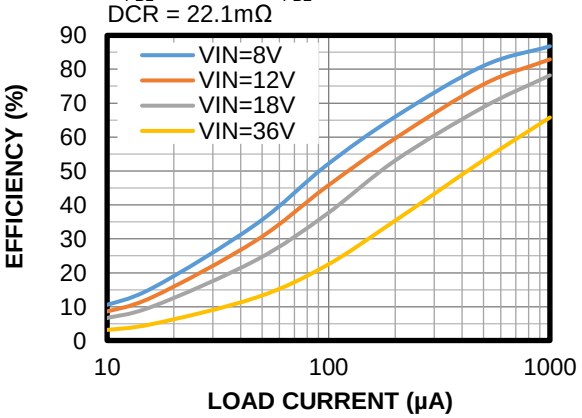
Input Current vs. Load Current for 4000 Version

R_{FB1} = 100kΩ, R_{FB2} = 19.1kΩ, DCR = 22.1mΩ



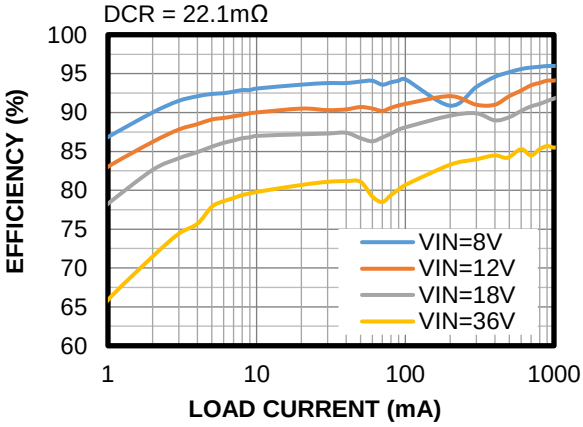
Efficiency vs. Load Current for 4000 Version

R_{FB1} = 100kΩ, R_{FB2} = 19.1kΩ, DCR = 22.1mΩ



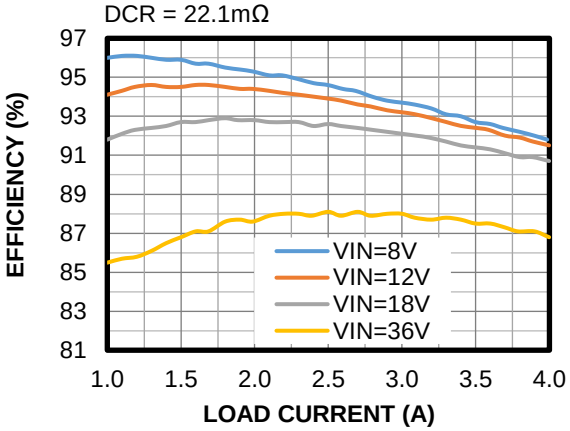
Efficiency vs. Load Current for 4000 Version

DCR = 22.1mΩ



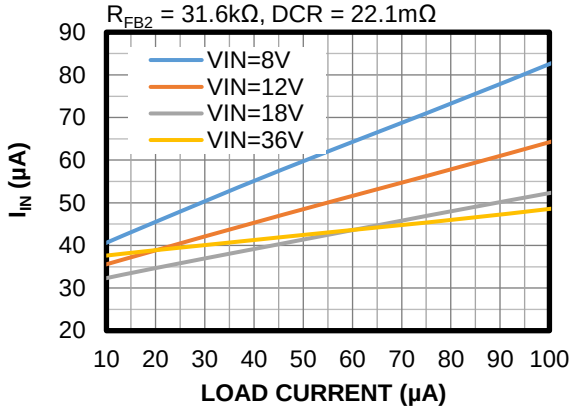
Efficiency vs. Load Current for 4000 Version

DCR = 22.1mΩ



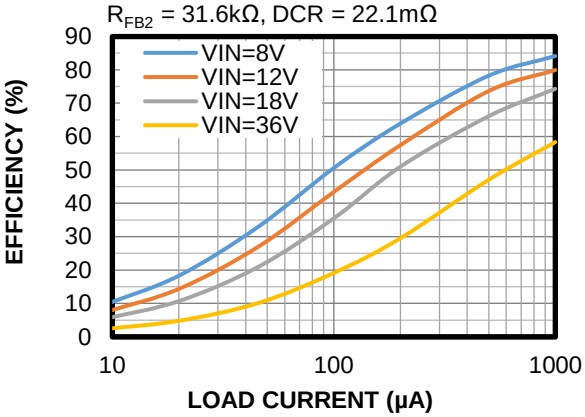
Input Current vs. Load Current for 4000 Version

V_{OUT} = 3.3V, R_{FB1} = 100kΩ, R_{FB2} = 31.6kΩ, DCR = 22.1mΩ



Efficiency vs. Load Current for 4000 Version

V_{OUT} = 3.3V, R_{FB1} = 100kΩ, R_{FB2} = 31.6kΩ, DCR = 22.1mΩ

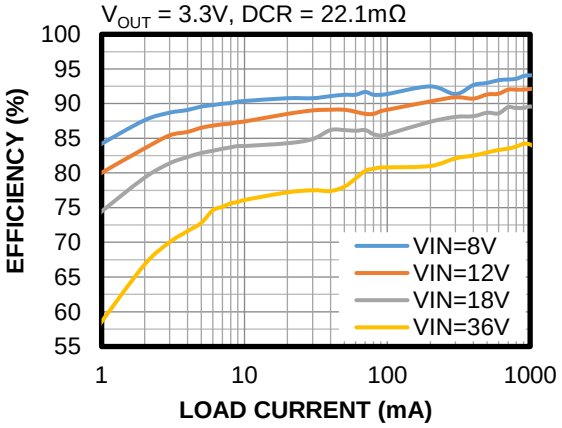


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

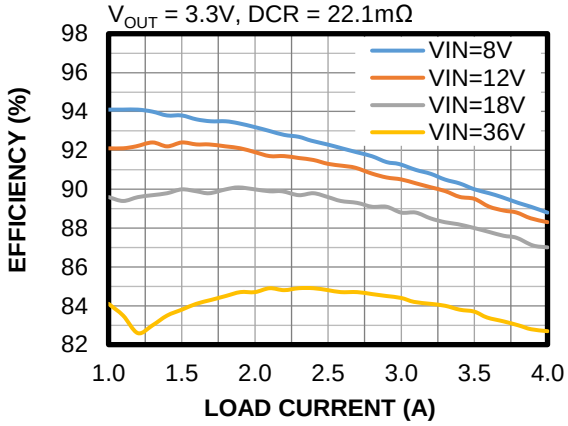
Efficiency vs. Load Current for 4000 Version

V_{OUT} = 3.3V, DCR = 22.1mΩ



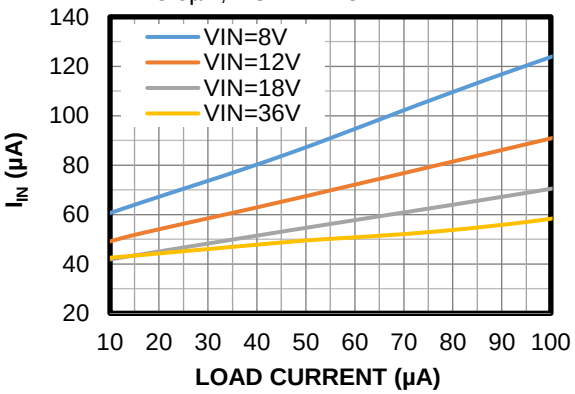
Efficiency vs. Load Current for 4000 Version

V_{OUT} = 3.3V, DCR = 22.1mΩ



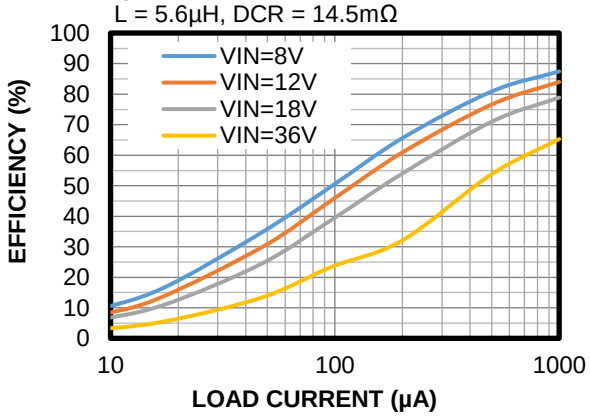
Input Current vs. Load Current for 4000 Version

f_{SW} = 415kHz, R_{FB1} = 100kΩ, R_{FB2} = 19.1kΩ, L = 5.6µH, DCR = 14.5mΩ



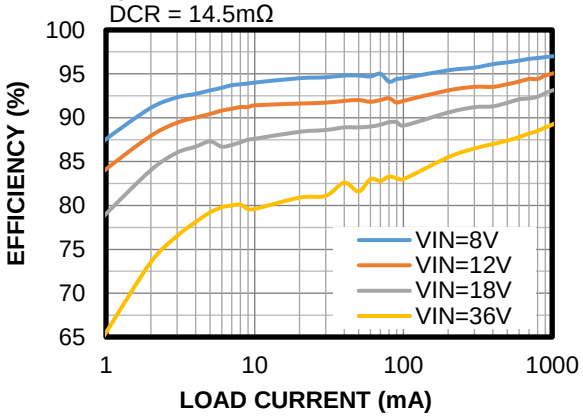
Efficiency vs. Load Current for 4000 Version

f_{SW} = 415kHz, R_{FB1} = 100kΩ, R_{FB2} = 19.1kΩ, L = 5.6µH, DCR = 14.5mΩ



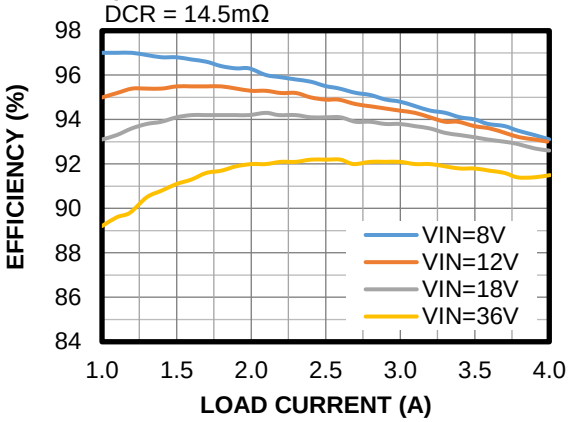
Efficiency vs. Load Current for 4000 Version

f_{SW} = 415kHz, L = 5.6µH, DCR = 14.5mΩ



Efficiency vs. Load Current for 4000 Version

f_{SW} = 415kHz, L = 5.6µH, DCR = 14.5mΩ

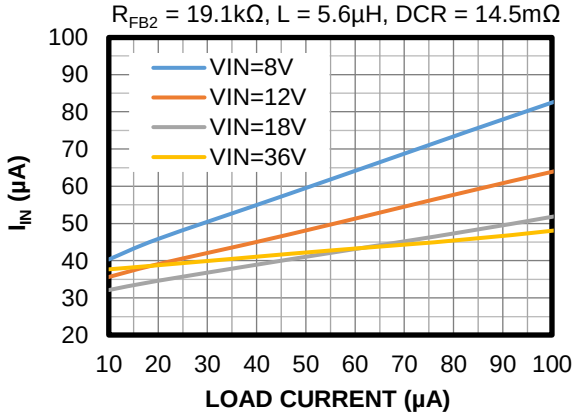


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

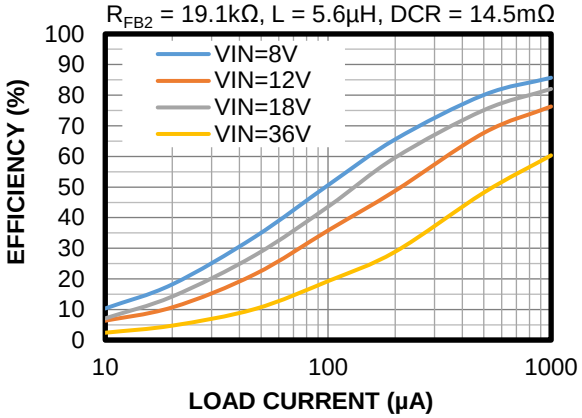
Input Current vs. Load Current for 4000 Version

V_{OUT} = 3.3V, f_{SW} = 415kHz, R_{FB1} = 100kΩ, R_{FB2} = 19.1kΩ, L = 5.6µH, DCR = 14.5mΩ



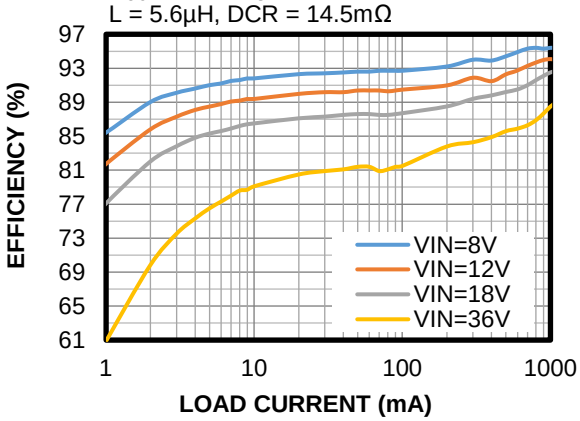
Efficiency vs. Load Current for 4000 Version

V_{OUT} = 3.3V, f_{SW} = 415kHz, R_{FB1} = 100kΩ, R_{FB2} = 19.1kΩ, L = 5.6µH, DCR = 14.5mΩ



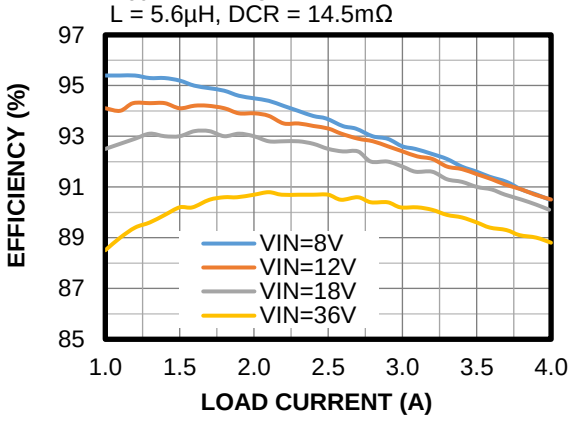
Efficiency vs. Load Current for 4000 Version

V_{OUT} = 3.3V, f_{SW} = 415kHz, L = 5.6µH, DCR = 14.5mΩ



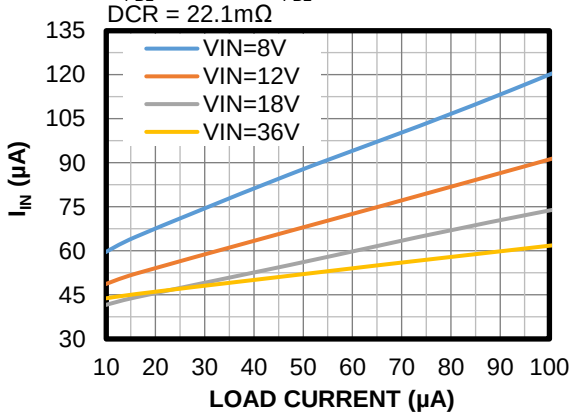
Efficiency vs. Load Current for 4000 Version

V_{OUT} = 3.3V, f_{SW} = 415kHz, L = 5.6µH, DCR = 14.5mΩ



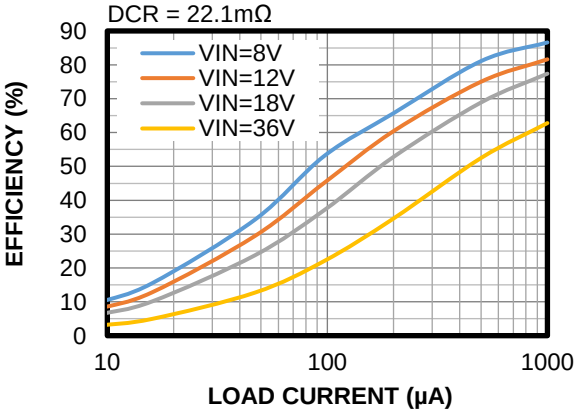
Input Current vs. Load Current for 3000 Version

R_{FB1} = 100kΩ, R_{FB2} = 19.1kΩ, DCR = 22.1mΩ



Efficiency vs. Load Current for 3000 Version

R_{FB1} = 100kΩ, R_{FB2} = 19.1kΩ, DCR = 22.1mΩ

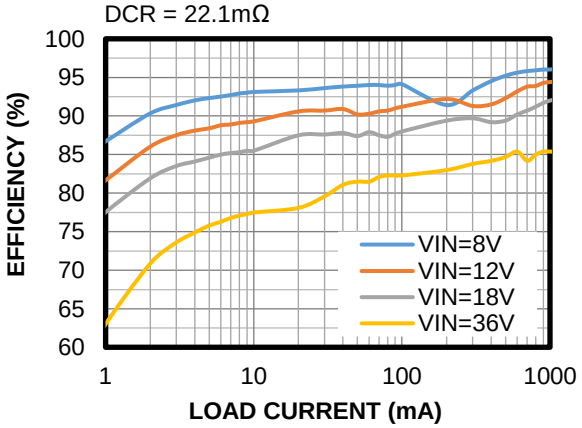


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

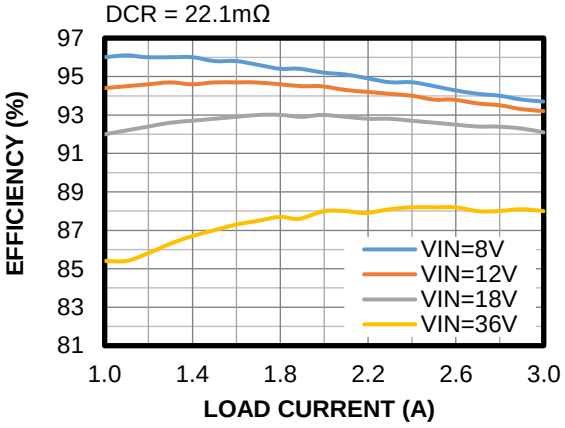
Efficiency vs. Load Current for 3000 Version

DCR = 22.1mΩ



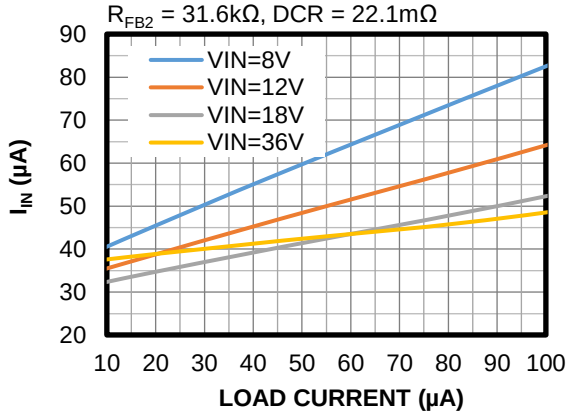
Efficiency vs. Load Current for 3000 Version

DCR = 22.1mΩ



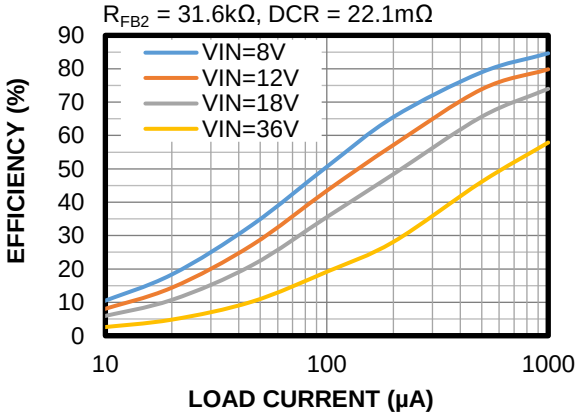
Input Current vs. Load Current for 3000 Version

V_{OUT} = 3.3V, R_{FB1} = 100kΩ,
R_{FB2} = 31.6kΩ, DCR = 22.1mΩ



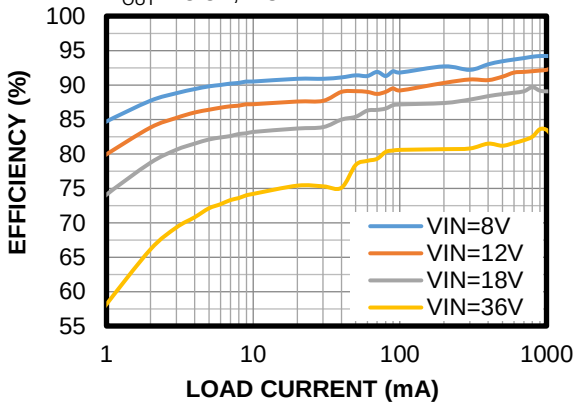
Efficiency vs. Load Current for 3000 Version

V_{OUT} = 3.3V, R_{FB1} = 100kΩ,
R_{FB2} = 31.6kΩ, DCR = 22.1mΩ



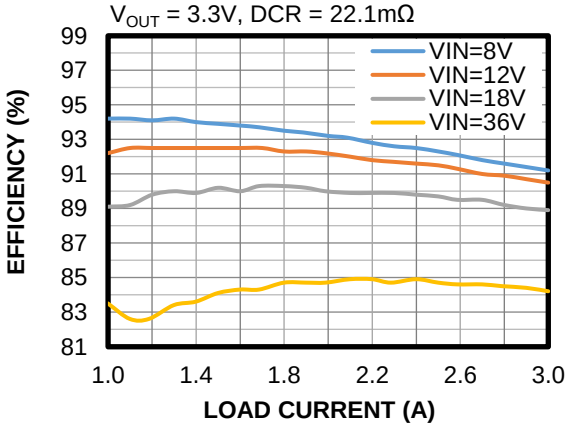
Efficiency vs. Load Current for 3000 Version

V_{OUT} = 3.3V, DCR = 22.1mΩ



Efficiency vs. Load Current for 3000 Version

V_{OUT} = 3.3V, DCR = 22.1mΩ

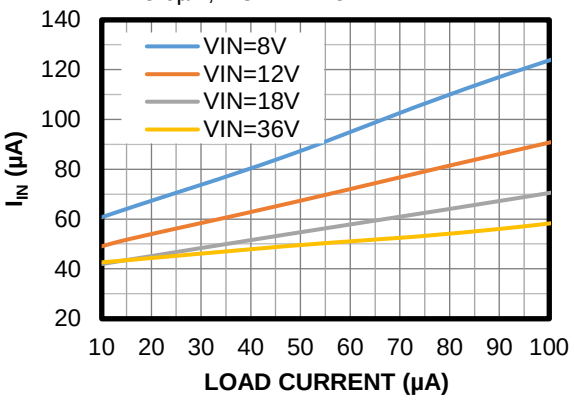


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

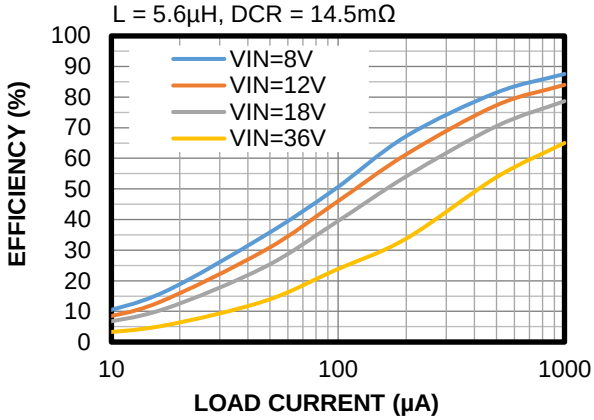
Input Current vs. Load Current for 3000 Version

f_{SW} = 415kHz, R_{FB1} = 100kΩ, R_{FB2} = 19.1kΩ, L = 5.6µH, DCR = 14.5mΩ



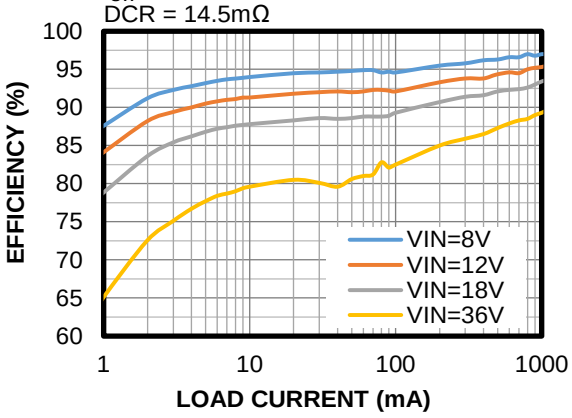
Efficiency vs. Load Current for 3000 Version

f_{SW} = 415kHz, R_{FB1} = 100kΩ, R_{FB2} = 19.1kΩ, L = 5.6µH, DCR = 14.5mΩ



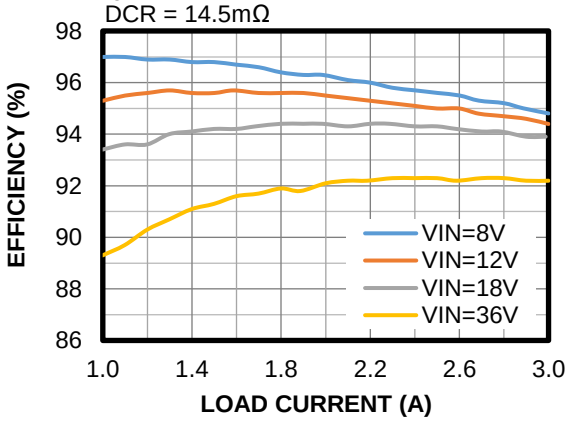
Efficiency vs. Load Current for 3000 Version

f_{SW} = 415kHz, L = 5.6µH, DCR = 14.5mΩ



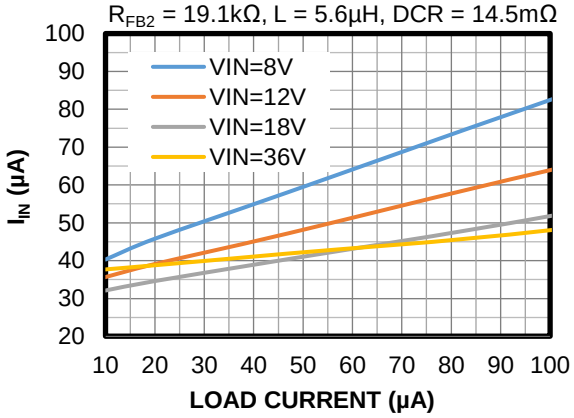
Efficiency vs. Load Current for 3000 Version

f_{SW} = 415kHz, L = 5.6µH, DCR = 14.5mΩ



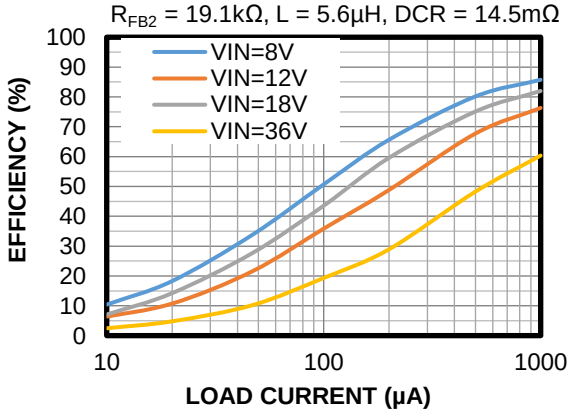
Input Current vs. Load Current for 3000 Version

V_{OUT} = 3.3V, f_{SW} = 415kHz, R_{FB1} = 100kΩ, R_{FB2} = 19.1kΩ, L = 5.6µH, DCR = 14.5mΩ



Efficiency vs. Load Current for 3000 Version

V_{OUT} = 3.3V, f_{SW} = 415kHz, R_{FB1} = 100kΩ, R_{FB2} = 19.1kΩ, L = 5.6µH, DCR = 14.5mΩ

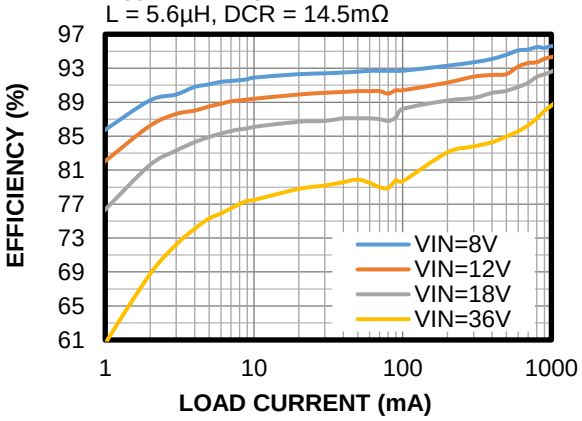


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

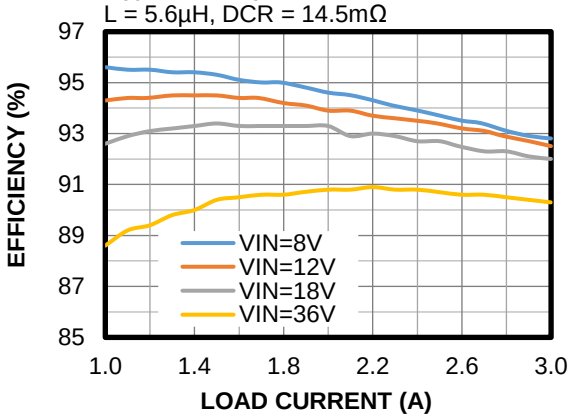
Efficiency vs. Load Current for 3000 Version

V_{OUT} = 3.3V, f_{SW} = 415kHz, L = 5.6µH, DCR = 14.5mΩ



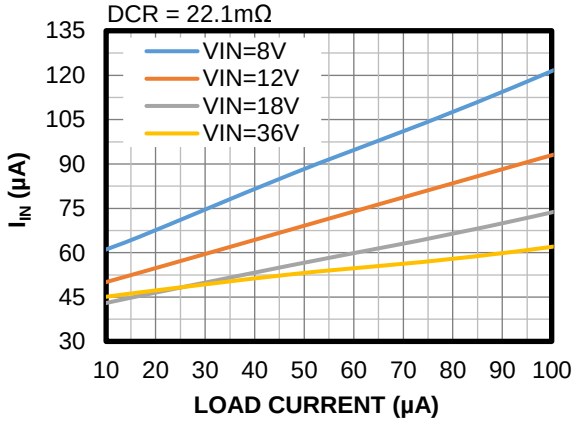
Efficiency vs. Load Current for 3000 Version

V_{OUT} = 3.3V, f_{SW} = 415kHz, L = 5.6µH, DCR = 14.5mΩ



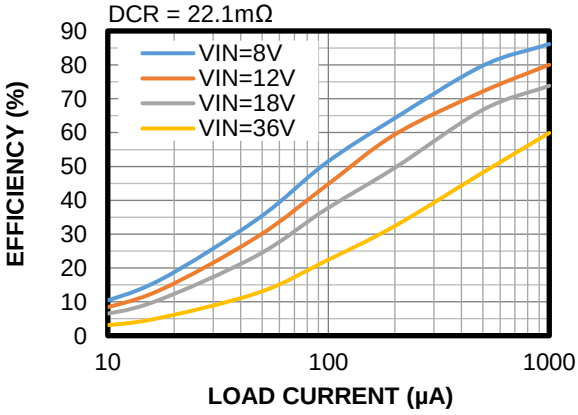
Input Current vs. Load Current for 2000 Version

R_{FB1} = 100kΩ, R_{FB2} = 19.1kΩ, DCR = 22.1mΩ



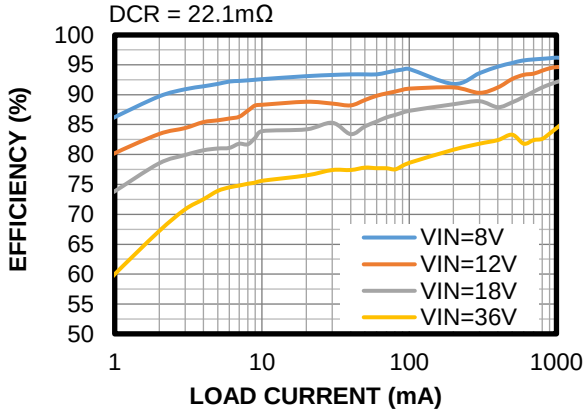
Efficiency vs. Load Current for 2000 Version

R_{FB1} = 100kΩ, R_{FB2} = 19.1kΩ, DCR = 22.1mΩ



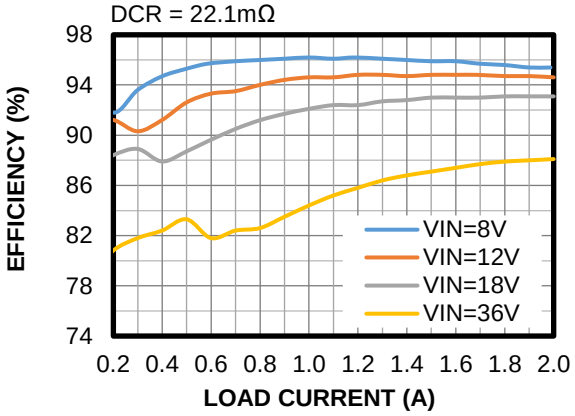
Efficiency vs. Load Current for 2000 Version

DCR = 22.1mΩ



Efficiency vs. Load Current for 2000 Version

DCR = 22.1mΩ

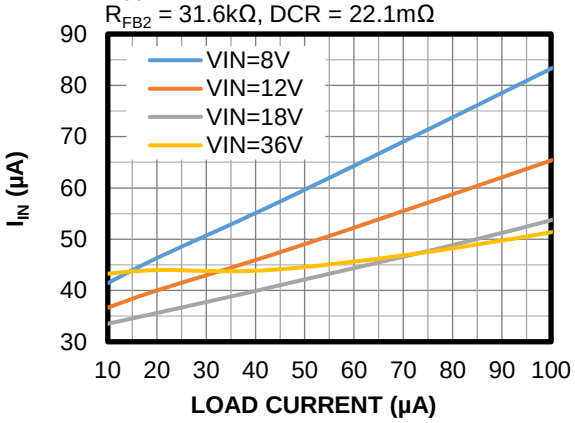


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

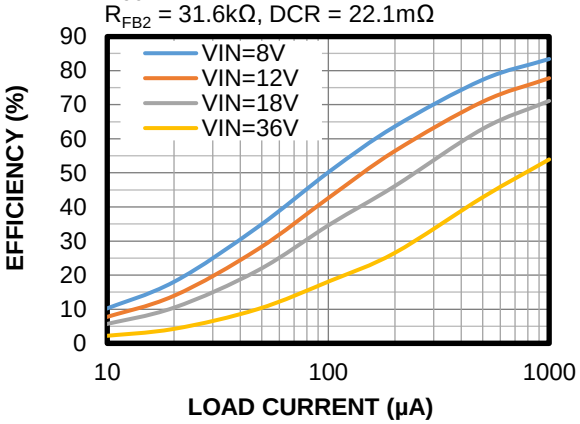
Input Current vs. Load Current for 2000 Version

V_{OUT} = 3.3V, R_{FB1} = 100kΩ, R_{FB2} = 31.6kΩ, DCR = 22.1mΩ



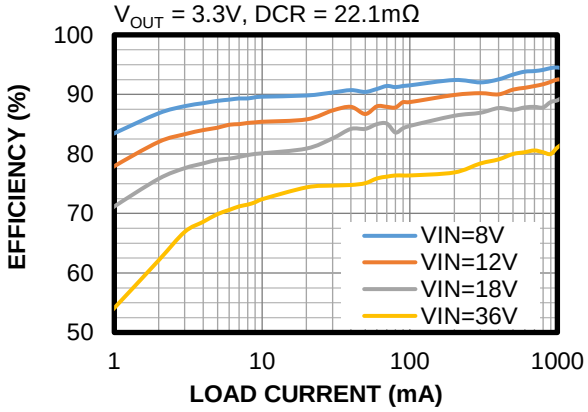
Efficiency vs. Load Current for 2000 Version

V_{OUT} = 3.3V, R_{FB1} = 100kΩ, R_{FB2} = 31.6kΩ, DCR = 22.1mΩ



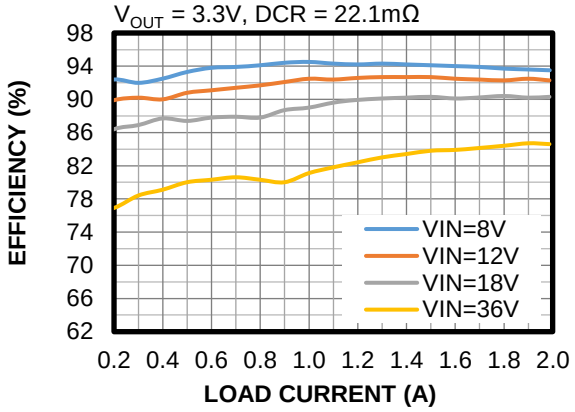
Efficiency vs. Load Current for 2000 Version

V_{OUT} = 3.3V, DCR = 22.1mΩ



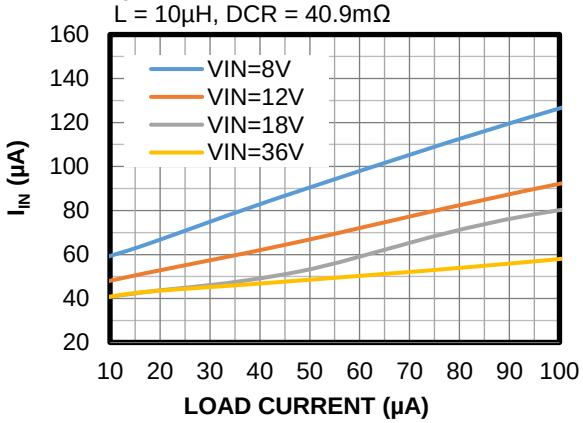
Efficiency vs. Load Current for 2000 Version

V_{OUT} = 3.3V, DCR = 22.1mΩ



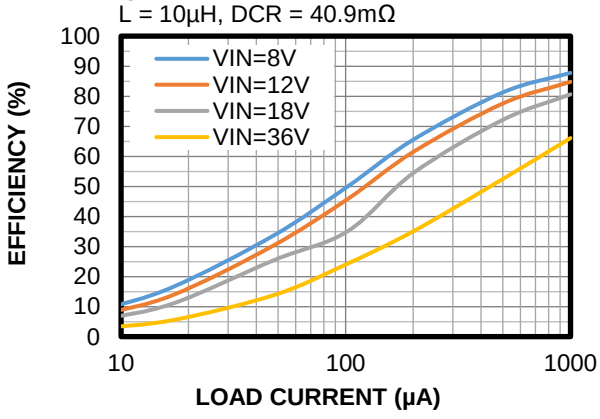
Input Current vs. Load Current for 2000 Version

f_{SW} = 415kHz, R_{FB1} = 100kΩ, R_{FB2} = 19.1kΩ, L = 10µH, DCR = 40.9mΩ



Efficiency vs. Load Current for 2000 Version

f_{SW} = 415kHz, R_{FB1} = 100kΩ, R_{FB2} = 19.1kΩ, L = 10µH, DCR = 40.9mΩ

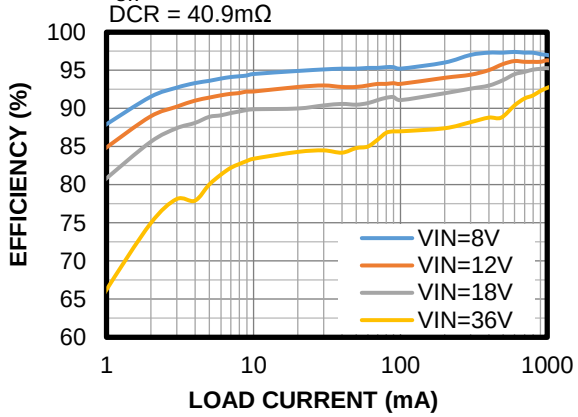


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

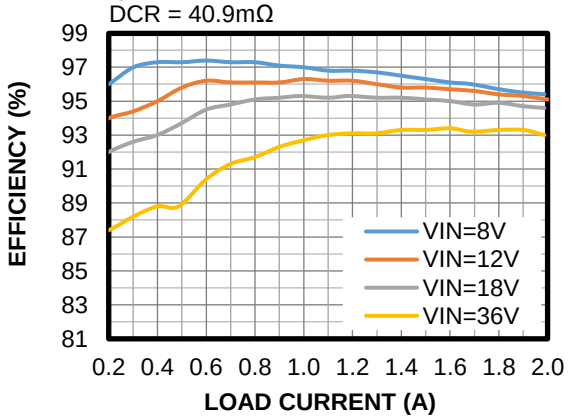
Efficiency vs. Load Current for 2000 Version

f_{SW} = 415kHz, L = 10µH, DCR = 40.9mΩ



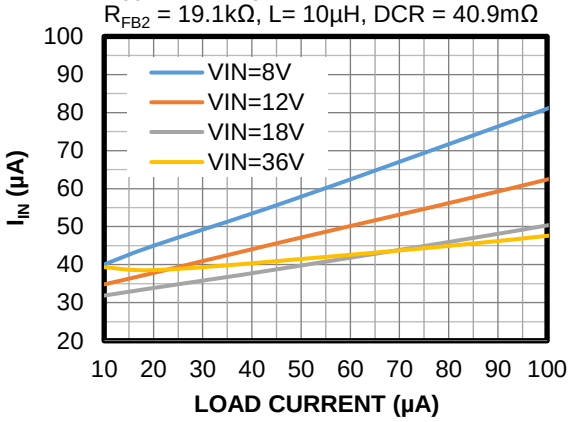
Efficiency vs. Load Current for 2000 Version

f_{SW} = 415kHz, L = 10µH, DCR = 40.9mΩ



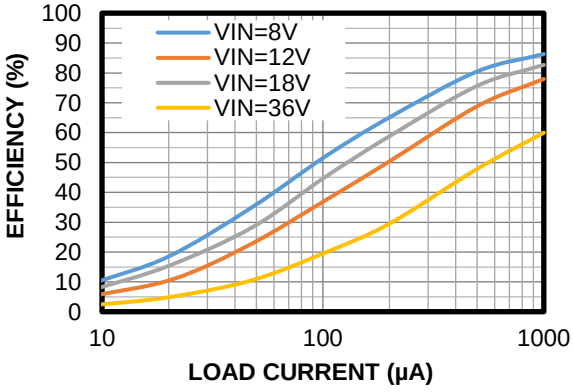
Input Current vs. Load Current for 2000 Version

V_{OUT} = 3.3V, f_{SW} = 415kHz, R_{FB1} = 100kΩ, R_{FB2} = 19.1kΩ, L= 10µH, DCR = 40.9mΩ



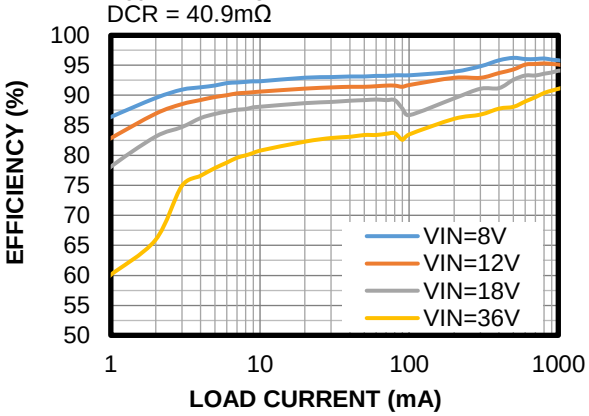
Efficiency vs. Load Current for 2000 Version

V_{OUT} = 3.3V, f_{SW} = 415kHz, R_{FB1} = 100kΩ, R_{FB2} = 19.1kΩ, L = 10µH, DCR = 40.9mΩ



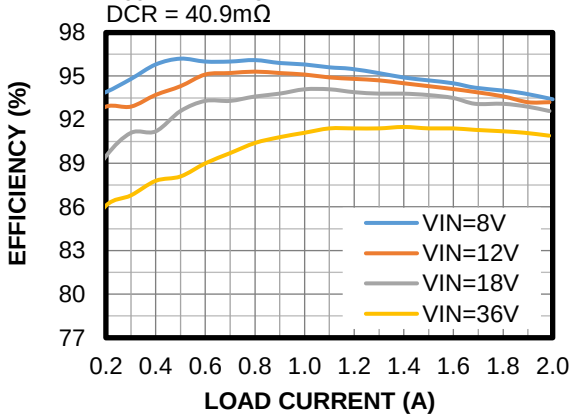
Efficiency vs. Load Current for 2000 Version

V_{OUT} = 3.3V, f_{SW} = 415kHz, L = 10µH, DCR = 40.9mΩ



Efficiency vs. Load Current for 2000 Version

V_{OUT} = 3.3V, f_{SW} = 415kHz, L = 10µH, DCR = 40.9mΩ

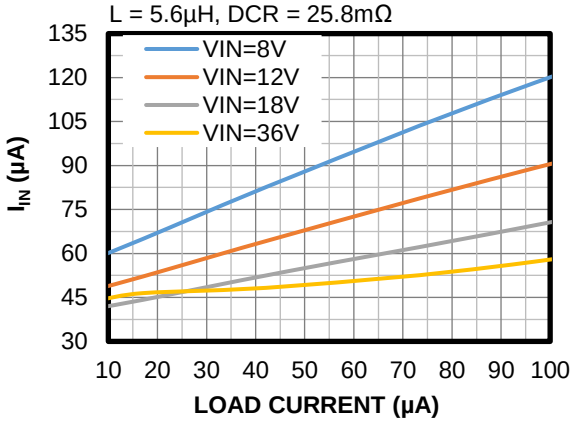


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

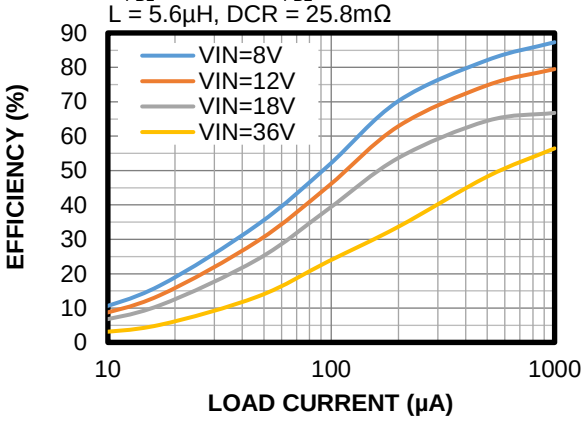
Input Current vs. Load Current for 1000/0000 Versions

R_{FB1} = 100kΩ, R_{FB2} = 19.1kΩ, L = 5.6µH, DCR = 25.8mΩ



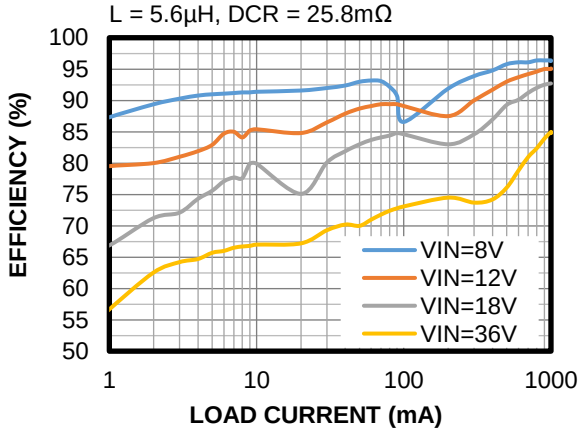
Efficiency vs. Load Current for 1000/0000 Versions

R_{FB1} = 100kΩ, R_{FB2} = 19.1kΩ, L = 5.6µH, DCR = 25.8mΩ



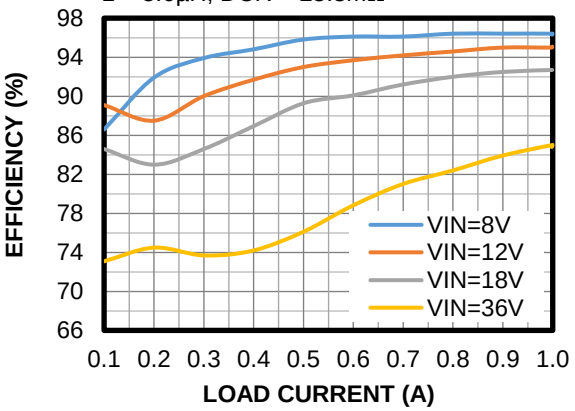
Efficiency vs. Load Current for 1000/0000 Versions

L = 5.6µH, DCR = 25.8mΩ



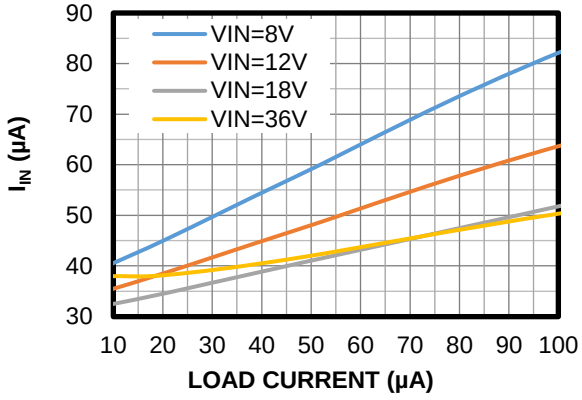
Efficiency vs. Load Current for 1000/0000 Versions

L = 5.6µH, DCR = 25.8mΩ



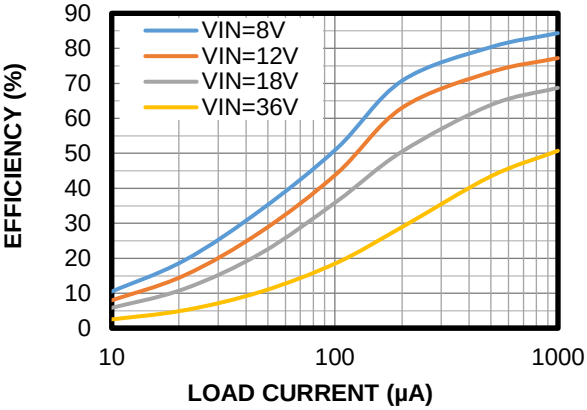
Input Current vs. Load Current for 1000/0000 Versions

V_{OUT} = 3.3V, R_{FB1} = 100kΩ, R_{FB2} = 31.6kΩ, L = 5.6µH, DCR = 25.8mΩ



Efficiency vs. Load Current for 1000/0000 Versions

V_{OUT} = 3.3V, R_{FB1} = 100kΩ, R_{FB2} = 31.6kΩ, L = 5.6µH, DCR = 25.8mΩ

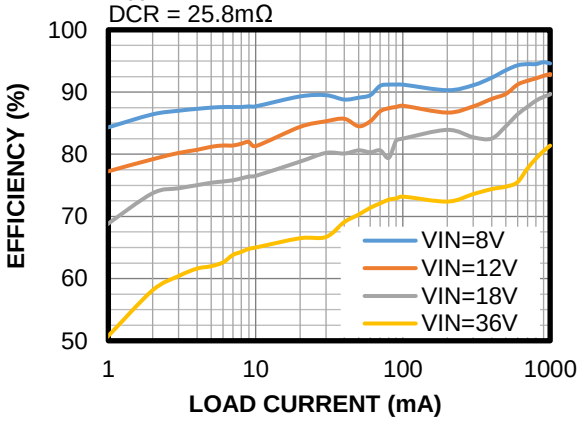


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

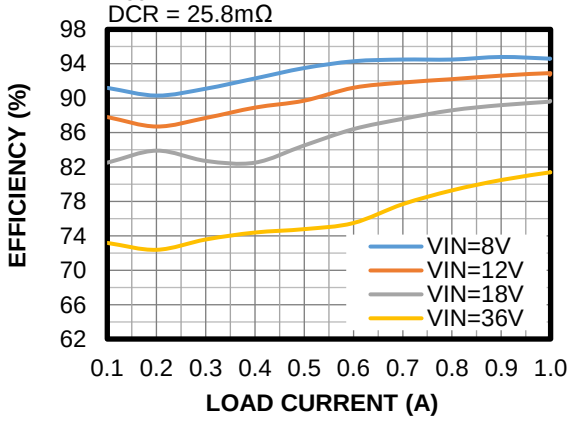
Efficiency vs. Load Current for 1000/0000 Versions

V_{OUT} = 3.3V, L = 5.6µH, DCR = 25.8mΩ



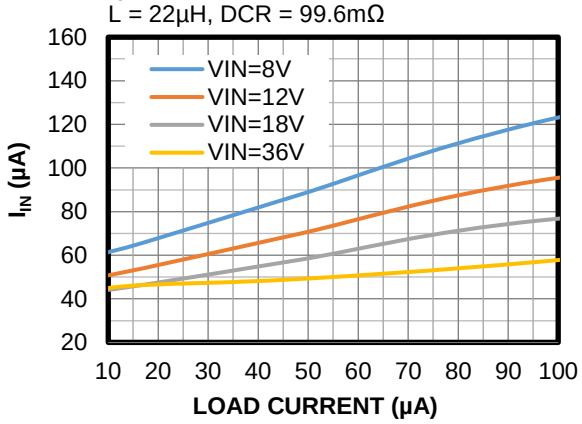
Efficiency vs. Load Current for 1000/0000 Versions

V_{OUT} = 3.3V, L = 5.6µH, DCR = 25.8mΩ



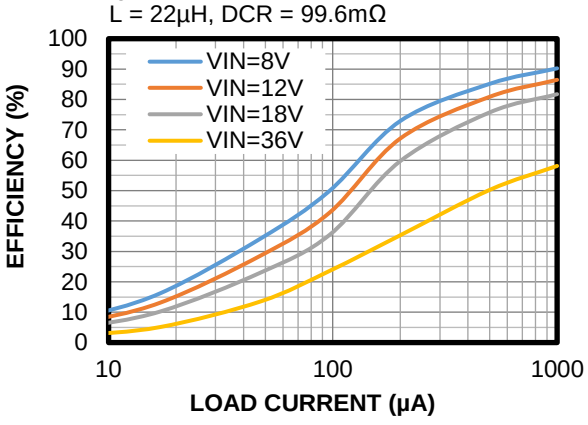
Input Current vs. Load Current for 1000/0000 Versions

f_{SW} = 415kHz, R_{FB1} = 100kΩ, R_{FB2} = 19.1kΩ, L = 22µH, DCR = 99.6mΩ



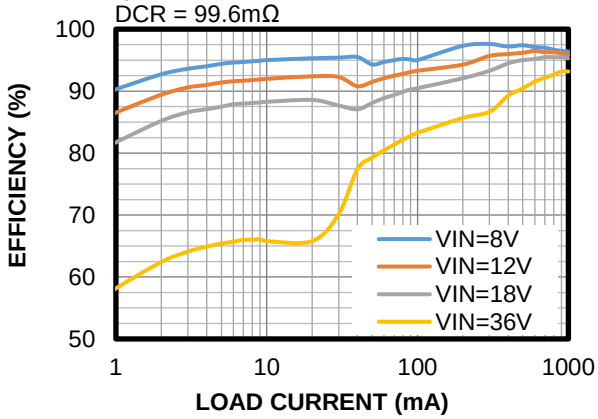
Efficiency vs. Load Current for 1000/0000 Versions

f_{SW} = 415kHz, R_{FB1} = 100kΩ, R_{FB2} = 19.1kΩ, L = 22µH, DCR = 99.6mΩ



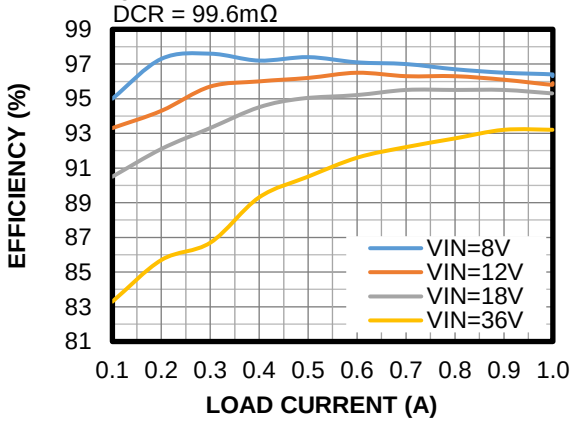
Efficiency vs. Load Current for 1000/0000 Versions

f_{SW} = 415kHz, L = 22µH, DCR = 99.6mΩ



Efficiency vs. Load Current for 1000/0000 Versions

f_{SW} = 415kHz, L = 22µH, DCR = 99.6mΩ

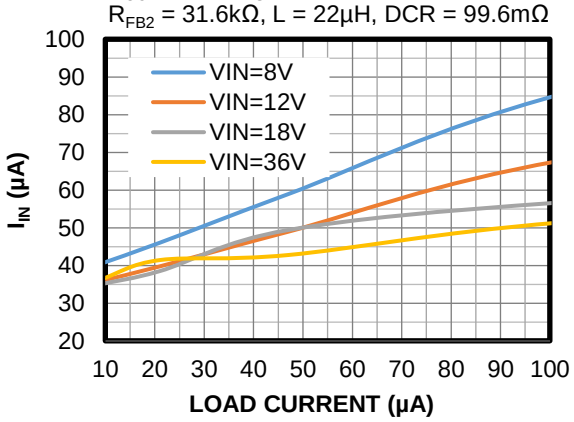


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

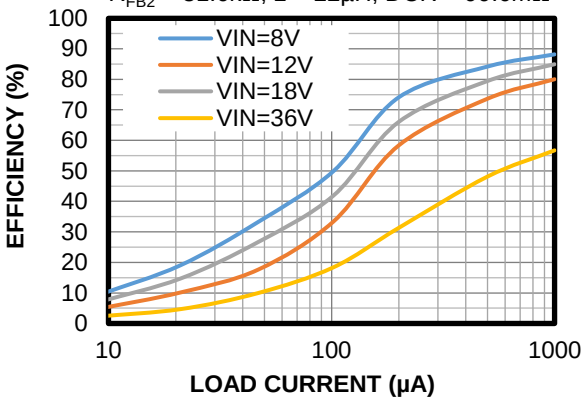
Input Current vs. Load Current for 1000/0000 Versions

V_{OUT} = 3.3V, f_{SW} = 415kHz, R_{FB1} = 100kΩ, R_{FB2} = 31.6kΩ, L = 22µH, DCR = 99.6mΩ



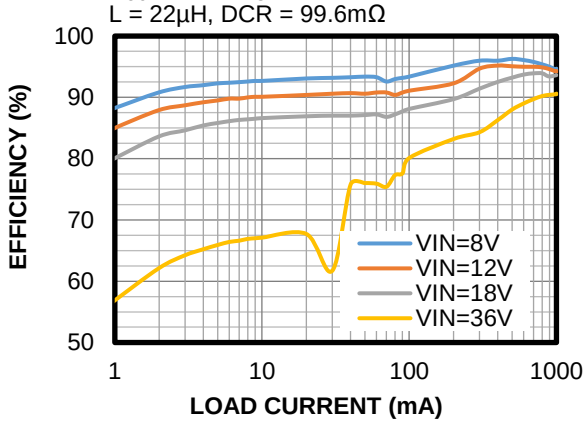
Efficiency vs. Load Current for 1000/0000 Versions

V_{OUT} = 3.3V, f_{SW} = 415kHz, R_{FB1} = 100kΩ, R_{FB2} = 31.6kΩ, L = 22µH, DCR = 99.6mΩ



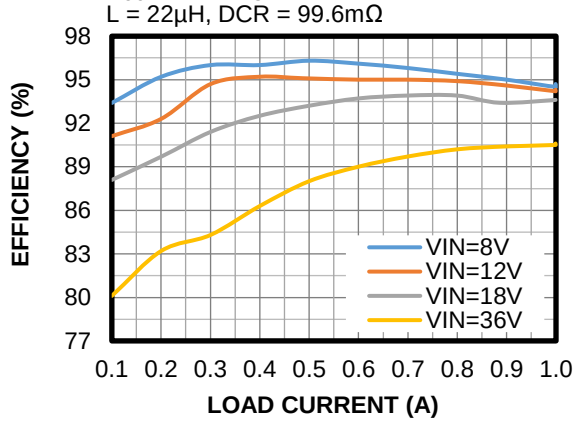
Efficiency vs. Load Current for 1000/0000 Versions

V_{OUT} = 3.3V, f_{SW} = 415kHz, L = 22µH, DCR = 99.6mΩ



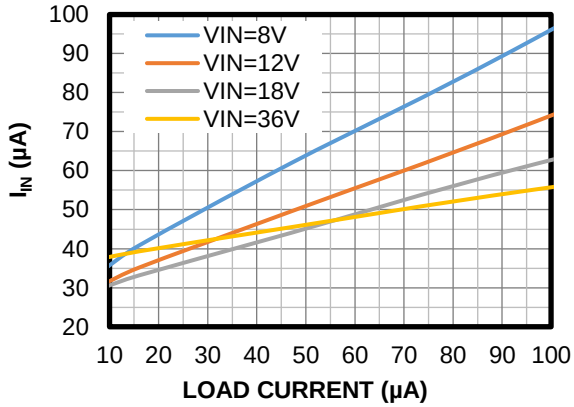
Efficiency vs. Load Current for 1000/0000 Versions

V_{OUT} = 3.3V, f_{SW} = 415kHz, L = 22µH, DCR = 99.6mΩ



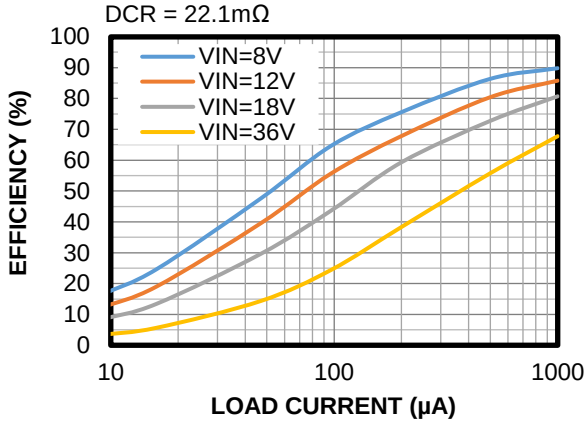
Input Current vs. Load Current for 4500/3500 Versions

DCR = 22.1mΩ



Efficiency vs. Load Current for 4500/3500 Versions

DCR = 22.1mΩ

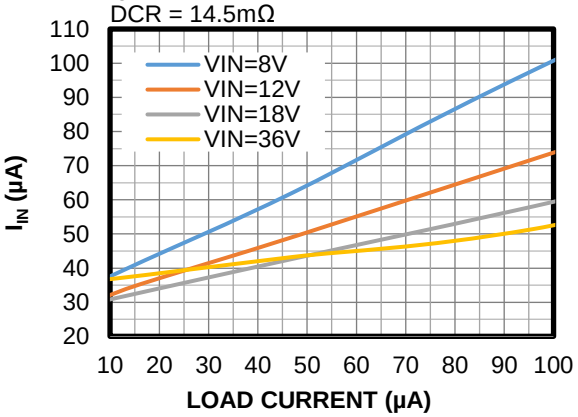


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

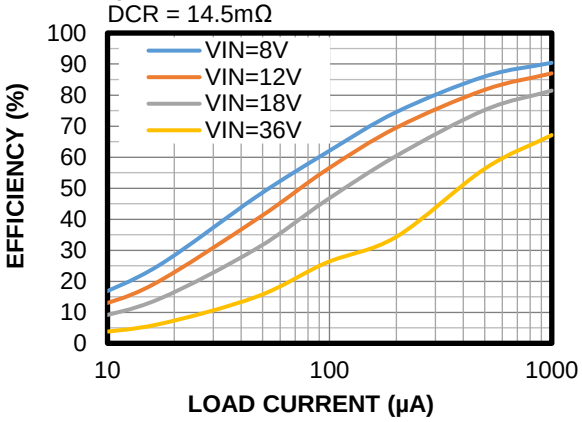
Input Current vs. Load Current for 4500/3500 Versions

f_{SW} = 415kHz, L = 5.6µH, DCR = 14.5mΩ



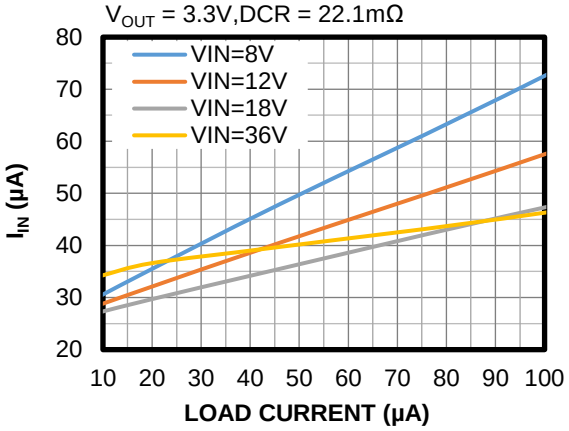
Efficiency vs. Load Current for 4500/3500 Versions

f_{SW} = 415kHz, L = 5.6µH, DCR = 14.5mΩ



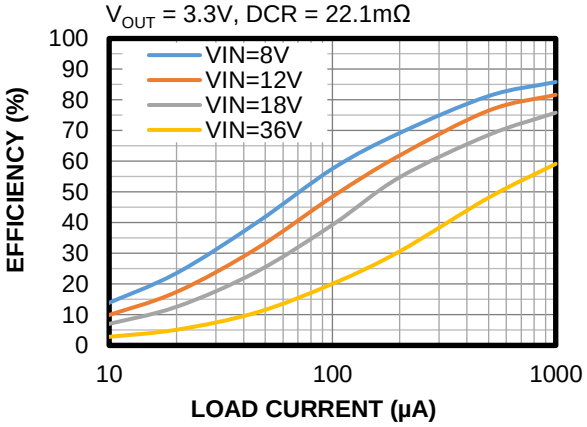
Input Current vs. Load Current for 4330/3330 Versions

V_{OUT} = 3.3V,DCR = 22.1mΩ



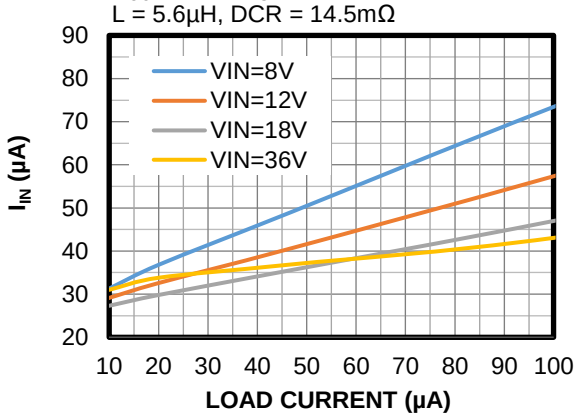
Efficiency vs. Load Current for 4330/3330 Versions

V_{OUT} = 3.3V, DCR = 22.1mΩ



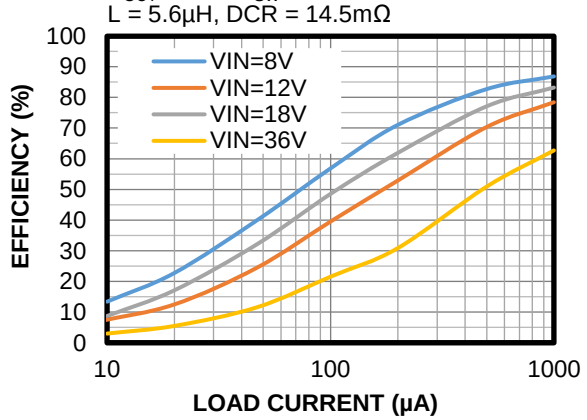
Input Current vs. Load Current for 4330/3330 Versions

V_{OUT} = 3.3V, f_{SW} = 415kHz, L = 5.6µH, DCR = 14.5mΩ



Efficiency vs. Load Current for 4330/3330 Versions

V_{OUT} = 3.3V, f_{SW} = 415kHz, L = 5.6µH, DCR = 14.5mΩ

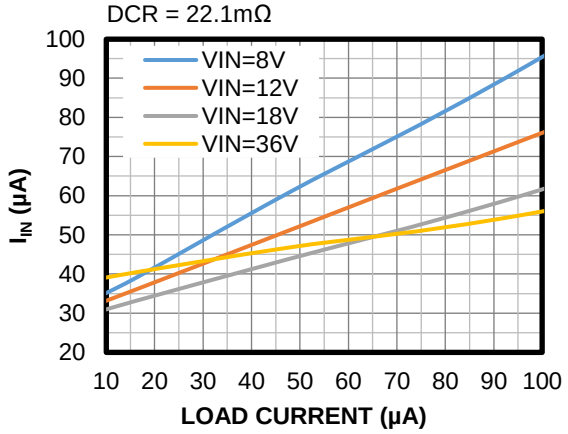


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

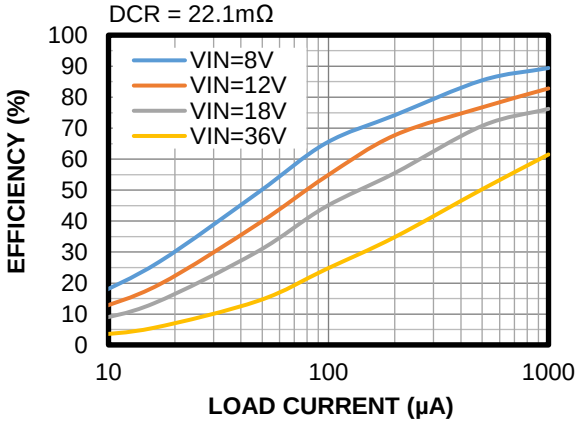
Input Current vs. Load Current for 2500 Version

DCR = 22.1mΩ



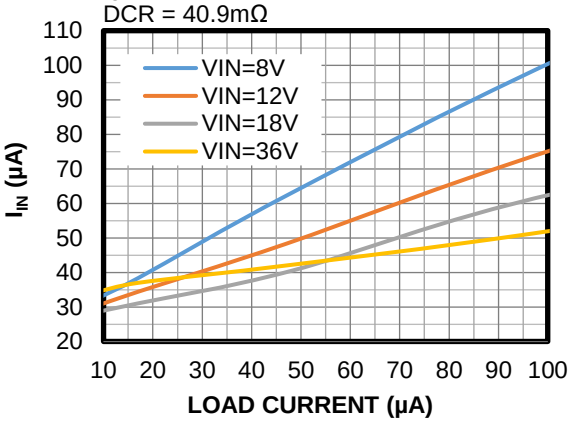
Efficiency vs. Load Current for 2500 Version

DCR = 22.1mΩ



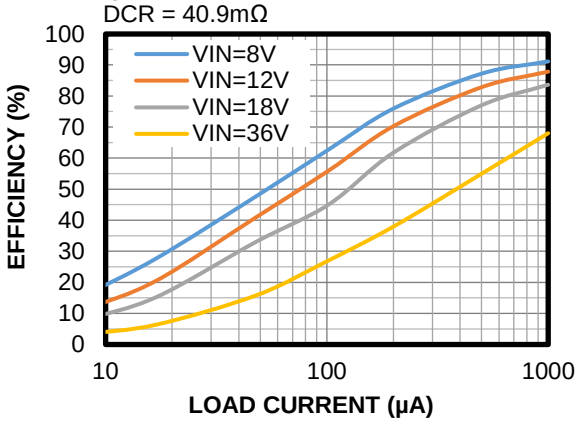
Input Current vs. Load Current for 2500 Version

f_{SW} = 415kHz, L = 10µH,
DCR = 40.9mΩ



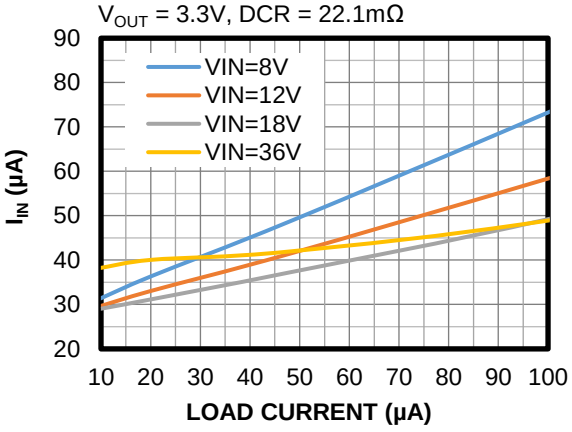
Efficiency vs. Load Current for 2500 Version

f_{SW} = 415kHz, L = 10µH,
DCR = 40.9mΩ



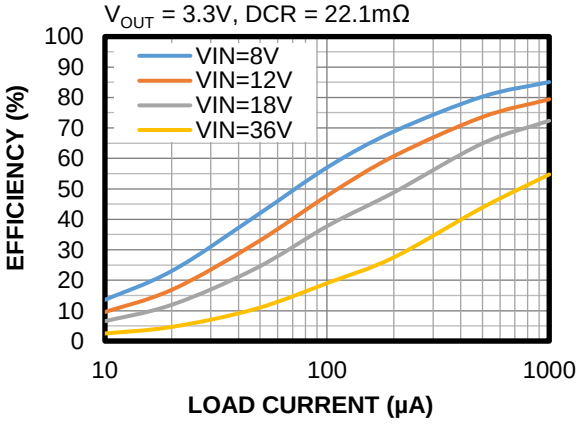
Input Current vs. Load Current for 2330 Version

V_{OUT} = 3.3V, DCR = 22.1mΩ



Efficiency vs. Load Current for 2330 Version

V_{OUT} = 3.3V, DCR = 22.1mΩ

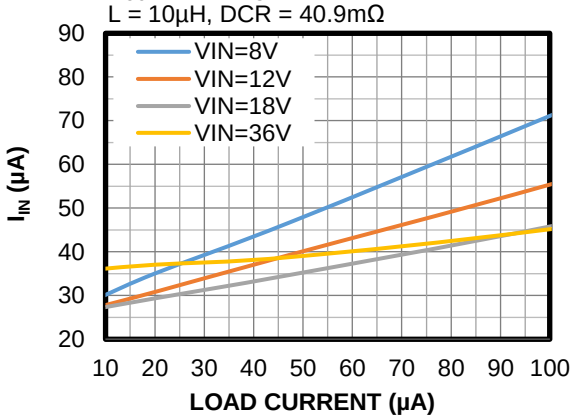


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

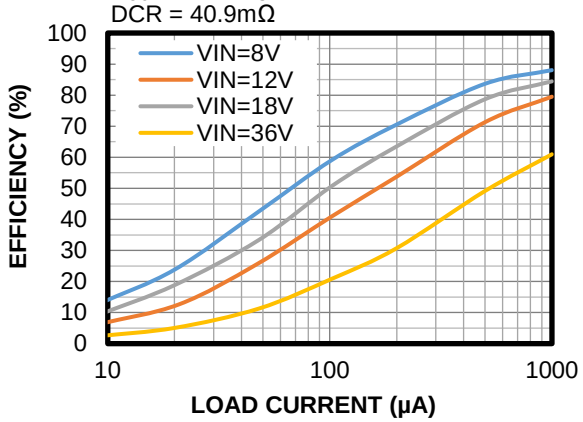
Input Current vs. Load Current for 2330 Version

V_{OUT} = 3.3V, f_{SW} = 415kHz, L = 10µH, DCR = 40.9mΩ



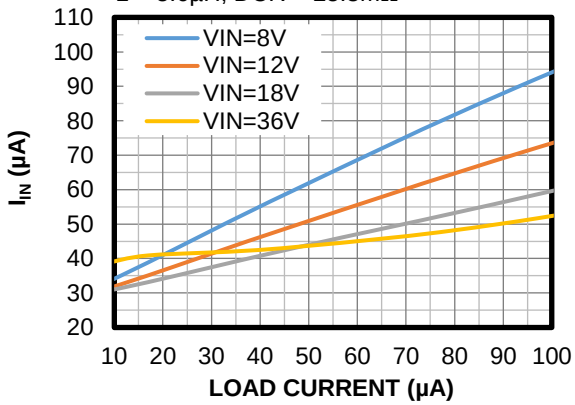
Efficiency vs. Load Current for 2330 Version

V_{OUT} = 3.3V, f_{SW} = 415kHz, L = 10µH, DCR = 40.9mΩ



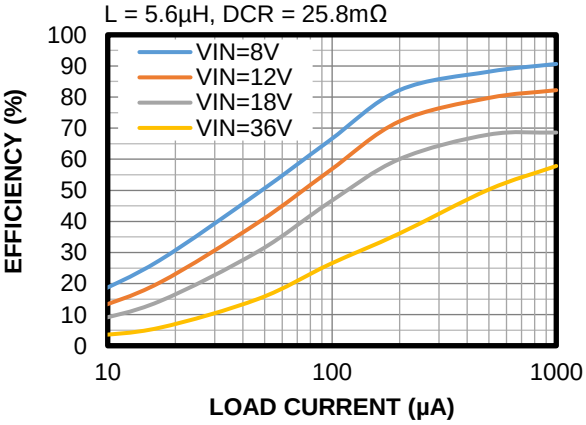
Input Current vs. Load Current for 1500/0500 Versions

L = 5.6µH, DCR = 25.8mΩ



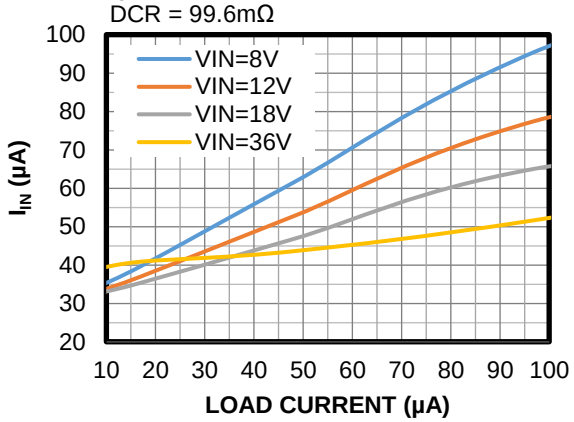
Efficiency vs. Load Current for 1500/0500 Versions

L = 5.6µH, DCR = 25.8mΩ



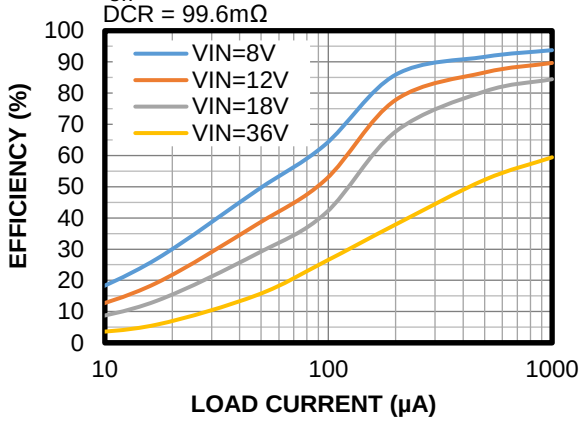
Input Current vs. Load Current for 1500/0500 Versions

f_{SW} = 415kHz, L = 22µH, DCR = 99.6mΩ



Efficiency vs. Load Current for 1500/0500 Versions

f_{SW} = 415kHz, L = 22µH, DCR = 99.6mΩ

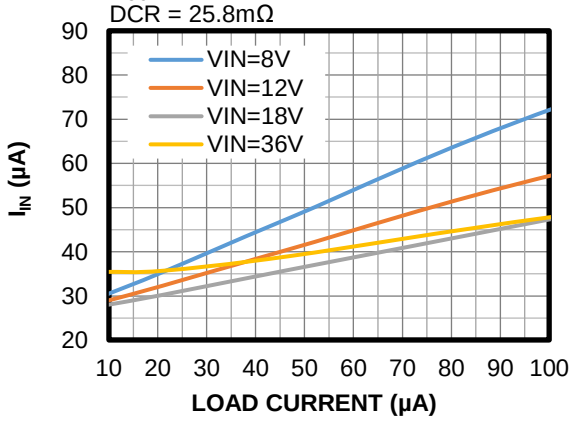


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

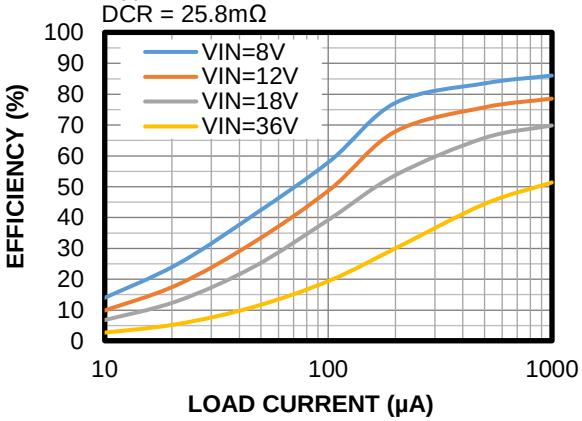
Input Current vs. Load Current for 1330/0330 Versions

V_{OUT} = 3.3V, L = 5.6µH, DCR = 25.8mΩ



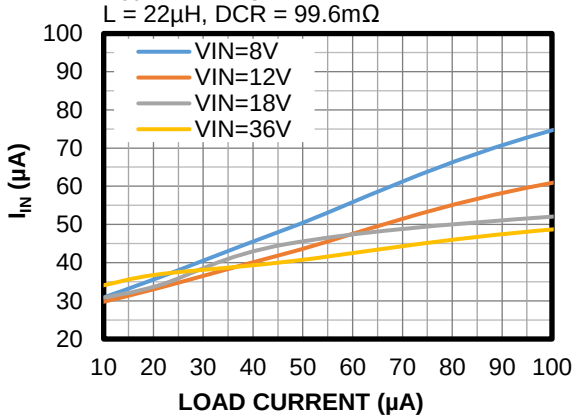
Efficiency vs. Load Current for 1330/0330 Versions

V_{OUT} = 3.3V, L = 5.6µH, DCR = 25.8mΩ



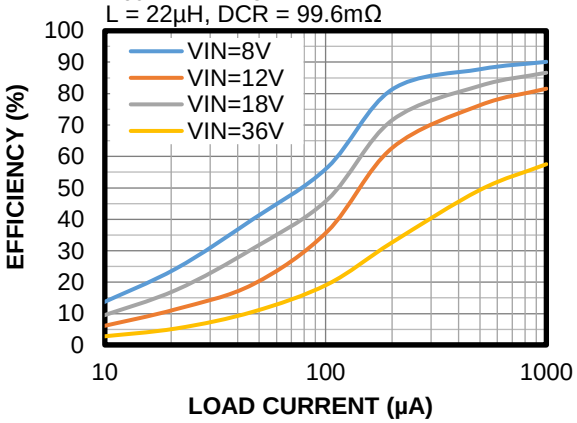
Input Current vs. Load Current for 1330/0330 Versions

V_{OUT} = 3.3V, f_{SW} = 415kHz, L = 22µH, DCR = 99.6mΩ



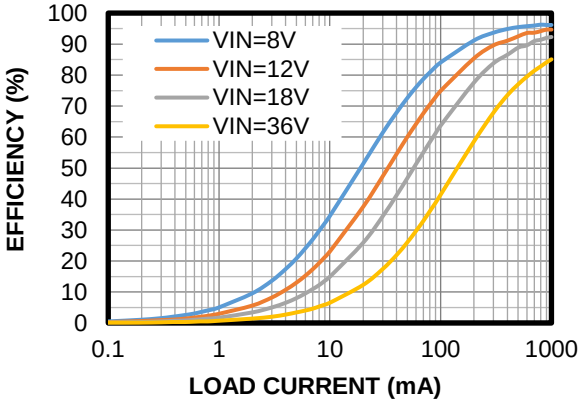
Efficiency vs. Load Current for 1330/0330 Versions

V_{OUT} = 3.3V, f_{SW} = 415kHz, L = 22µH, DCR = 99.6mΩ



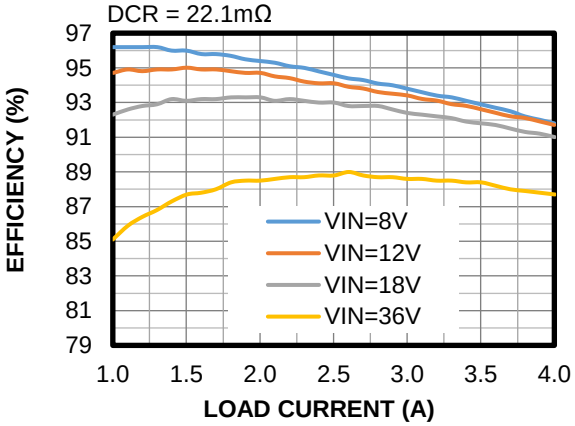
Efficiency vs. Load Current for 4006/3006 Versions

DCR = 22.1mΩ



Efficiency vs. Load Current for 4006/3006 Versions

DCR = 22.1mΩ

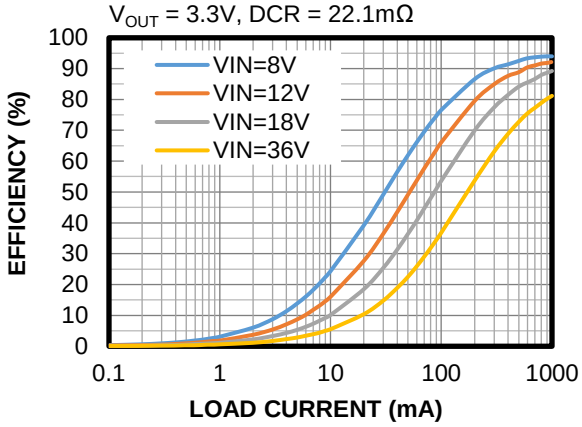


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

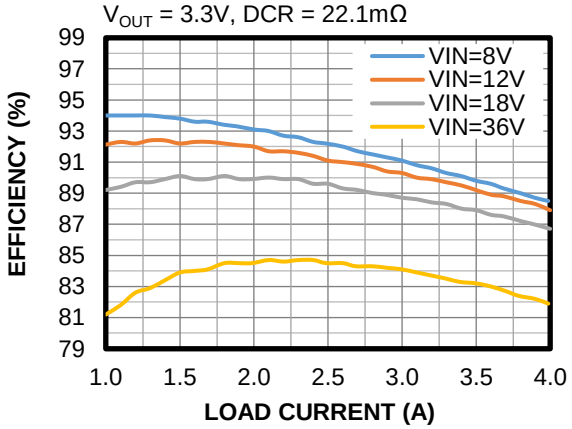
Efficiency vs. Load Current for 4006/3006 Versions

V_{OUT} = 3.3V, DCR = 22.1mΩ



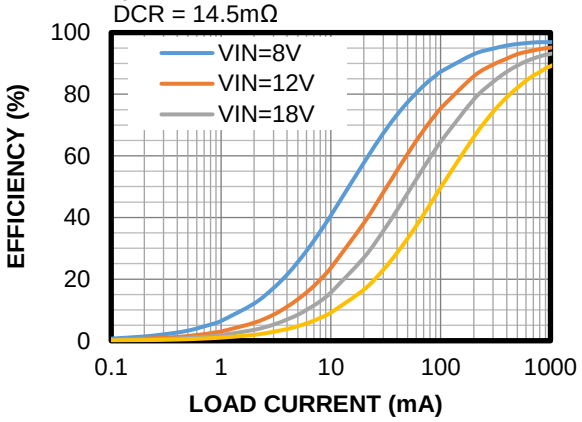
Efficiency vs. Load Current for 4006/3006 Versions

V_{OUT} = 3.3V, DCR = 22.1mΩ



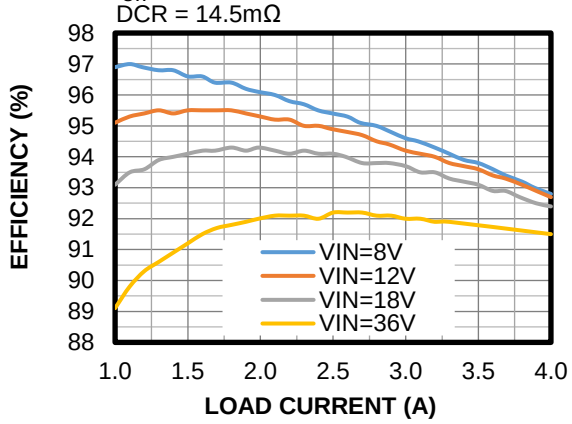
Efficiency vs. Load Current for 4006/3006 Versions

f_{SW} = 415kHz, L = 5.6µH, DCR = 14.5mΩ



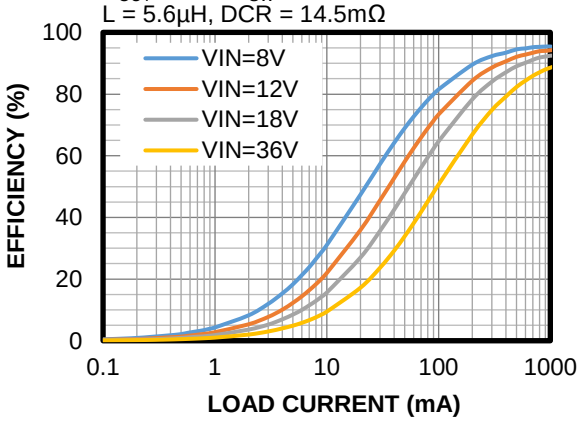
Efficiency vs. Load Current for 4006/3006 Versions

f_{SW} = 415kHz, L = 5.6µH, DCR = 14.5mΩ



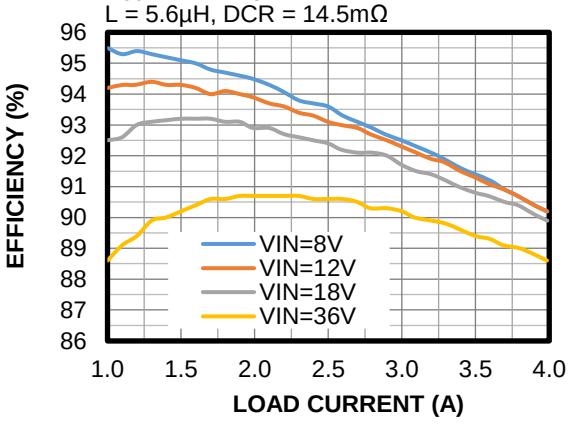
Efficiency vs. Load Current for 4006/3006 Versions

V_{OUT} = 3.3V, f_{SW} = 415kHz, L = 5.6µH, DCR = 14.5mΩ



Efficiency vs. Load Current for 4006/3006 Versions

V_{OUT} = 3.3V, f_{SW} = 415kHz, L = 5.6µH, DCR = 14.5mΩ

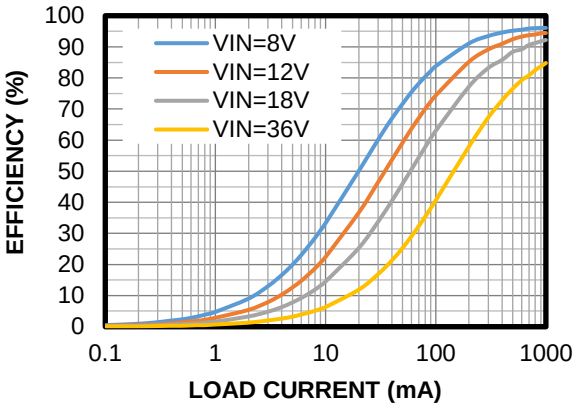


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

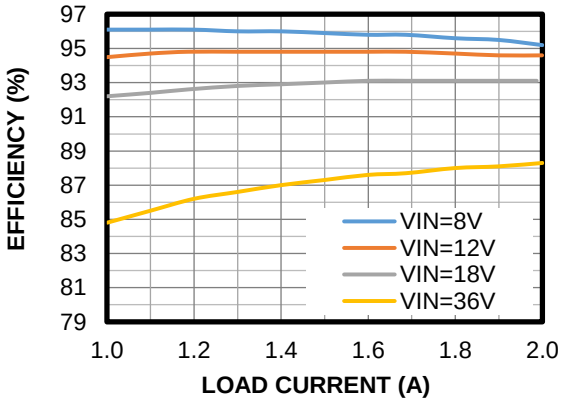
Efficiency vs. Load Current for 2006 Version

DCR = 22.1mΩ



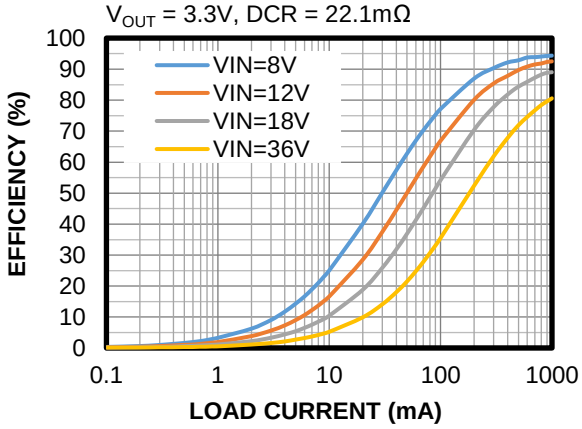
Efficiency vs. Load Current for 2006 Version

DCR = 22.1mΩ



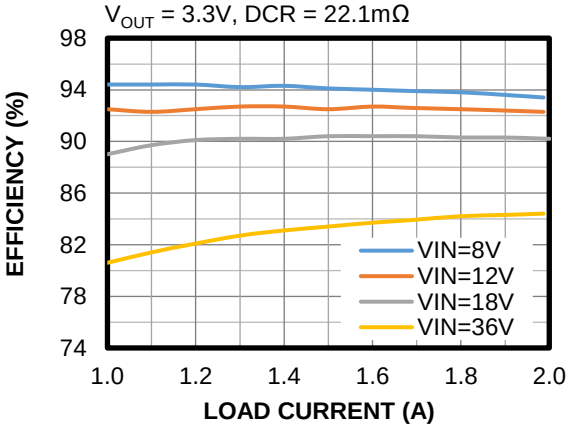
Efficiency vs. Load Current for 2006 Version

V_{OUT} = 3.3V, DCR = 22.1mΩ



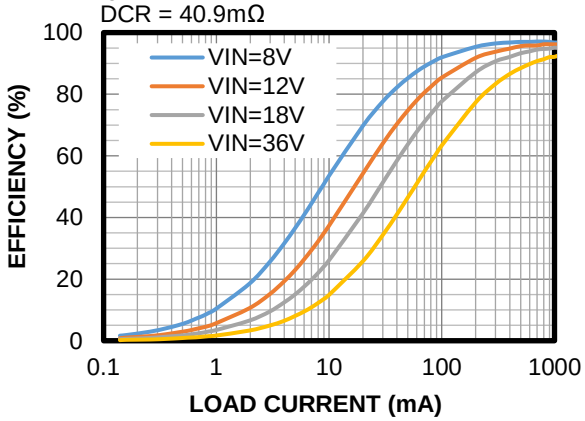
Efficiency vs. Load Current for 2006 Version

V_{OUT} = 3.3V, DCR = 22.1mΩ



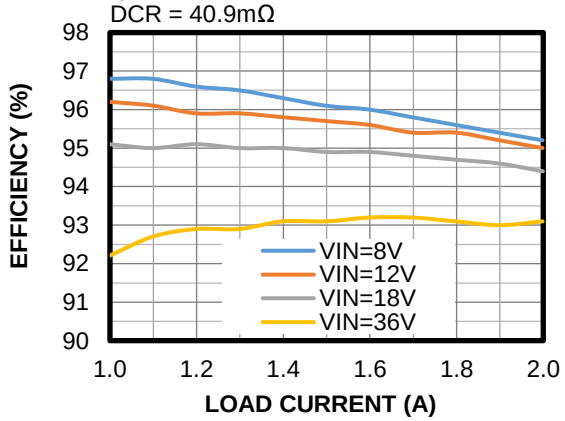
Efficiency vs. Load Current for 2006 Version

f_{SW} = 415kHz, L = 10µH,
DCR = 40.9mΩ



Efficiency vs. Load Current for 2006 Version

f_{SW} = 415kHz, L = 10µH,
DCR = 40.9mΩ

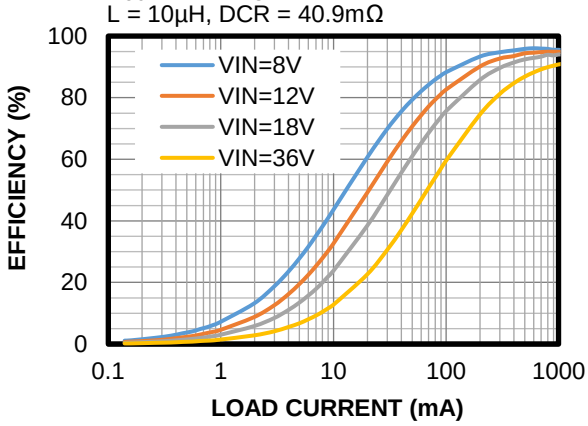


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

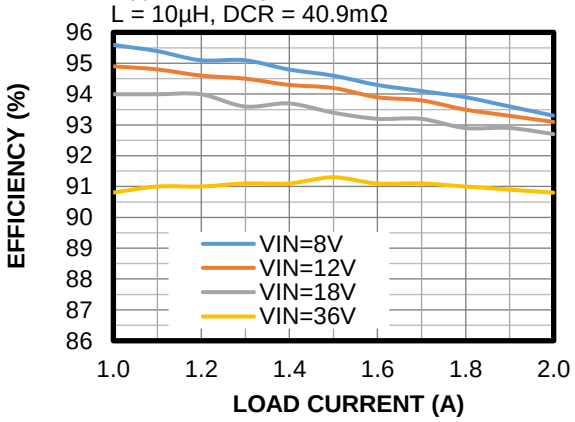
Efficiency vs. Load Current for 2006 Version

V_{OUT} = 3.3V, f_{SW} = 415kHz, L = 10µH, DCR = 40.9mΩ



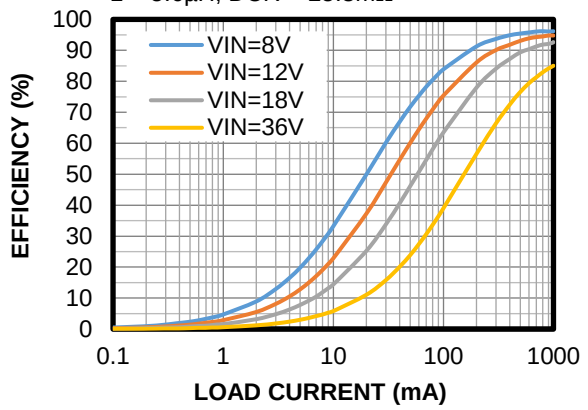
Efficiency vs. Load Current for 2006 Version

V_{OUT} = 3.3V, f_{SW} = 415kHz, L = 10µH, DCR = 40.9mΩ



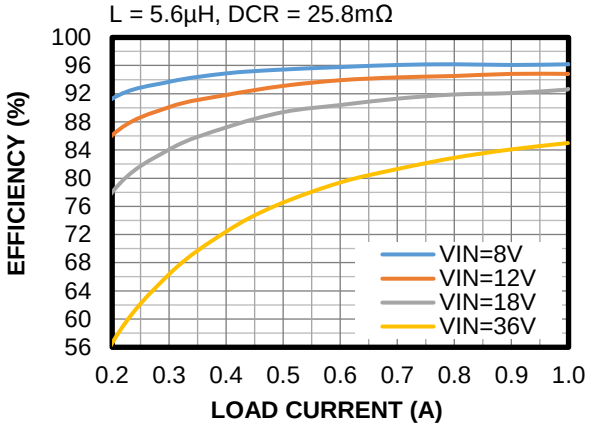
Efficiency vs. Load Current for 1006/0006 Versions

L = 5.6µH, DCR = 25.8mΩ



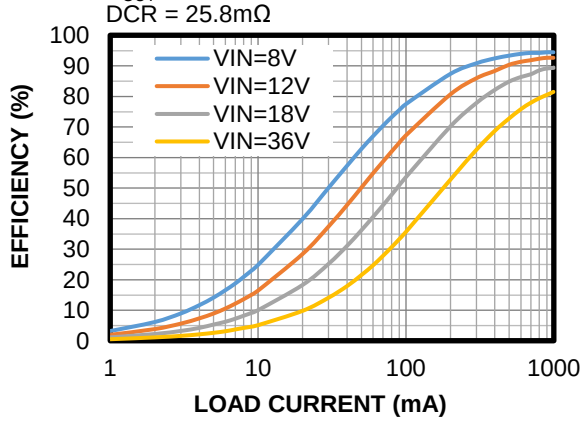
Efficiency vs. Load Current for 1006/0006 Versions

L = 5.6µH, DCR = 25.8mΩ



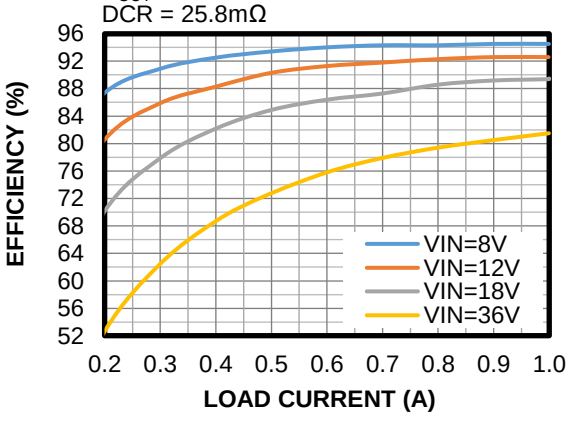
Efficiency vs. Load Current for 1006/0006 Versions

V_{OUT} = 3.3V, L = 5.6µH, DCR = 25.8mΩ



Efficiency vs. Load Current for 1006/0006 Versions

V_{OUT} = 3.3V, L = 5.6µH, DCR = 25.8mΩ

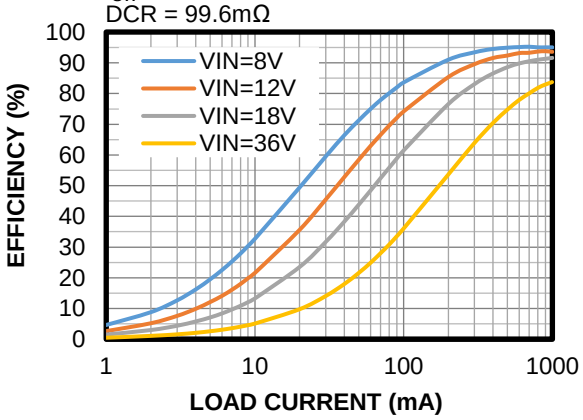


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

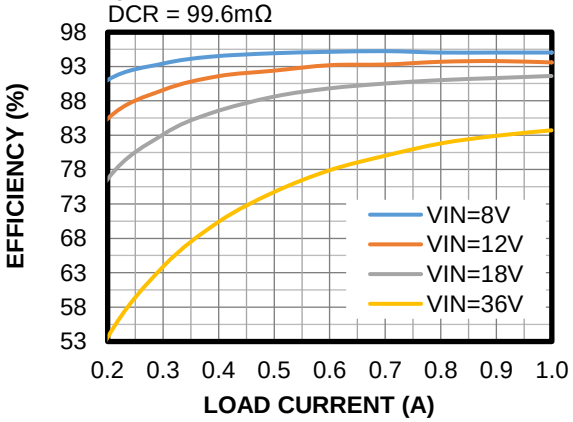
Efficiency vs. Load Current for 1006/0006 Versions

f_{SW} = 415kHz, L = 22µH, DCR = 99.6mΩ



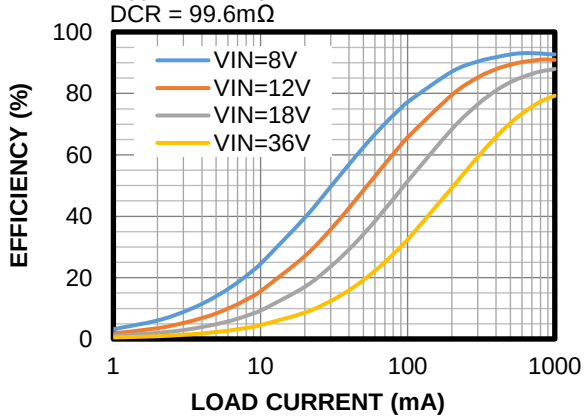
Efficiency vs. Load Current for 1006/0006 Versions

f_{SW} = 415kHz, L = 22µH, DCR = 99.6mΩ



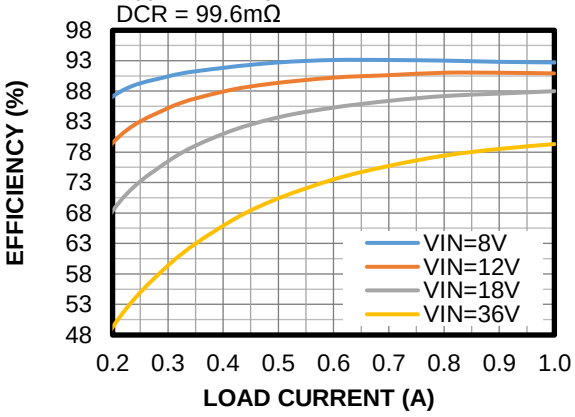
Efficiency vs. Load Current for 1006/0006 Versions

V_{OUT} = 3.3V, f_{SW} = 415kHz, L = 22µH, DCR = 99.6mΩ



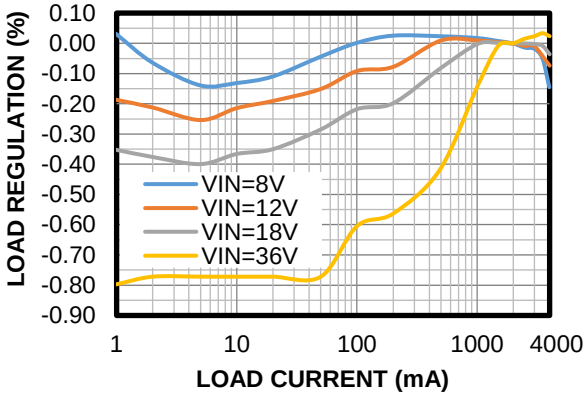
Efficiency vs. Load Current for 1006/0006 Versions

V_{OUT} = 3.3V, f_{SW} = 415kHz, L = 22µH, DCR = 99.6mΩ



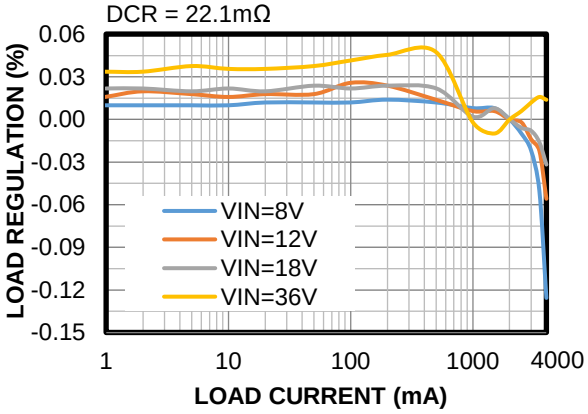
Load Regulation for 4000 Version

DCR = 22.1mΩ



Load Regulation for 4006 Version

DCR = 22.1mΩ

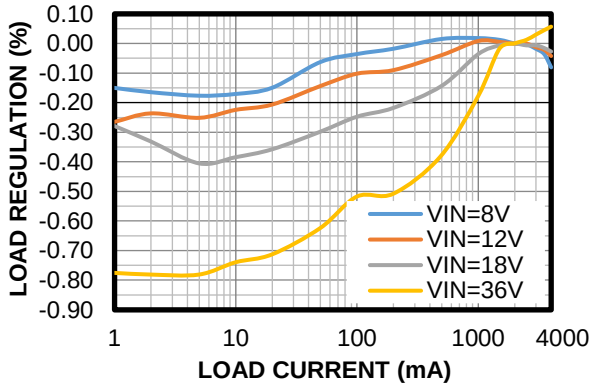


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

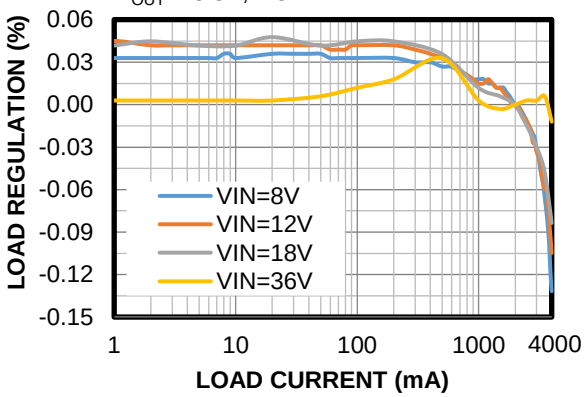
Load Regulation for 4000 Version

V_{OUT} = 3.3V, DCR = 22.1mΩ



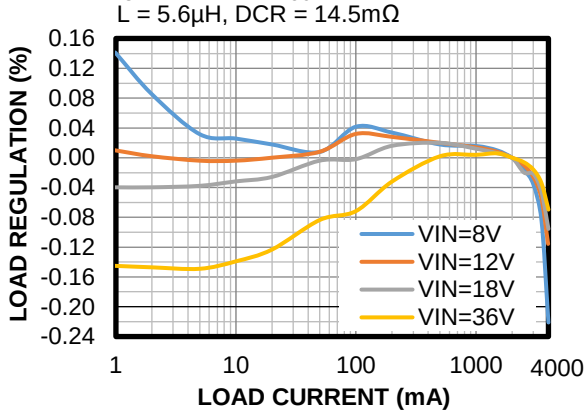
Load Regulation for 4006 Version

V_{OUT} = 3.3V, DCR = 22.1mΩ



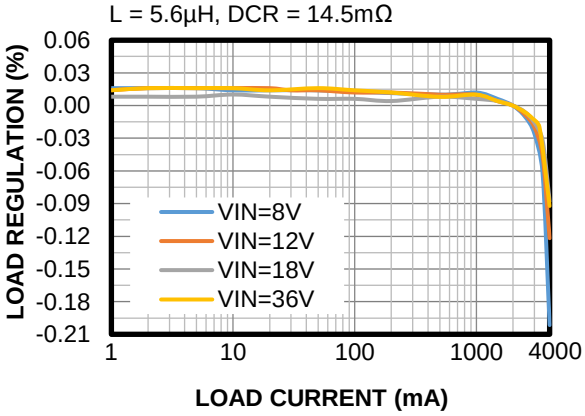
Load Regulation for 4000 Version

f_{SW} = 415kHz, C_{OUT} = 22µF x 3,
L = 5.6µH, DCR = 14.5mΩ



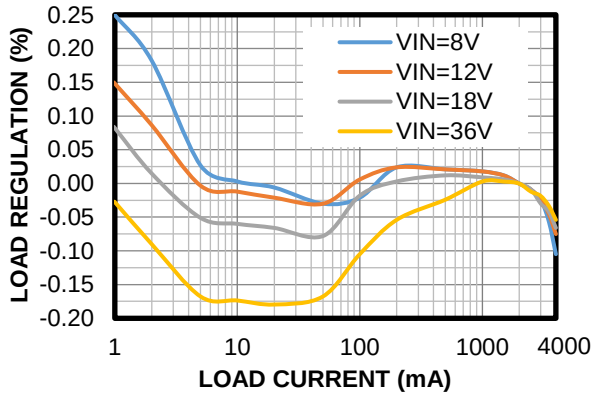
Load Regulation for 4006 Version

f_{SW} = 415kHz, C_{OUT} = 22µF x 3,
L = 5.6µH, DCR = 14.5mΩ



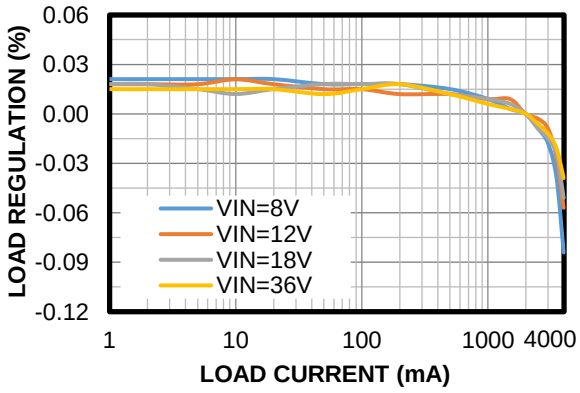
Load Regulation for 4000 Version

V_{OUT} = 3.3V, f_{SW} = 415kHz,
C_{OUT} = 22µF x 3, L = 5.6µH,
DCR = 14.5mΩ



Load Regulation for 4006 Version

V_{OUT} = 3.3V, f_{SW} = 415kHz, C_{OUT} = 22µF x 3,
L = 5.6µH, DCR = 14.5mΩ

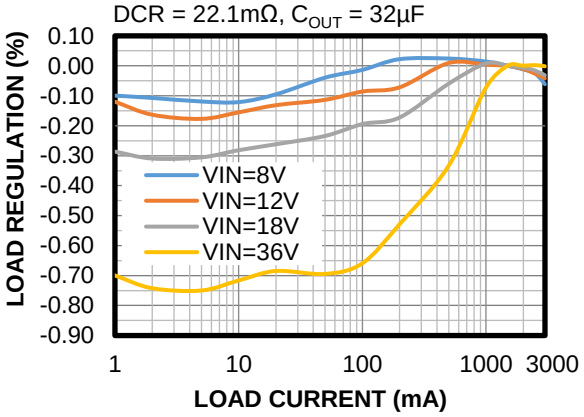


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

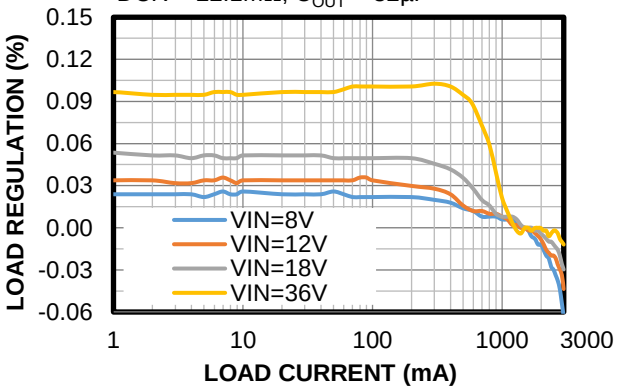
Load Regulation for 3000 Version

DCR = 22.1mΩ, C_{OUT} = 32µF



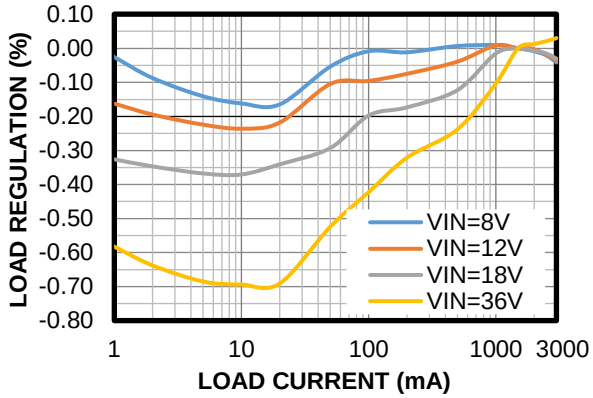
Load Regulation for 3006 Version

DCR = 22.1mΩ, C_{OUT} = 32µF



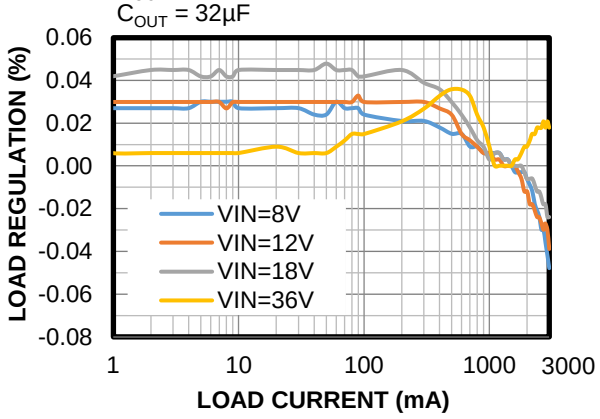
Load Regulation for 3000 Version

V_{OUT} = 3.3V, DCR = 22.1mΩ,
C_{OUT} = 32µF



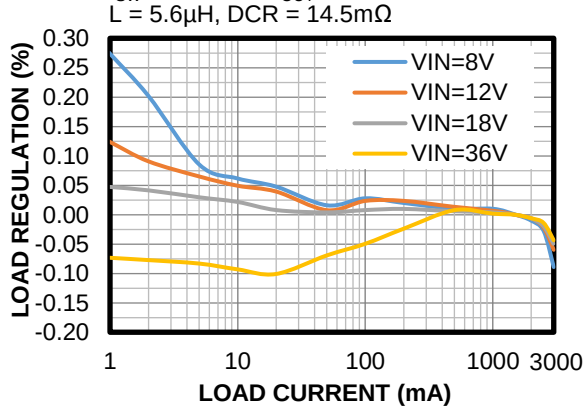
Load Regulation for 3006 Version

V_{OUT} = 3.3V, DCR = 22.1mΩ,
C_{OUT} = 32µF



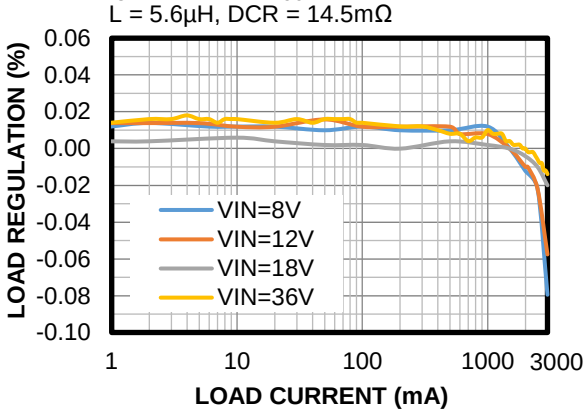
Load Regulation for 3000 Version

f_{SW} = 415kHz, C_{OUT} = 22µF x 2,
L = 5.6µH, DCR = 14.5mΩ



Load Regulation for 3006 Version

f_{SW} = 415kHz, C_{OUT} = 22µF x 2,
L = 5.6µH, DCR = 14.5mΩ

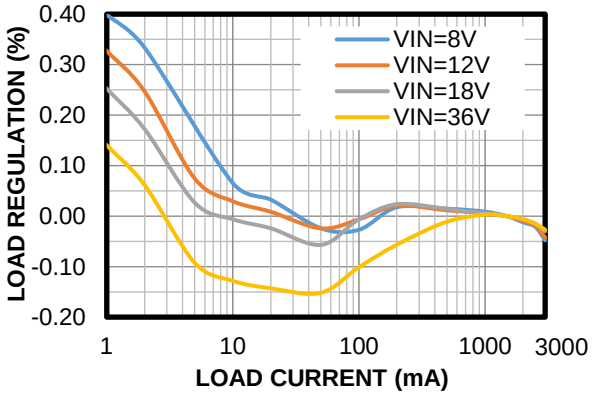


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

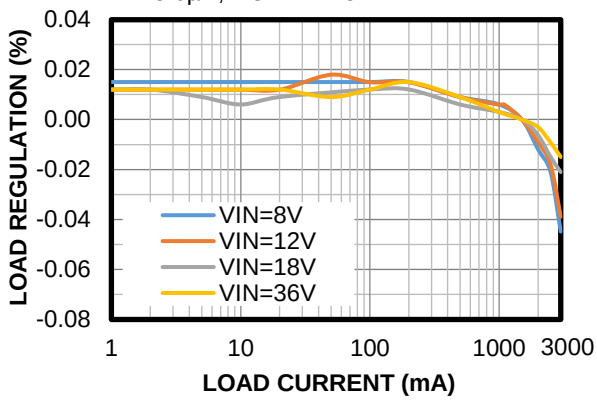
Load Regulation for 3000 Version

V_{OUT} = 3.3V, f_{SW} = 415kHz, C_{OUT} = 22µF x 2, L = 5.6µH, DCR = 14.5mΩ



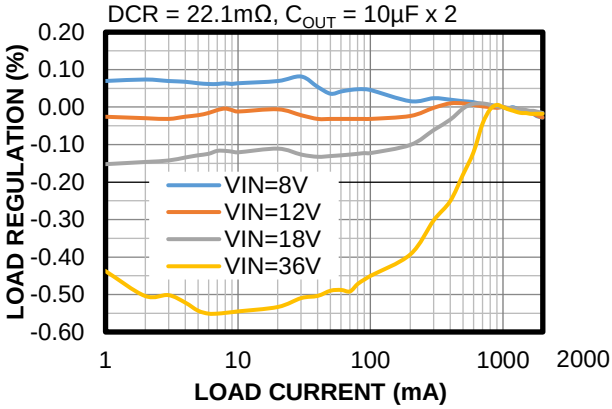
Load Regulation for 3006 Version

V_{OUT} = 3.3V, f_{SW} = 415kHz, C_{OUT} = 22µF x 2, L = 5.6µH, DCR = 14.5mΩ



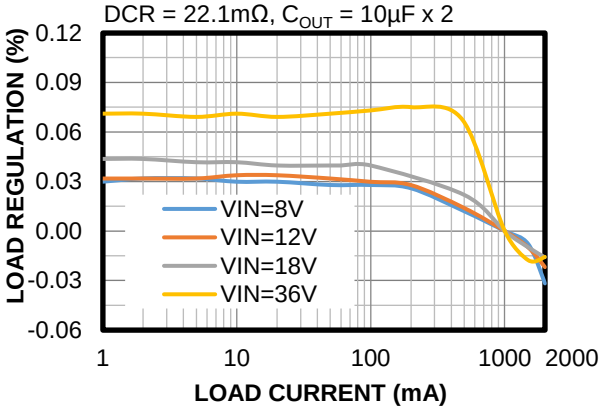
Load Regulation for 2000 Version

DCR = 22.1mΩ, C_{OUT} = 10µF x 2



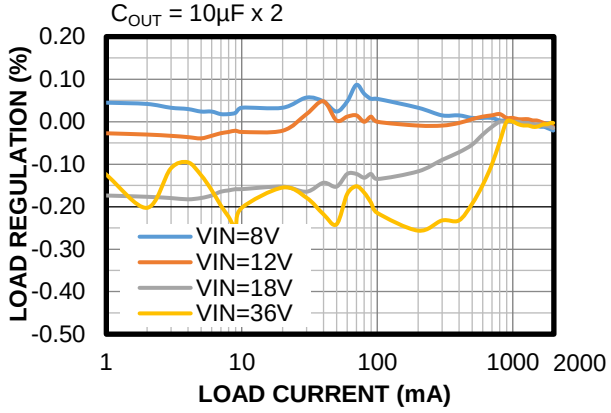
Load Regulation for 2006 Version

DCR = 22.1mΩ, C_{OUT} = 10µF x 2



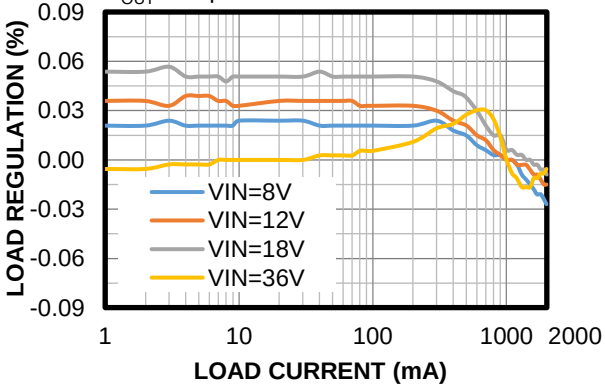
Load Regulation for 2000 Version

V_{OUT} = 3.3V, DCR = 22.1mΩ, C_{OUT} = 10µF x 2



Load Regulation for 2006 Version

V_{OUT} = 3.3V, DCR = 22.1mΩ, C_{OUT} = 10µF x 2

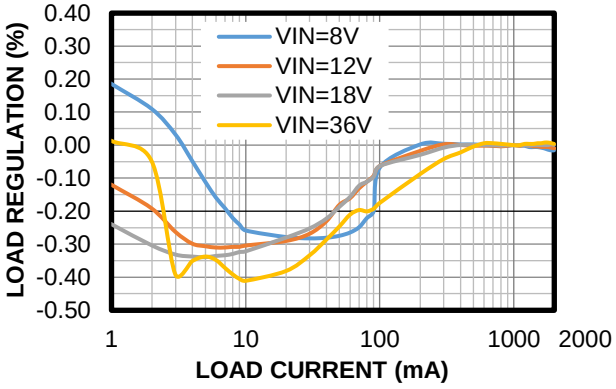


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

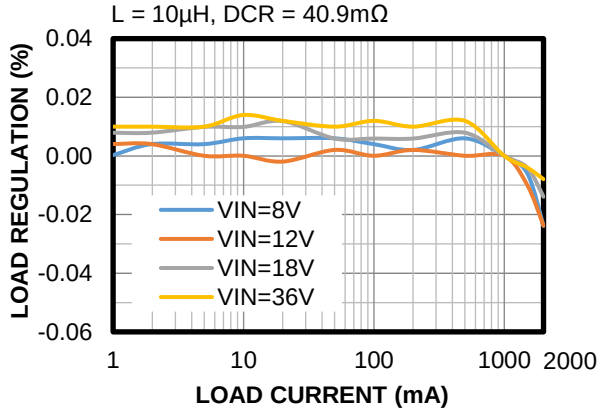
Load Regulation for 2000 Version

f_{SW} = 415kHz, C_{OUT} = 10µF x 3,
L = 10µH, DCR = 40.9mΩ



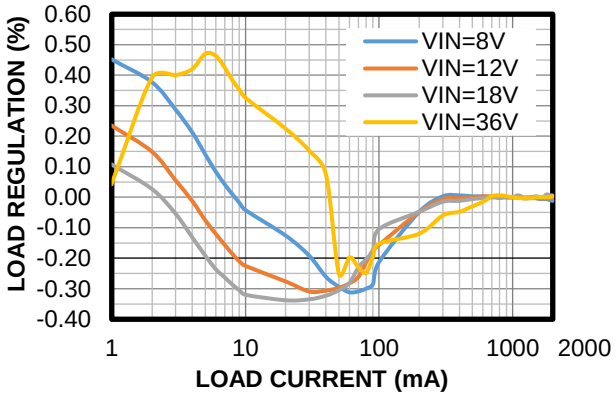
Load Regulation for 2006 Version

f_{SW} = 415kHz, C_{OUT} = 10µF x 3,
L = 10µH, DCR = 40.9mΩ



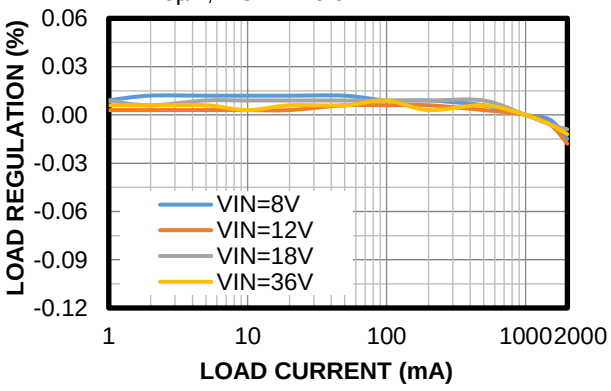
Load Regulation for 2000 Version

V_{OUT} = 3.3V, f_{SW} = 415kHz,
C_{OUT} = 10µF x 3, L = 10µH,
DCR = 40.9mΩ



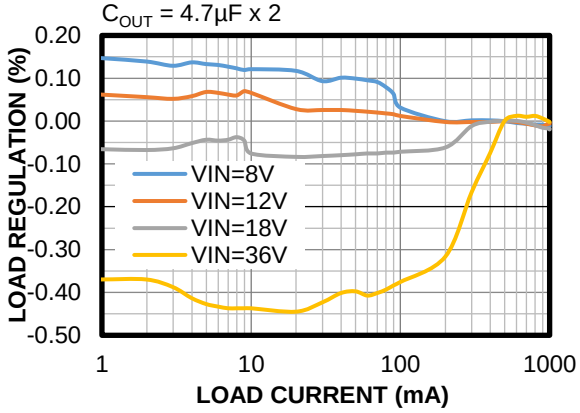
Load Regulation for 2006 Version

V_{OUT} = 3.3V, f_{SW} = 415kHz, C_{OUT} = 10µF x 3,
L = 10µH, DCR = 40.9mΩ



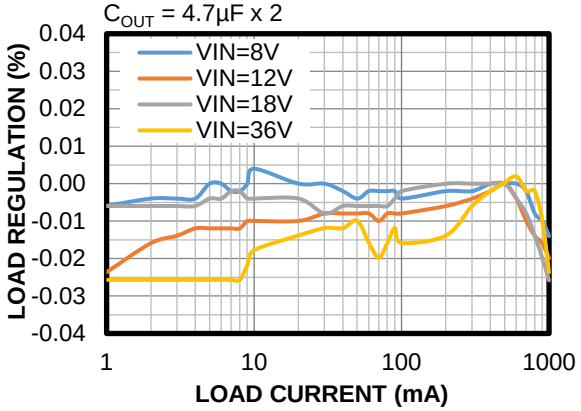
Load Regulation for 1000 Version

L = 5.6µH, DCR = 25.8mΩ,
C_{OUT} = 4.7µF x 2



Load Regulation for 1006 Version

L = 5.6µH, DCR = 25.8mΩ,
C_{OUT} = 4.7µF x 2

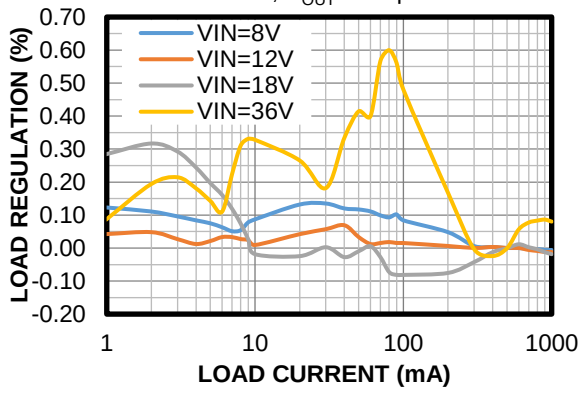


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

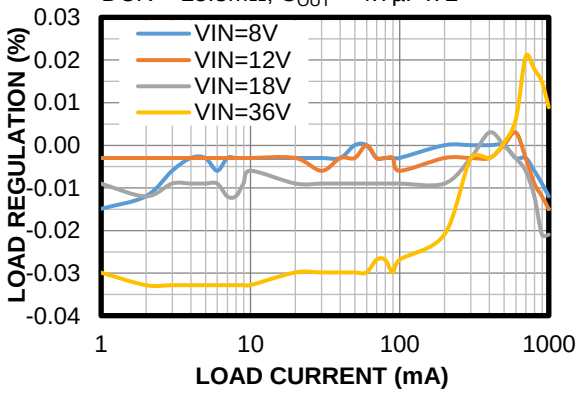
Load Regulation for 1000 Version

V_{OUT} = 3.3V, L = 5.6µH,
DCR = 25.8mΩ, C_{OUT} = 4.7µF x 2



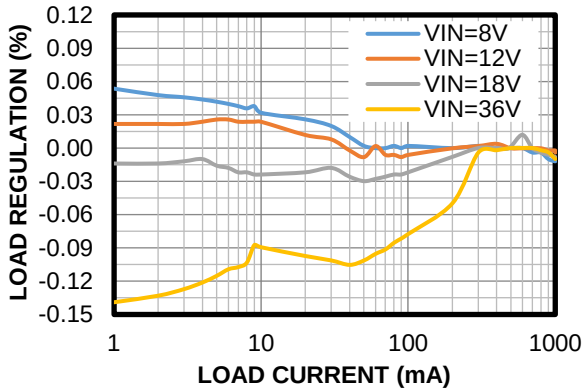
Load Regulation for 1006 Version

V_{OUT} = 3.3V, L = 5.6µH,
DCR = 25.8mΩ, C_{OUT} = 4.7µF x 2



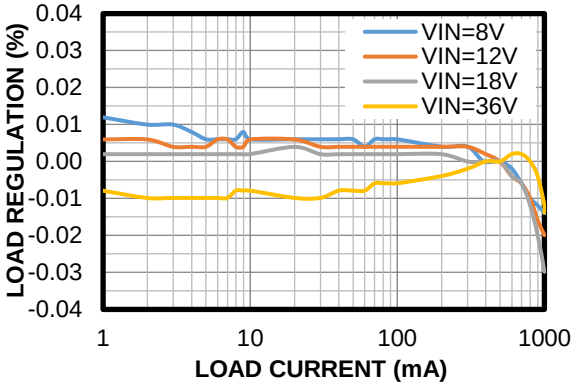
Load Regulation for 1000 Version

f_{SW} = 415kHz, C_{OUT} = 4.7µF x 3,
L = 22µH, DCR = 99.6mΩ



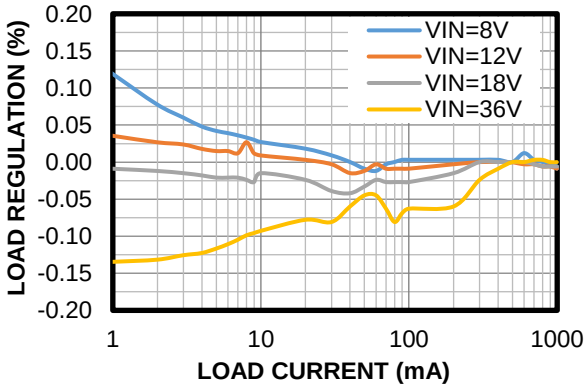
Load Regulation for 1006 Version

f_{SW} = 415kHz, C_{OUT} = 4.7µF x 3,
L = 22µH, DCR = 99.6mΩ



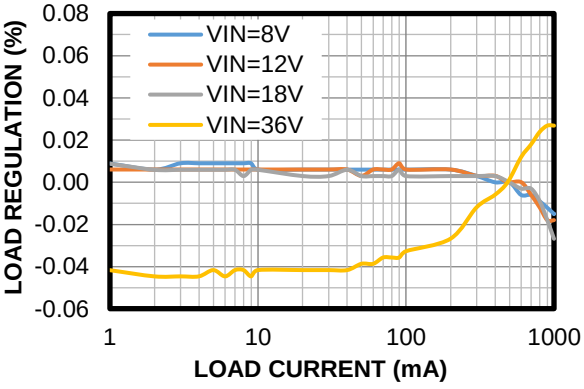
Load Regulation for 1000 Version

V_{OUT} = 3.3V, f_{SW} = 415kHz,
C_{OUT} = 4.7µF x 3, L = 22µH,
DCR = 99.6mΩ



Load Regulation for 1006 Version

V_{OUT} = 3.3V, f_{SW} = 415kHz,
C_{OUT} = 4.7µF x 3, L = 22µH,
DCR = 99.6mΩ

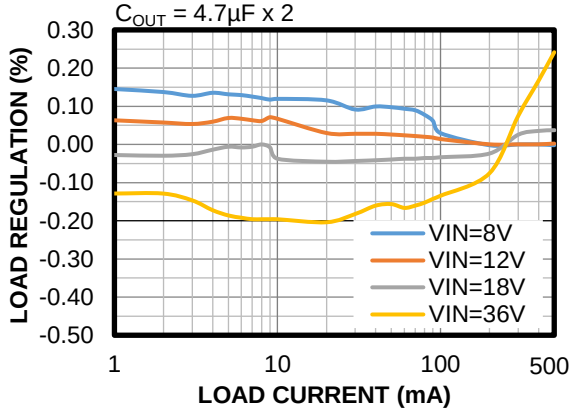


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

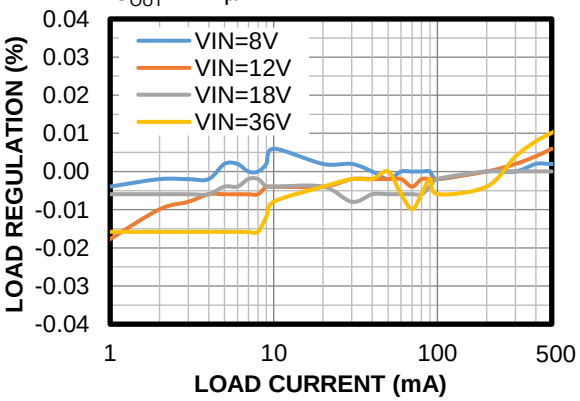
Load Regulation for 0000 Version

L = 5.6µH, DCR = 25.8mΩ,
C_{OUT} = 4.7µF x 2



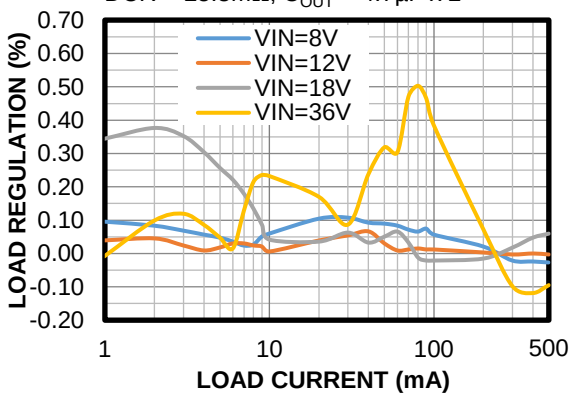
Load Regulation for 0006 Version

L = 5.6µH, DCR = 25.8mΩ,
C_{OUT} = 4.7µF x 2



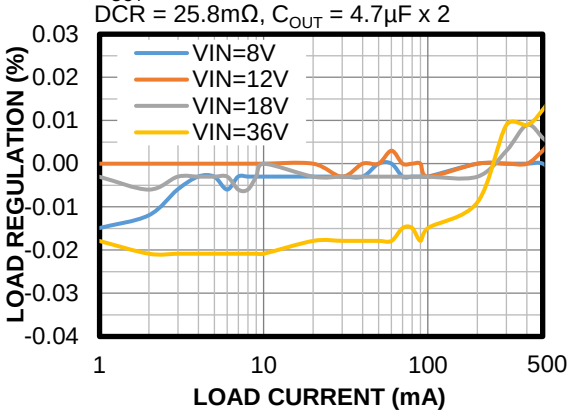
Load Regulation for 0000 Version

V_{OUT} = 3.3V, L = 5.6µH,
DCR = 25.8mΩ, C_{OUT} = 4.7µF x 2



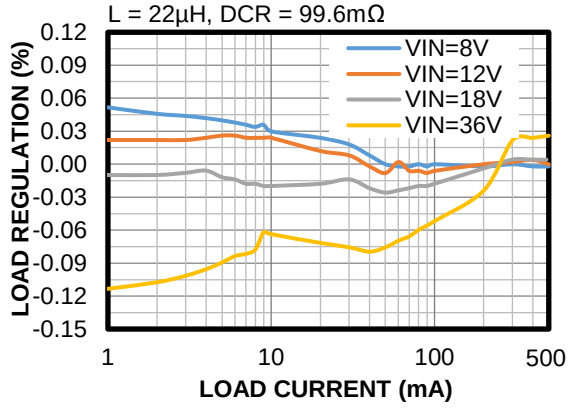
Load Regulation for 0006 Version

V_{OUT} = 3.3V, L = 5.6µH,
DCR = 25.8mΩ, C_{OUT} = 4.7µF x 2



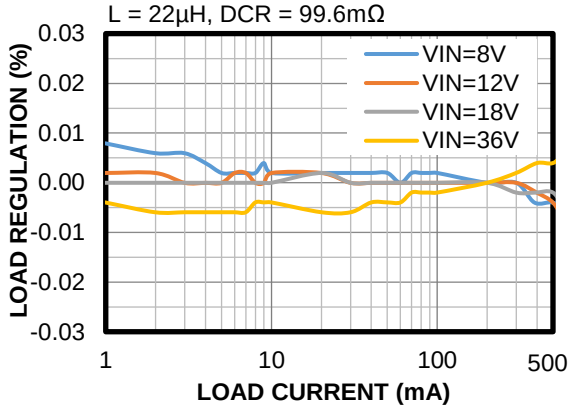
Load Regulation for 0000 Version

f_{SW} = 415kHz, C_{OUT} = 4.7µF x 3,
L = 22µH, DCR = 99.6mΩ



Load Regulation for 0006 Version

f_{SW} = 415kHz, C_{OUT} = 4.7µF x 3,
L = 22µH, DCR = 99.6mΩ

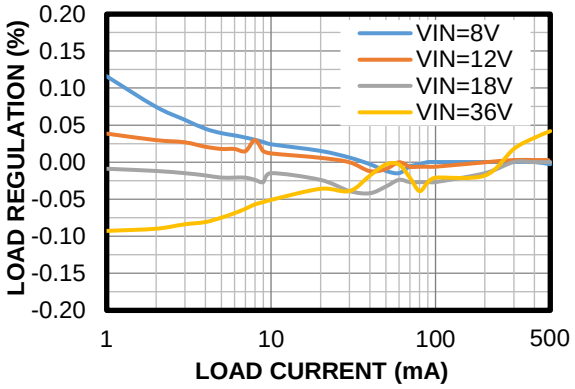


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

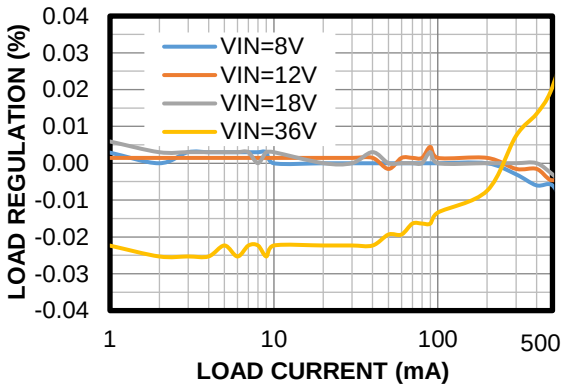
Load Regulation for 0000 Version

V_{OUT} = 3.3V, f_{SW} = 415kHz,
C_{OUT} = 4.7µF x 3, L = 22µH,
DCR = 99.6mΩ



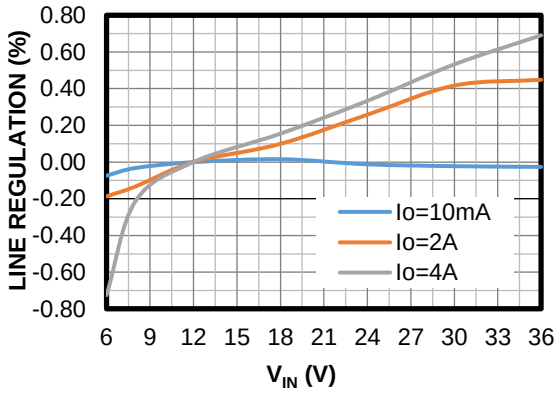
Load Regulation for 0006 Version

V_{OUT} = 3.3V, f_{SW} = 415kHz,
C_{OUT} = 4.7µF x 3, L = 22µH,
DCR = 99.6mΩ



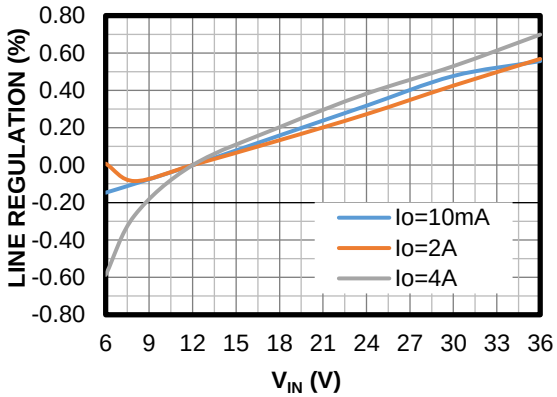
Line Regulation for 4000 Version

DCR = 22.1mΩ



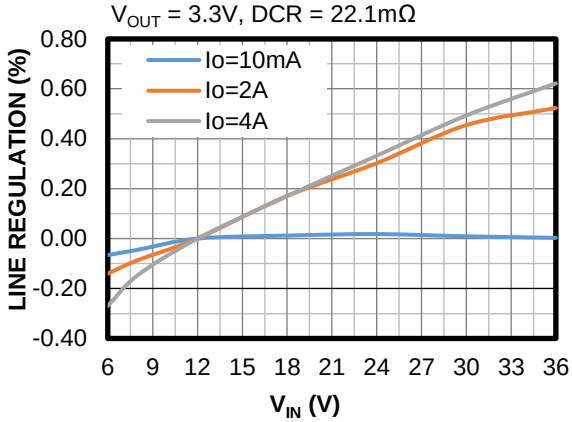
Line Regulation for 4006 Version

DCR = 22.1mΩ



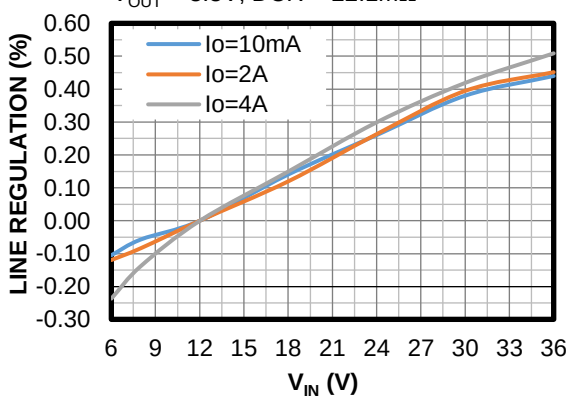
Line Regulation for 4000 Version

V_{OUT} = 3.3V, DCR = 22.1mΩ



Line Regulation for 4006 Version

V_{OUT} = 3.3V, DCR = 22.1mΩ

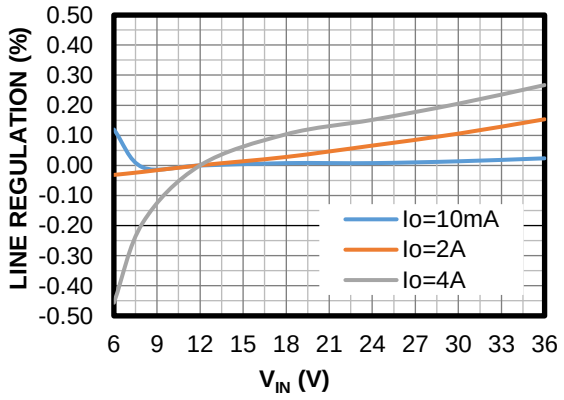


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

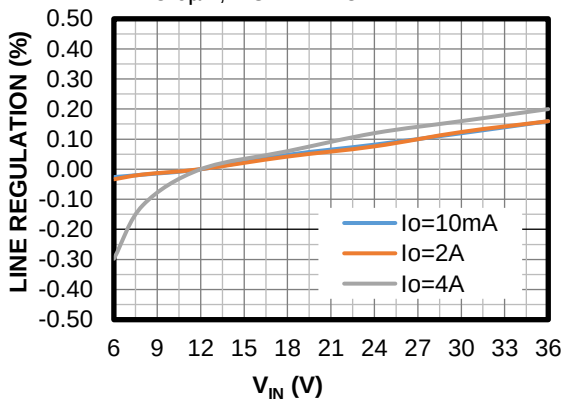
Line Regulation for 4000 Version

f_{SW} = 415kHz, C_{OUT} = 22µF x 3,
L = 5.6µH, DCR = 14.5mΩ



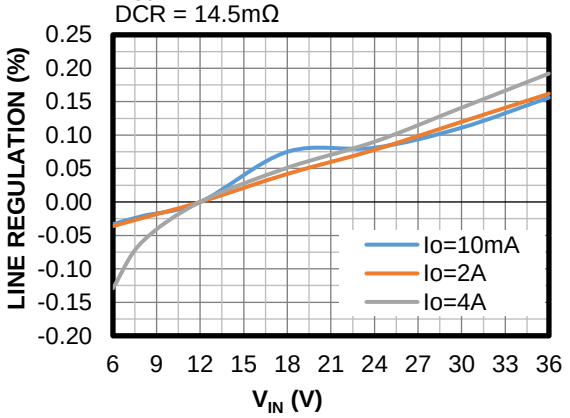
Line Regulation for 4006 Version

f_{SW} = 415kHz, C_{OUT} = 22µF x 3,
L = 5.6µH, DCR = 14.5mΩ



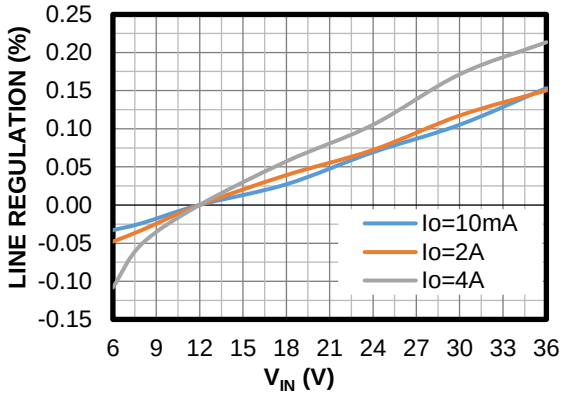
Line Regulation for 4000 Version

V_{OUT} = 3.3V, f_{SW} = 415kHz,
C_{OUT} = 22µF x 3, L = 5.6µH,
DCR = 14.5mΩ



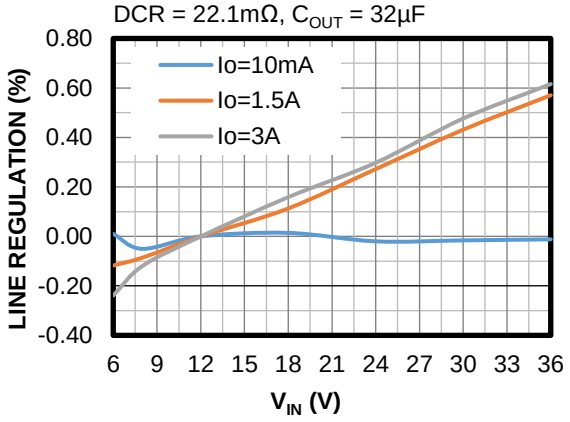
Line Regulation for 4006 Version

V_{OUT} = 3.3V, f_{SW} = 415kHz,
C_{OUT} = 22µF x 3, L = 5.6µH,
DCR = 14.5mΩ



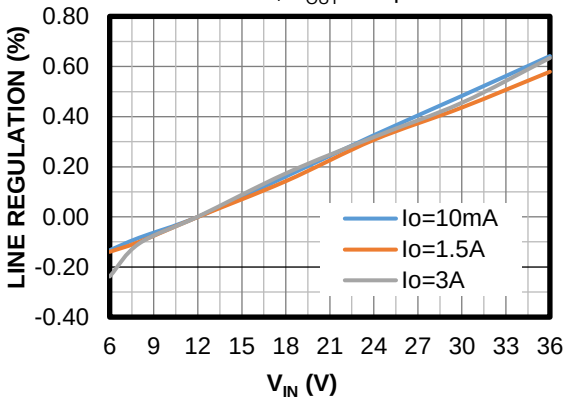
Line Regulation for 3000 Version

DCR = 22.1mΩ, C_{OUT} = 32µF



Line Regulation for 3006 Version

DCR = 22.1mΩ, C_{OUT} = 32µF

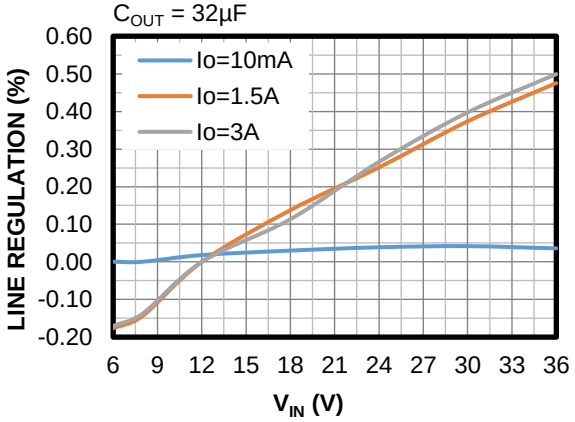


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

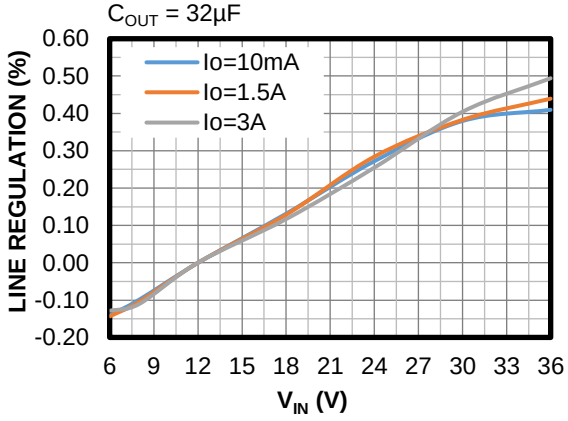
Line Regulation for 3000 Version

V_{OUT} = 3.3V, DCR = 22.1mΩ,
C_{OUT} = 32µF



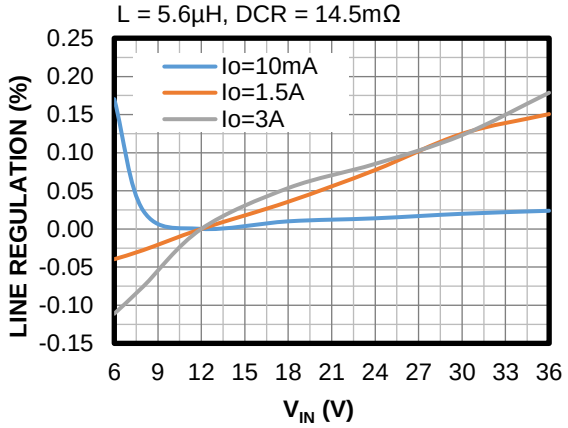
Line Regulation for 3006 Version

V_{OUT} = 3.3V, DCR = 22.1mΩ,
C_{OUT} = 32µF



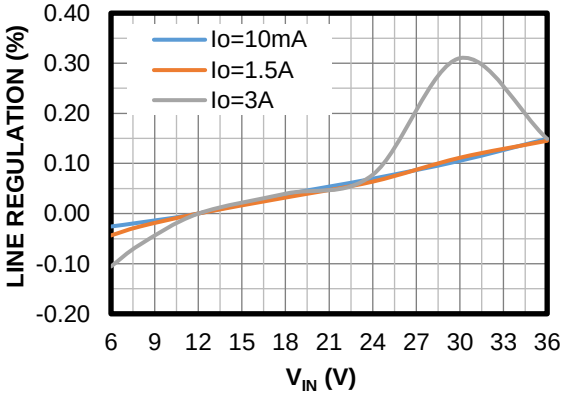
Line Regulation for 3000 Version

f_{SW} = 415kHz, C_{OUT} = 22µF x 2,
L = 5.6µH, DCR = 14.5mΩ



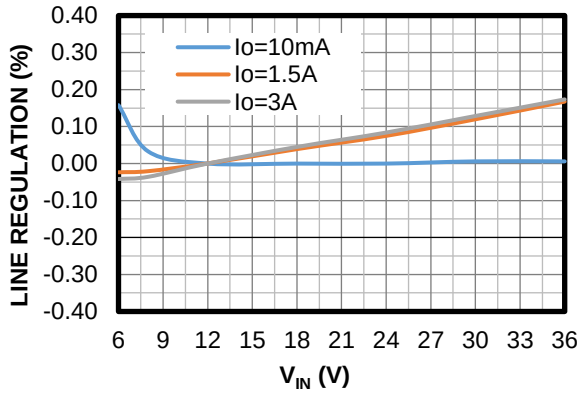
Line Regulation for 3006 Version

f_{SW} = 415kHz, C_{OUT} = 22µF x 2,
L = 5.6µH, DCR = 14.5mΩ



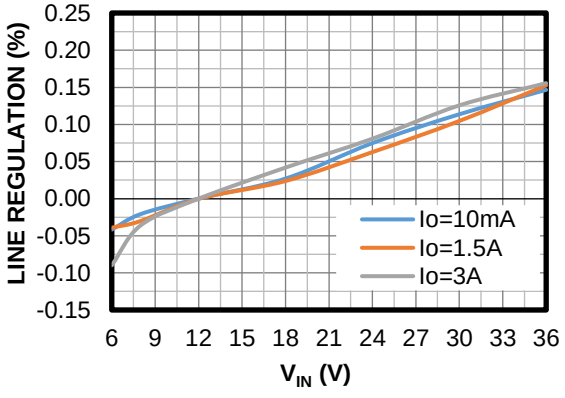
Line Regulation for 3000 Version

V_{OUT} = 3.3V, f_{SW} = 415kHz,
C_{OUT} = 22µF x 2, L = 5.6µH,
DCR = 14.5mΩ



Line Regulation for 3006 Version

V_{OUT} = 3.3V, f_{SW} = 415kHz,
C_{OUT} = 22µF x 2, L = 5.6µH,
DCR = 14.5mΩ

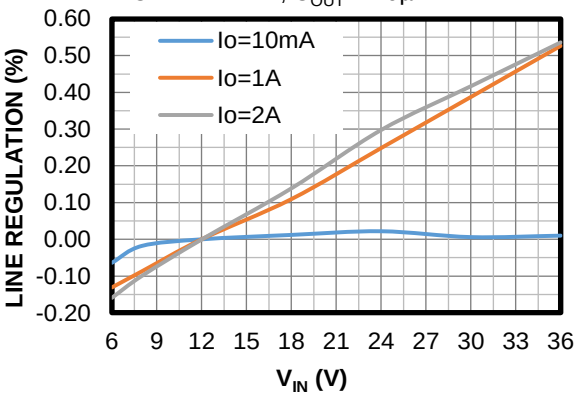


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

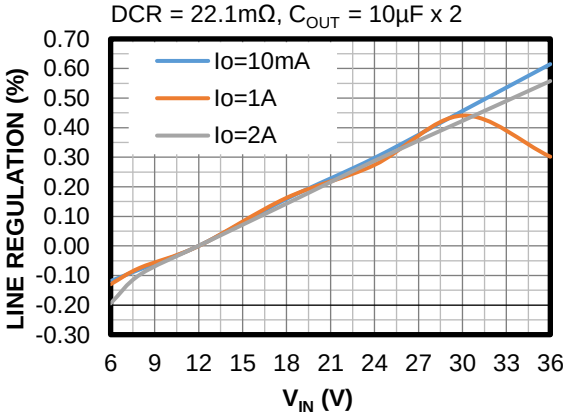
Line Regulation for 2000 Version

DCR = 22.1mΩ, C_{OUT} = 10µF x 2



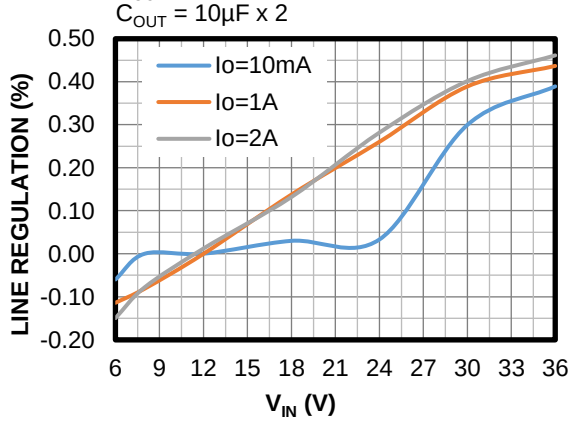
Line Regulation for 2006 Version

DCR = 22.1mΩ, C_{OUT} = 10µF x 2



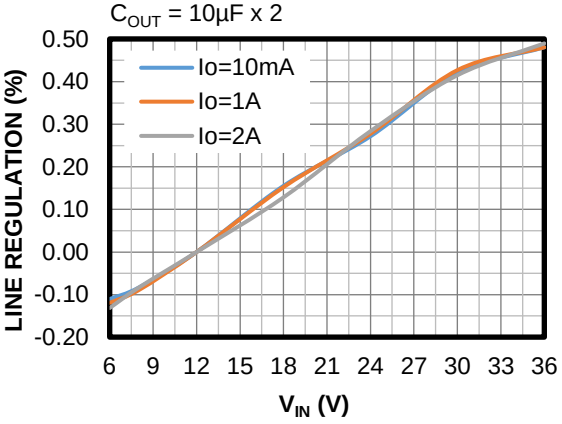
Line Regulation for 2000 Version

V_{OUT} = 3.3V, DCR = 22.1mΩ,
C_{OUT} = 10µF x 2



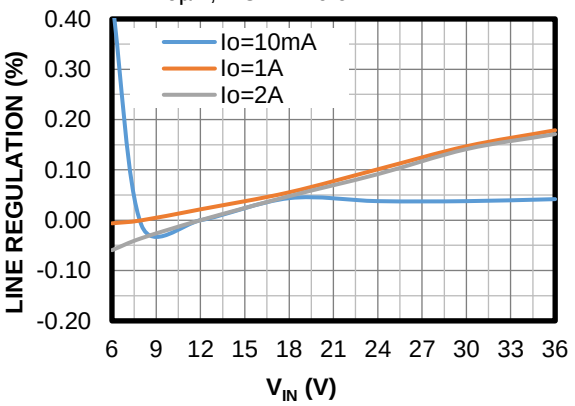
Line Regulation for 2006 Version

V_{OUT} = 3.3V, DCR = 22.1mΩ,
C_{OUT} = 10µF x 2



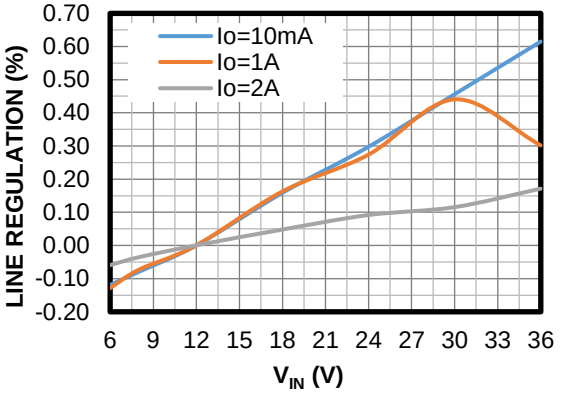
Line Regulation for 2000 Version

f_{SW} = 415kHz, C_{OUT} = 10µF x 3,
L = 10µH, DCR = 40.9mΩ



Line Regulation for 2006 Version

f_{SW} = 415kHz, C_{OUT} = 10µF x 3,
L = 10µH, DCR = 40.9mΩ

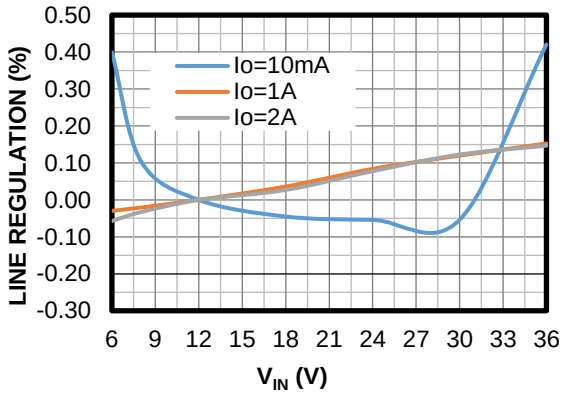


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

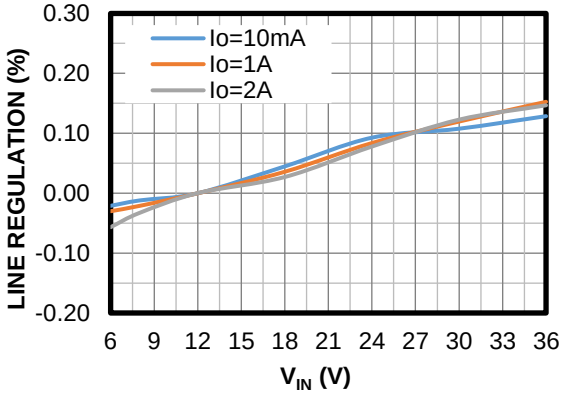
Line Regulation for 2000 Version

V_{OUT} = 3.3V, f_{SW} = 415kHz,
C_{OUT} = 10µF x 3, L = 10µH,
DCR = 40.9mΩ



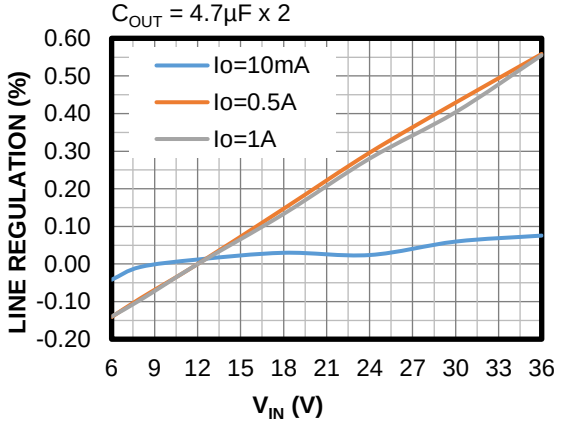
Line Regulation for 2006 Version

V_{OUT} = 3.3V, f_{SW} = 415kHz,
C_{OUT} = 10µF x 3, L = 10µH,
DCR = 40.9mΩ



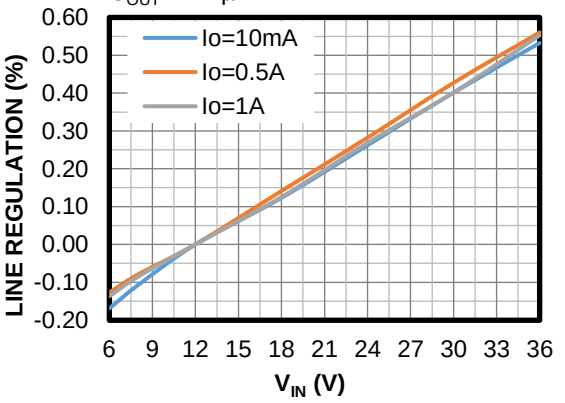
Line Regulation for 1000 Version

L = 5.6µH, DCR = 25.8mΩ,
C_{OUT} = 4.7µF x 2



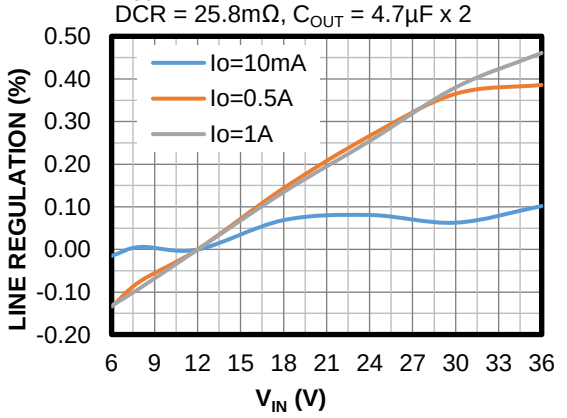
Line Regulation for 1006 Version

V_{OUT} = 5V, L = 5.6µH, DCR = 25.8mΩ,
C_{OUT} = 4.7µF x 2



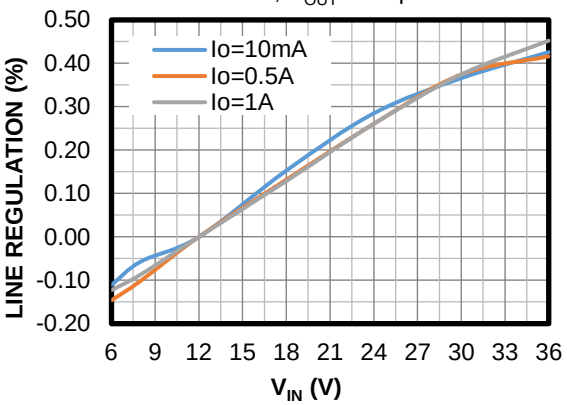
Line Regulation for 1000 Version

V_{OUT} = 3.3V, L = 5.6µH,
DCR = 25.8mΩ, C_{OUT} = 4.7µF x 2



Line Regulation for 1006 Version

V_{OUT} = 3.3V, L = 5.6µH,
DCR = 25.8mΩ, C_{OUT} = 4.7µF x 2

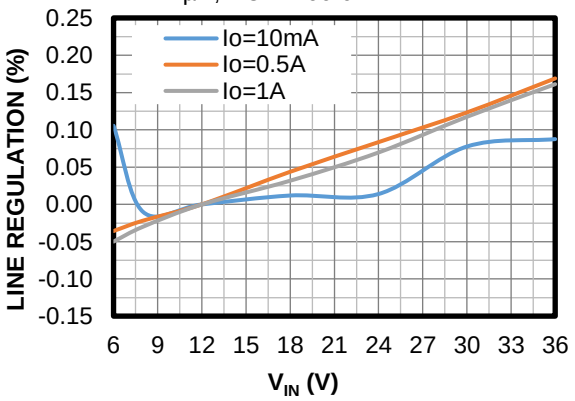


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

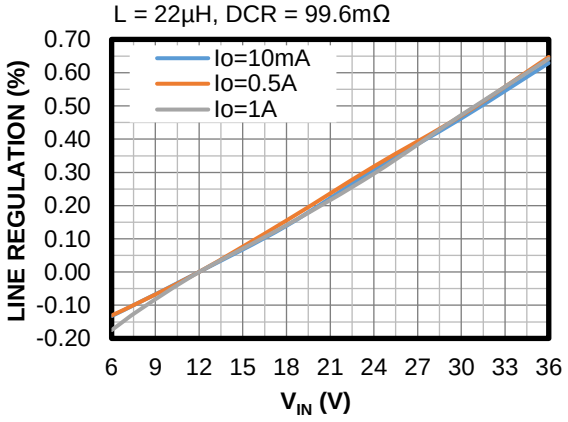
Line Regulation for 1000 Version

f_{SW} = 415kHz, C_{OUT} = 4.7µF x 3,
L = 22µH, DCR = 99.6mΩ



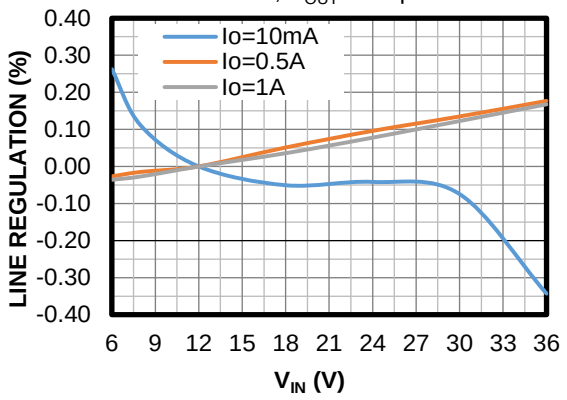
Line Regulation for 1006 Version

f_{SW} = 415kHz, C_{OUT} = 4.7µF x 3,
L = 22µH, DCR = 99.6mΩ



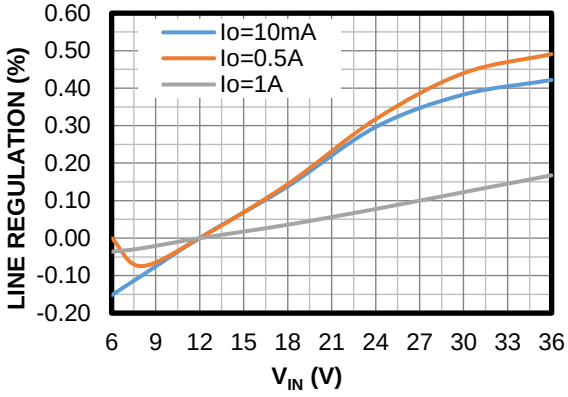
Line Regulation for 1000 Version

V_{OUT} = 3.3V, f_{SW} = 415kHz, L = 22µH,
DCR = 99.6mΩ, C_{OUT} = 4.7µF x 3



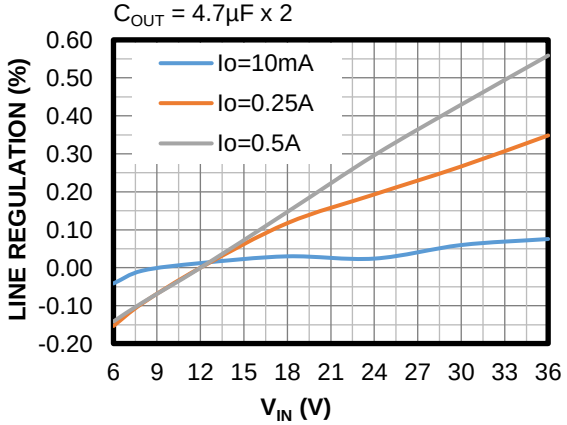
Line Regulation for 1006 Version

V_{OUT} = 3.3V, f_{SW} = 415kHz, L = 22µH,
DCR = 99.6mΩ, C_{OUT} = 4.7µF x 3



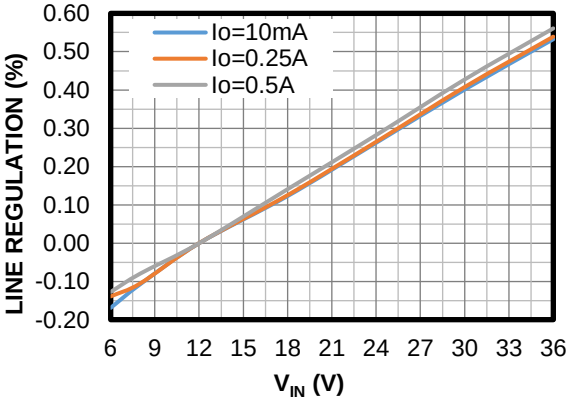
Line Regulation for 0000 Version

L = 5.6µH, DCR = 25.8mΩ,
C_{OUT} = 4.7µF x 2



Line Regulation for 0006 Version

L = 5.6µH, DCR = 25.8mΩ,
C_{OUT} = 4.7µF x 2

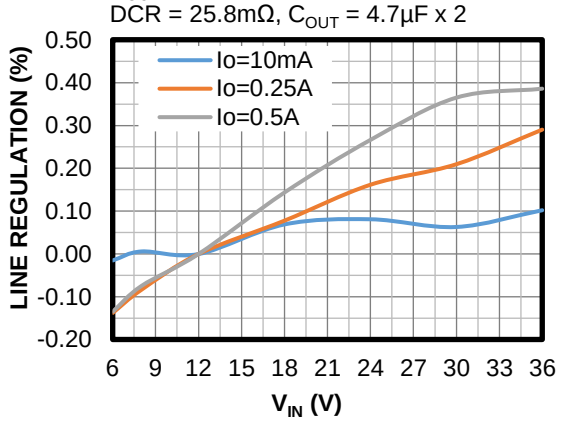


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

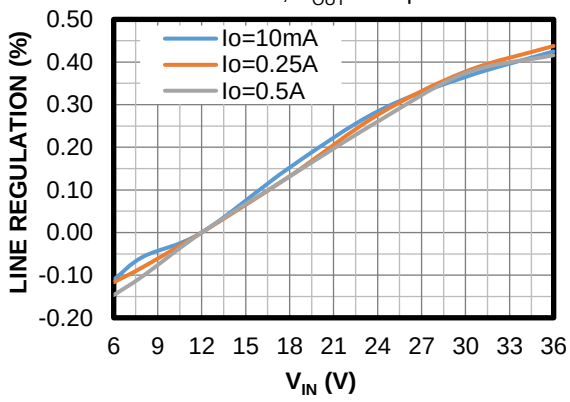
Line Regulation for 0000 Version

V_{OUT} = 3.3V, L = 5.6µH,
DCR = 25.8mΩ, C_{OUT} = 4.7µF x 2



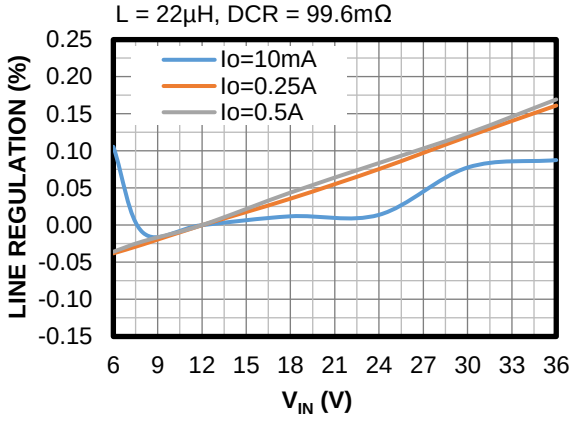
Line Regulation for 0006 Version

V_{OUT} = 3.3V, L = 5.6µH,
DCR = 25.8mΩ, C_{OUT} = 4.7µF x 2



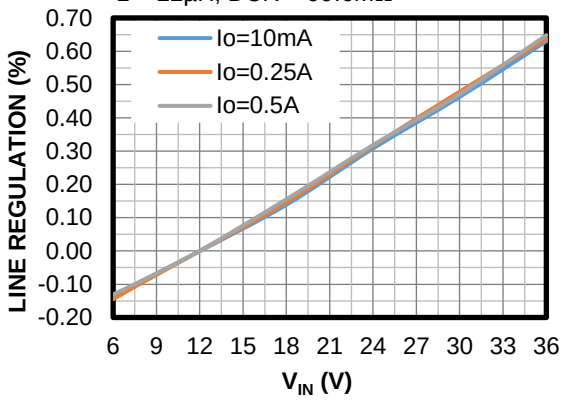
Line Regulation for 0000 Version

f_{SW} = 415kHz, C_{OUT} = 4.7µF x 3,
L = 22µH, DCR = 99.6mΩ



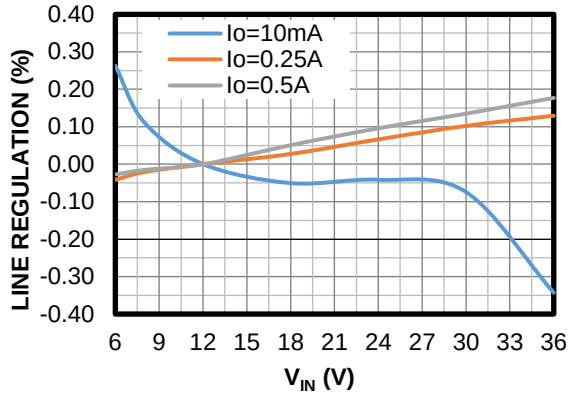
Line Regulation for 0006 Version

f_{SW} = 415kHz, C_{OUT} = 4.7µF x 3,
L = 22µH, DCR = 99.6mΩ



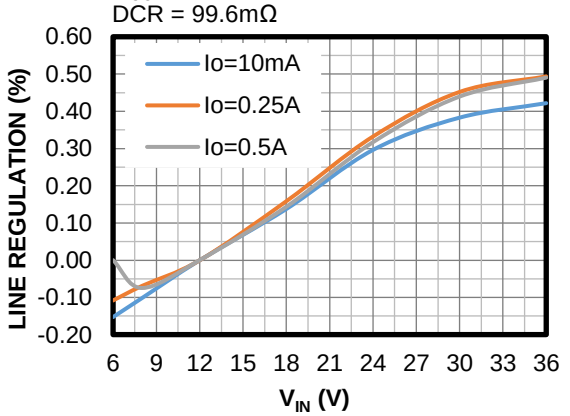
Line Regulation for 0000 Version

V_{OUT} = 3.3V, f_{SW} = 415kHz,
C_{OUT} = 4.7µF x 3, L = 22µH,
DCR = 99.6mΩ,



Line Regulation for 0006 Version

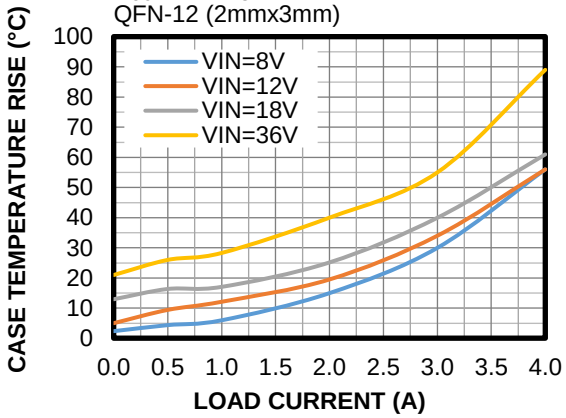
V_{OUT} = 3.3V, f_{SW} = 415kHz,
C_{OUT} = 4.7µF x 3, L = 22µH,
DCR = 99.6mΩ



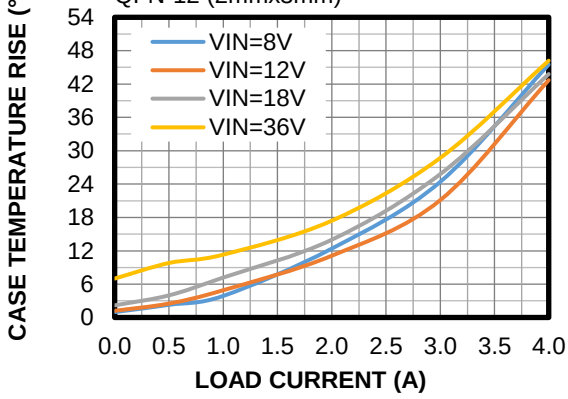
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

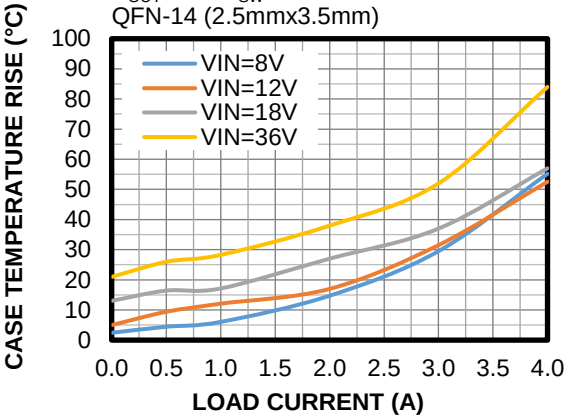
Case Temperature Rise
V_{OUT} = 5V, f_{SW} = 2.2MHz, FCCM,
QFN-12 (2mmx3mm)



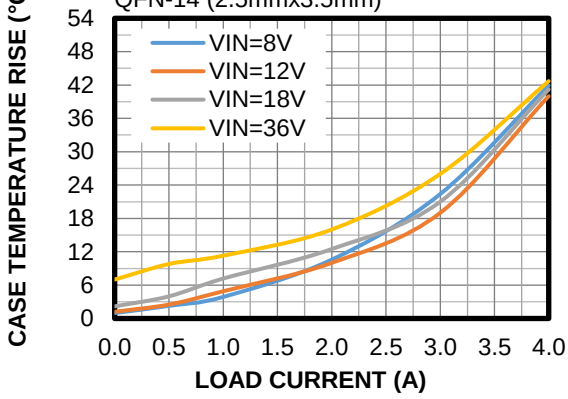
Case Temperature Rise
V_{OUT} = 5V, f_{SW} = 415kHz, FCCM,
QFN-12 (2mmx3mm)



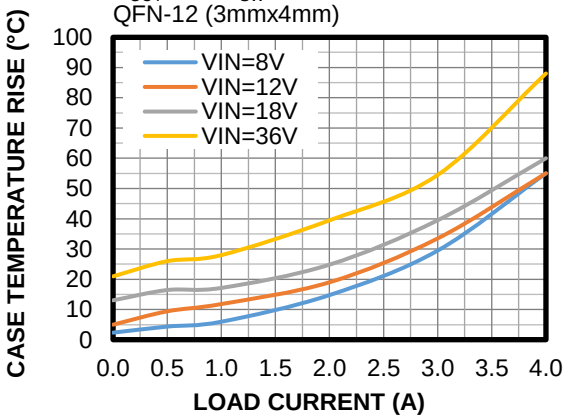
Case Temperature Rise
V_{OUT} = 5V, f_{SW} = 2.2MHz, FCCM,
QFN-14 (2.5mmx3.5mm)



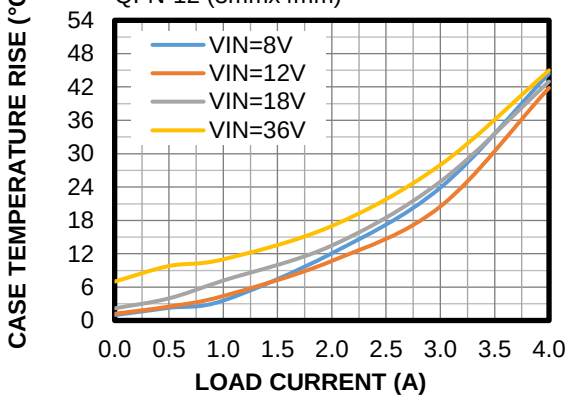
Case Temperature Rise
V_{OUT} = 5V, f_{SW} = 415kHz, FCCM,
QFN-14 (2.5mmx3.5mm)



Case Temperature Rise
V_{OUT} = 5V, f_{SW} = 2.2MHz, FCCM,
QFN-12 (3mmx4mm)



Case Temperature Rise
V_{OUT} = 5V, f_{SW} = 415kHz, FCCM,
QFN-12 (3mmx4mm)

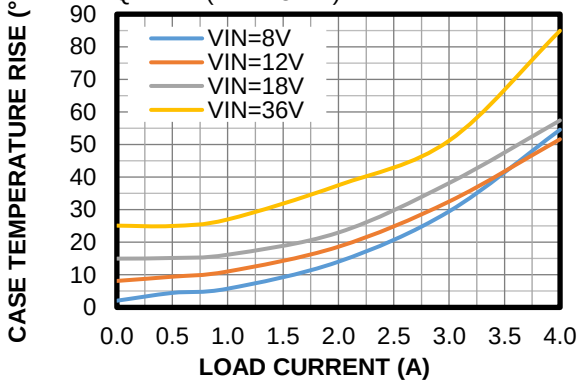


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

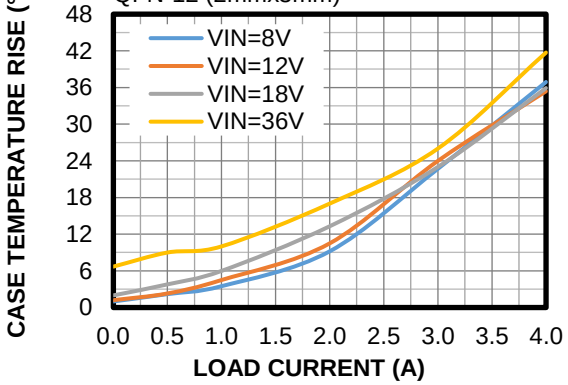
Case Temperature Rise

V_{OUT} = 3.3V, f_{SW} = 2.2MHz, FCCM, QFN-12 (2mmx3mm)



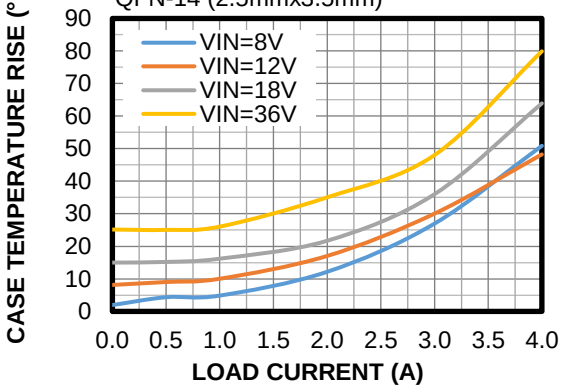
Case Temperature Rise

V_{OUT} = 3.3V, f_{SW} = 415kHz, FCCM, QFN-12 (2mmx3mm)



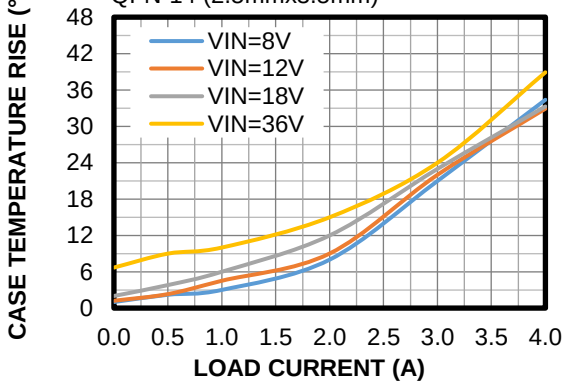
Case Temperature Rise

V_{OUT} = 3.3V, f_{SW} = 2.2MHz, FCCM, QFN-14 (2.5mmx3.5mm)



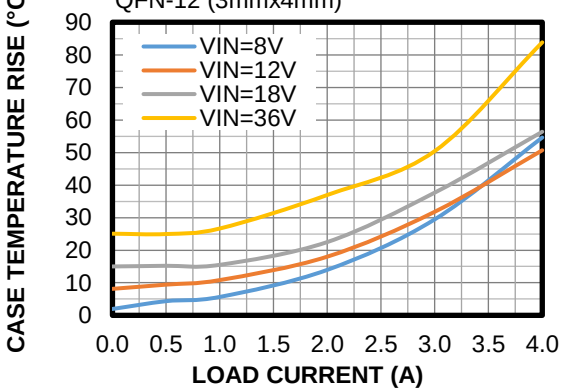
Case Temperature Rise

V_{OUT} = 3.3V, f_{SW} = 415kHz, FCCM, QFN-14 (2.5mmx3.5mm)



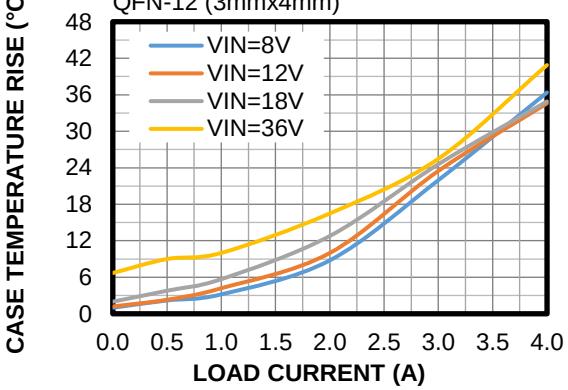
Case Temperature Rise

V_{OUT} = 3.3V, f_{SW} = 2.2MHz, FCCM, QFN-12 (3mmx4mm)



Case Temperature Rise

V_{OUT} = 3.3V, f_{SW} = 415kHz, FCCM, QFN-12 (3mmx4mm)

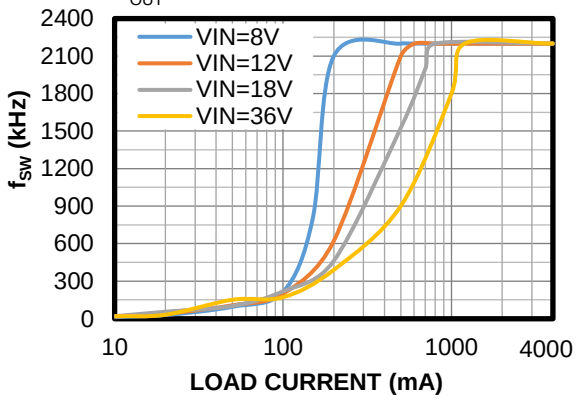


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

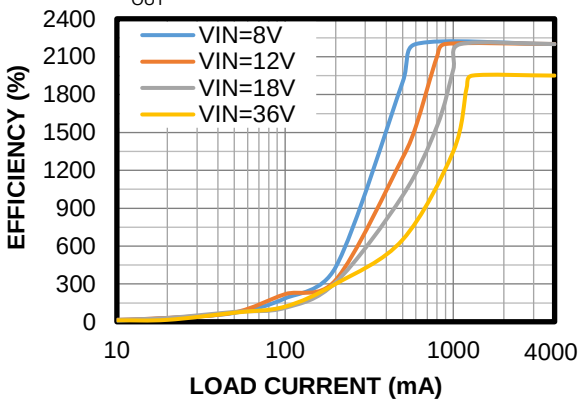
Switching Frequency vs. Load Current for 4000/3000 Versions

V_{OUT} = 5V



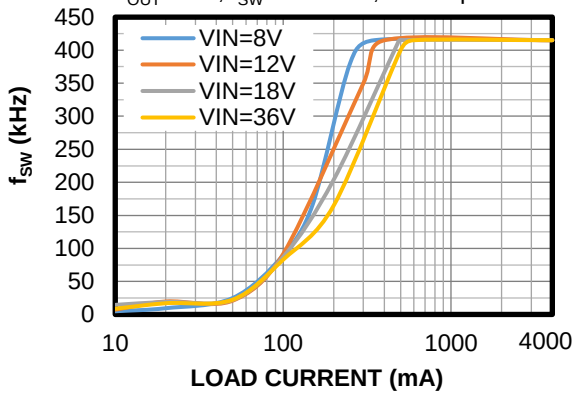
Switching Frequency vs. Load Current for 4000/3000 Versions

V_{OUT} = 3.3V



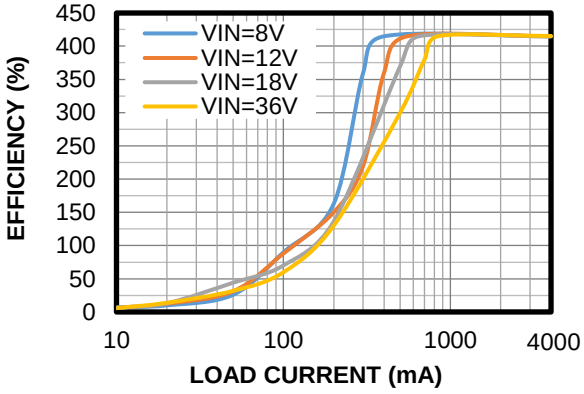
Switching Frequency vs. Load Current for 4000/3000 Versions

V_{OUT} = 5V, f_{SW} = 415kHz, L = 5.6µH



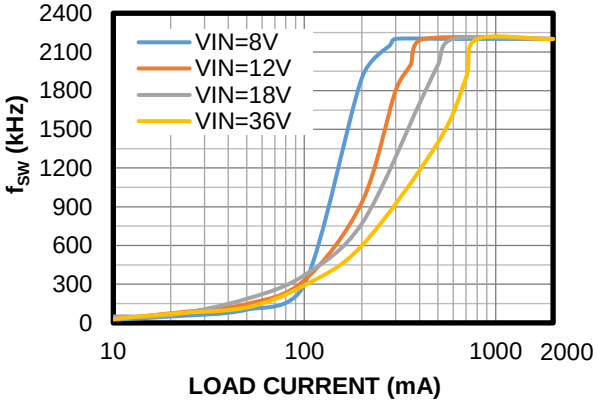
Switching Frequency vs. Load Current for 4000/3000 Versions

V_{OUT} = 3.3V, f_{SW} = 415kHz, L = 5.6µH



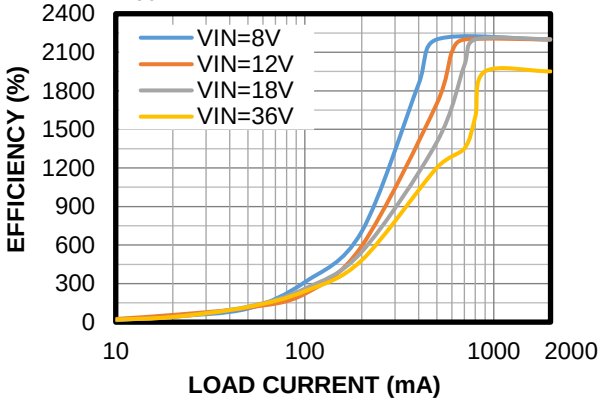
Switching Frequency vs. Load Current for 2000 Version

V_{OUT} = 5V



Switching Frequency vs. Load Current for 2000 Version

V_{OUT} = 3.3V

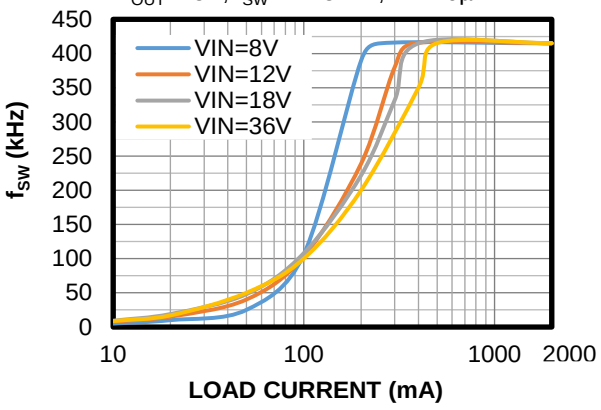


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

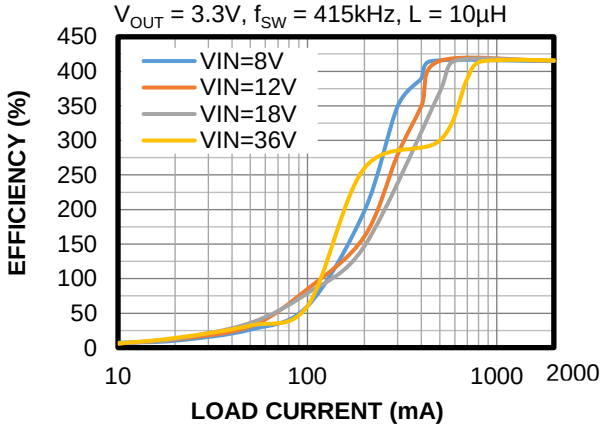
Switching Frequency vs. Load Current for 2000 Version

V_{OUT} = 5V, f_{SW} = 415kHz, L = 10µH



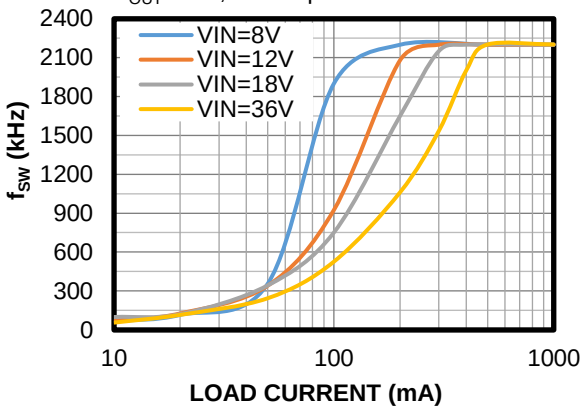
Switching Frequency vs. Load Current for 2000 Version

V_{OUT} = 3.3V, f_{SW} = 415kHz, L = 10µH



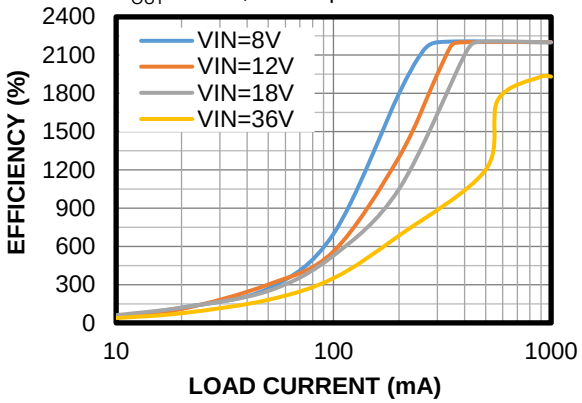
Switching Frequency vs. Load Current for 1000/0000 Versions

V_{OUT} = 5V, L = 5.6µH



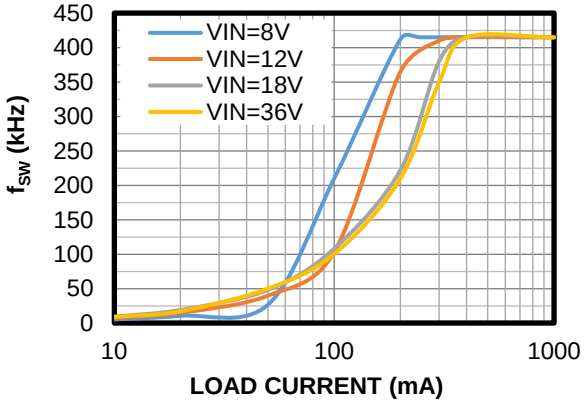
Switching Frequency vs. Load Current for 1000/0000 Versions

V_{OUT} = 3.3V, L = 5.6µH



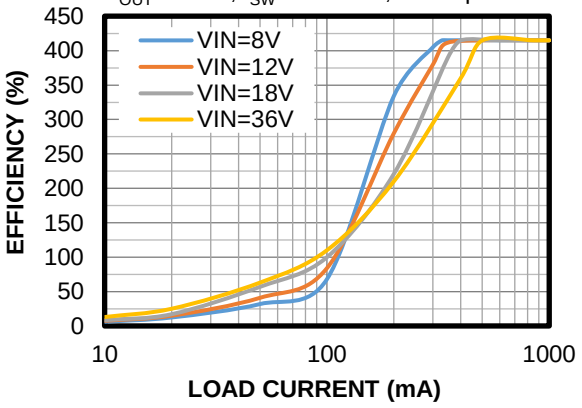
Switching Frequency vs. Load Current for 1000/0000 Versions

V_{OUT} = 5V, f_{SW} = 415kHz, L = 22µH



Switching Frequency vs. Load Current for 1000/0000 Versions

V_{OUT} = 3.3V, f_{SW} = 415kHz, L = 22µH

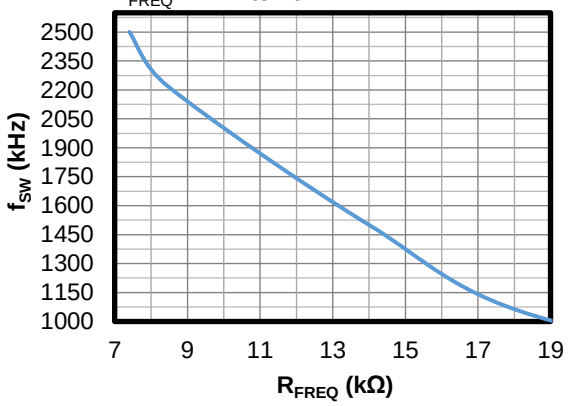


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

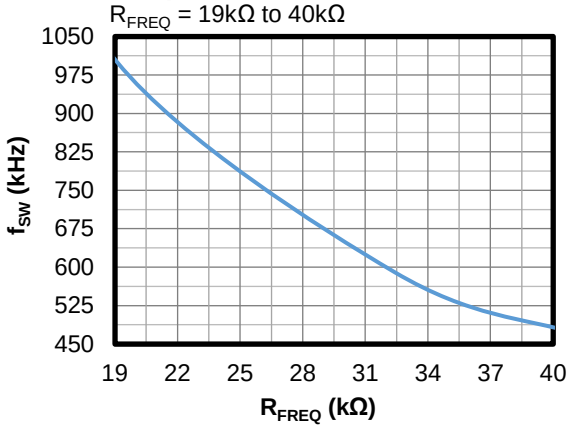
Switching Frequency vs. Frequency Resistor

R_{FREQ} = 7kΩ to 19kΩ



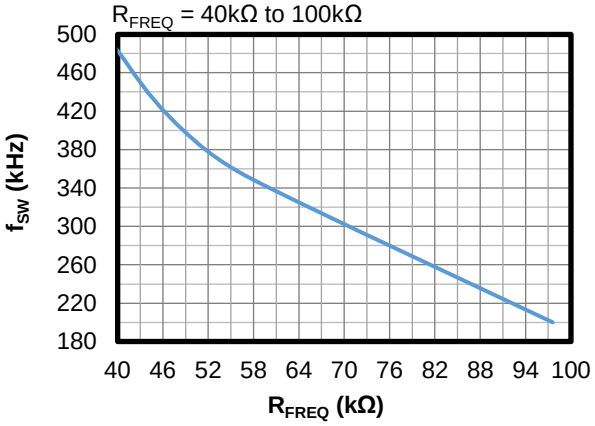
Switching Frequency vs. Frequency Resistor

R_{FREQ} = 19kΩ to 40kΩ



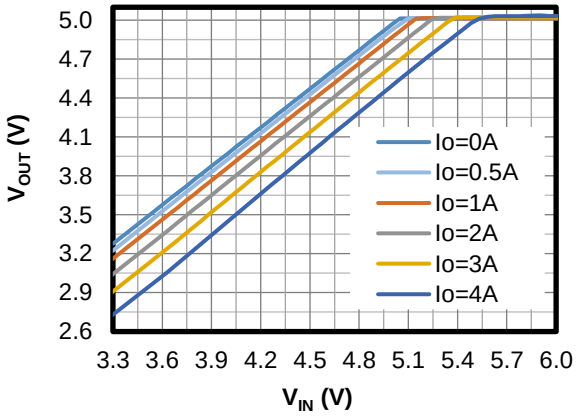
Switching Frequency vs. Frequency Resistor

R_{FREQ} = 40kΩ to 100kΩ



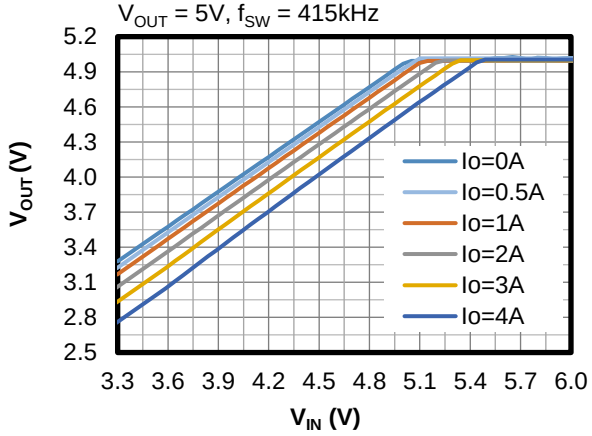
Low-Dropout Mode

V_{OUT} = 5V, f_{SW} = 2.2MHz



Low-Dropout Mode

V_{OUT} = 5V, f_{SW} = 415kHz

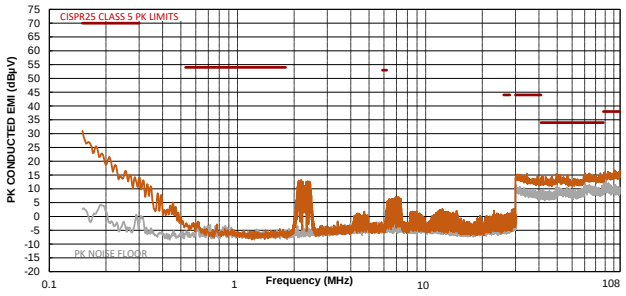


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.(13)

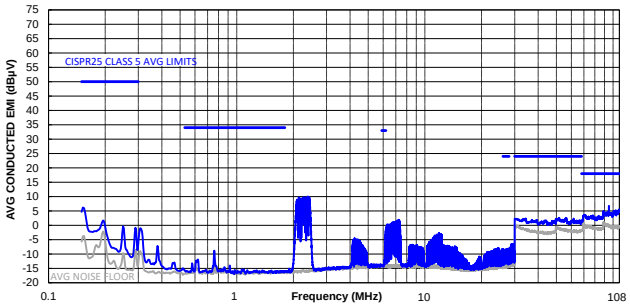
CISPR 25 Class 5 Peak Conducted Emissions

150kHz to 108MHz



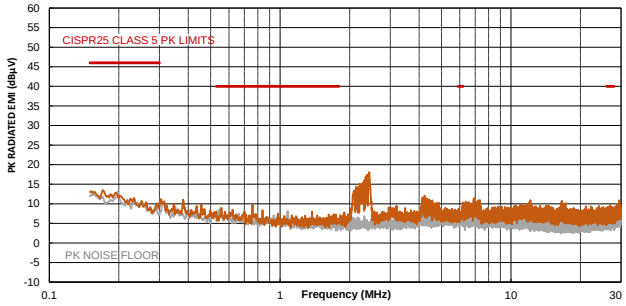
CISPR 25 Class 5 Average Conducted Emissions

150kHz to 108MHz



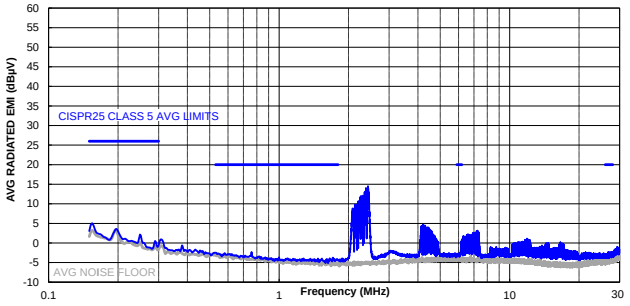
CISPR 25 Class 5 Peak Radiated Emissions

150kHz to 30MHz



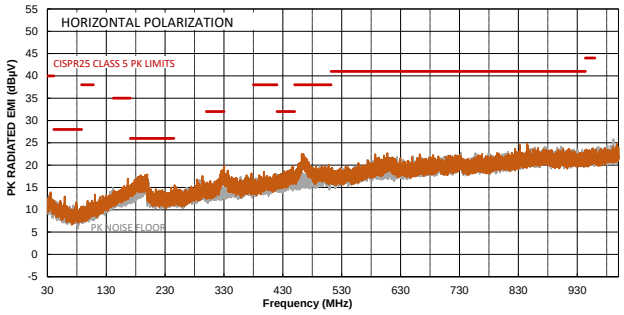
CISPR 25 Class 5 Average Radiated Emissions

150kHz to 30MHz



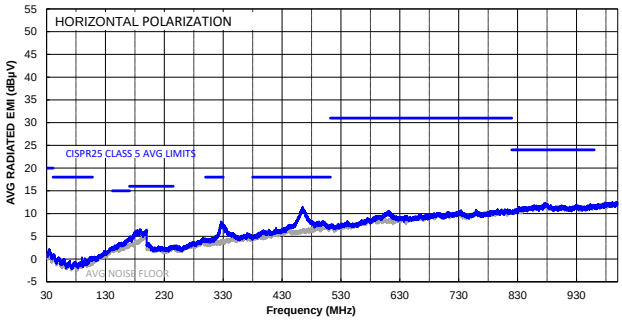
CISPR 25 Class 5 Peak Radiated Emissions

Horizontal, 30MHz to 1GHz



CISPR 25 Class 5 Average Radiated Emissions

Horizontal, 30MHz to 1GHz

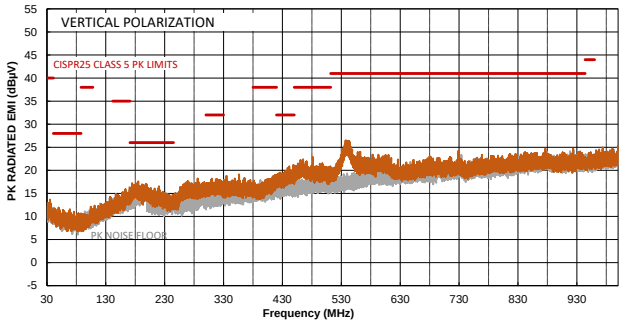


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.(13)

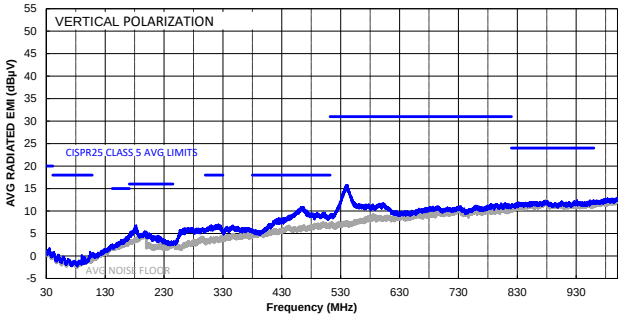
CISPR 25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 1GHz



CISPR 25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 1GHz



Note:

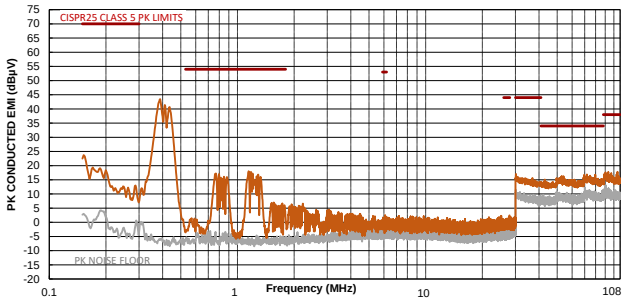
13) The EMC test results are based on the typical application circuit with EMI filters (see Figure 50 on page 94).

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.(14)

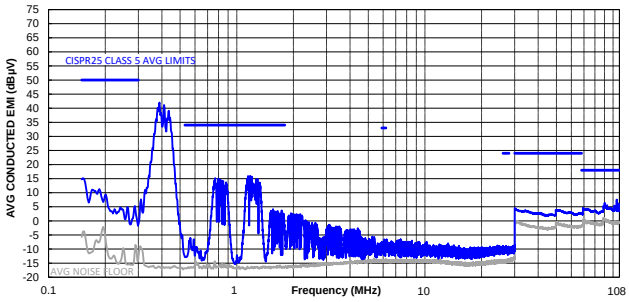
CISPR 25 Class 5 Peak Conducted Emissions

150kHz to 108MHz



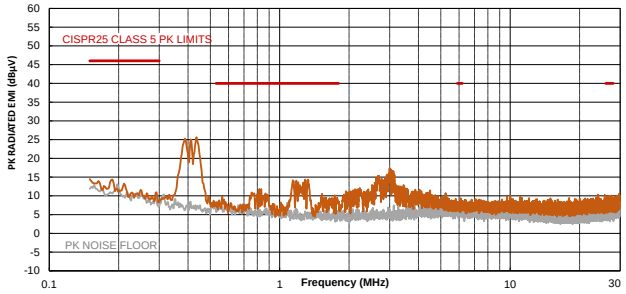
CISPR 25 Class 5 Average Conducted Emissions

150kHz to 108MHz



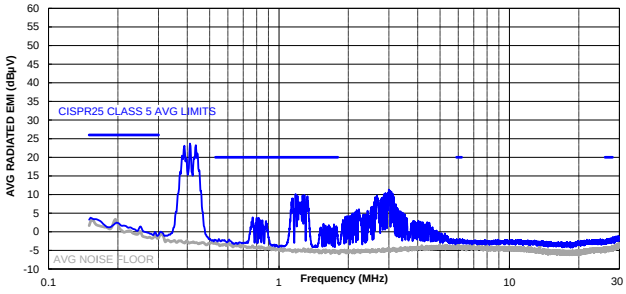
CISPR 25 Class 5 Peak Radiated Emissions

150kHz to 30MHz



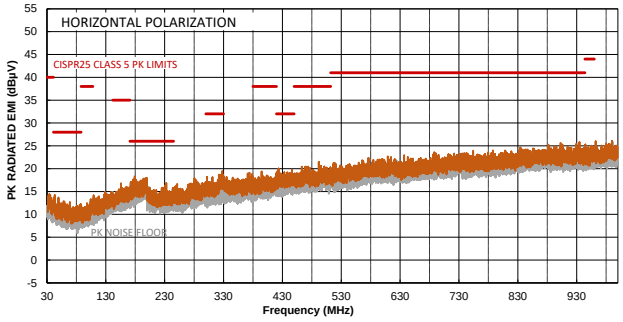
CISPR 25 Class 5 Average Radiated Emissions

150kHz to 30MHz



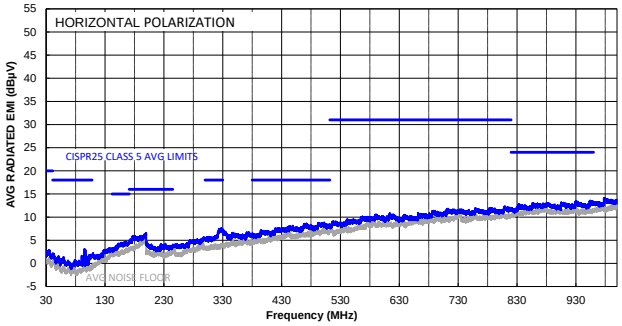
CISPR 25 Class 5 Peak Radiated Emissions

Horizontal, 30MHz to 1GHz



CISPR 25 Class 5 Average Radiated Emissions

Horizontal, 30MHz to 1GHz

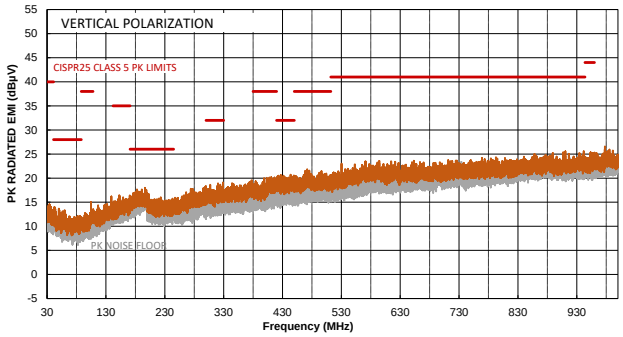


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.(14)

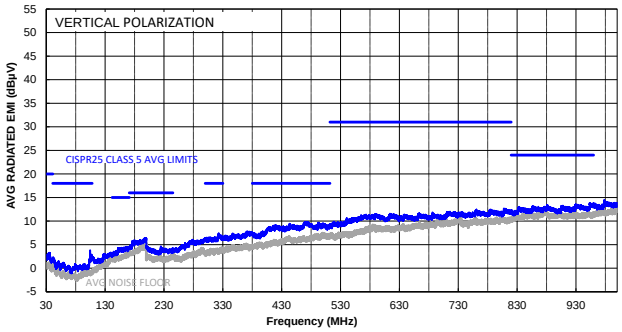
CISPR 25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 1GHz



CISPR 25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 1GHz



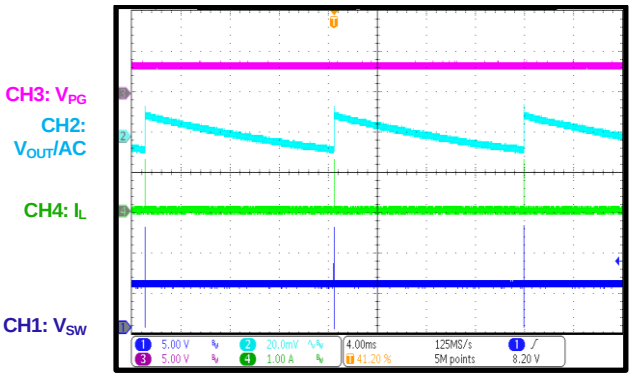
Note:

14) The EMC test results are based on the typical application circuit with EMI filters (see Figure 51 on page 95).

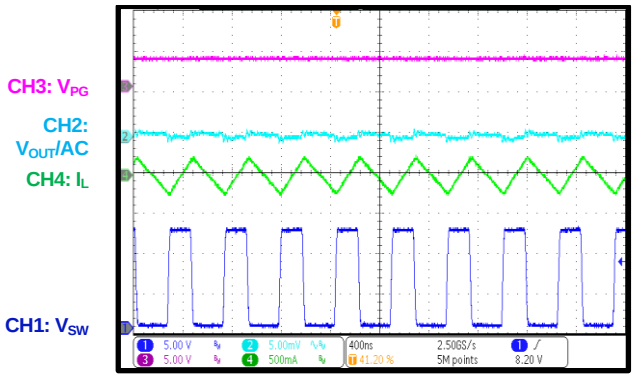
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

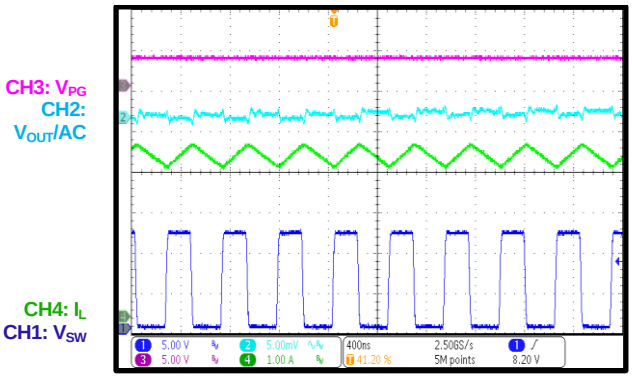
Steady State
AAM mode, I_{OUT} = 0A



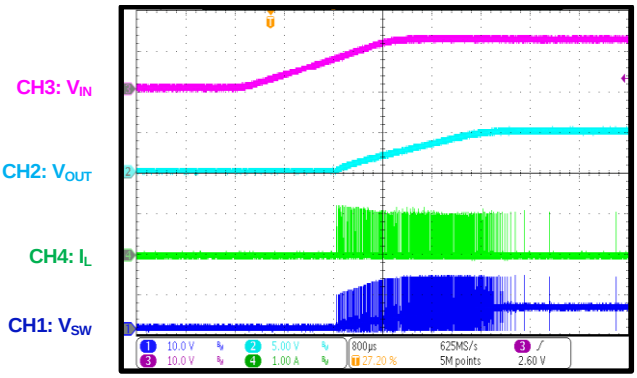
Steady State
FCCM, I_{OUT} = 0A



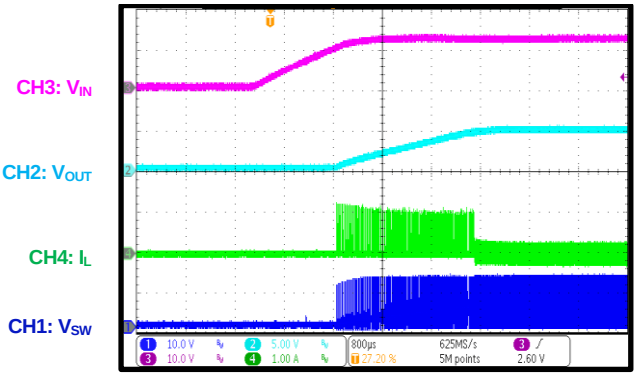
Steady State
I_{OUT} = 4A



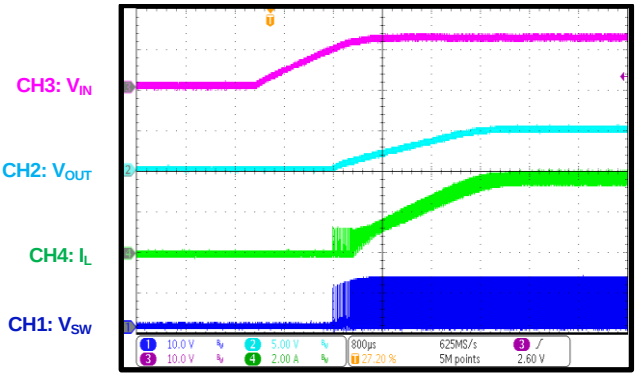
Start-Up through VIN
AAM mode, I_{OUT} = 0A



Start-Up through VIN
FCCM, I_{OUT} = 0A



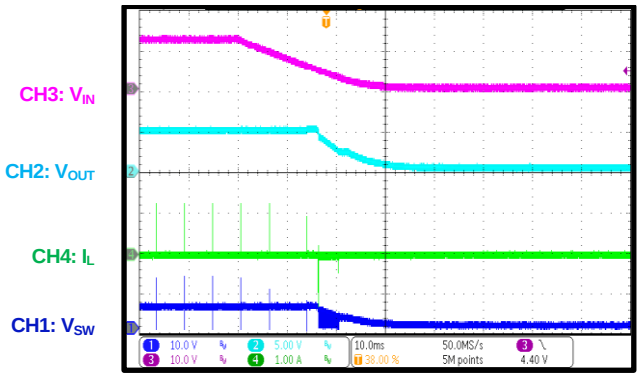
Start-Up through VIN
I_{OUT} = 4A



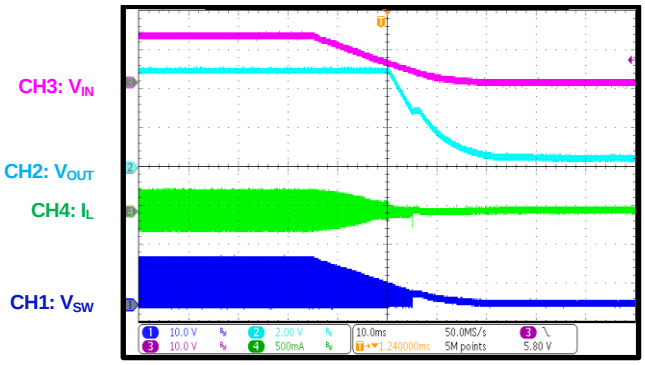
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

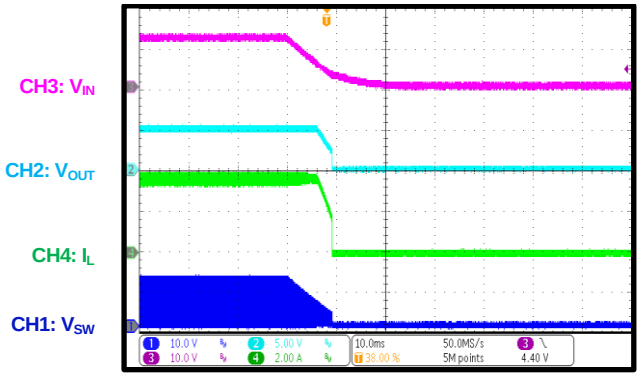
Shutdown through VIN
AAM mode, I_{OUT} = 0A



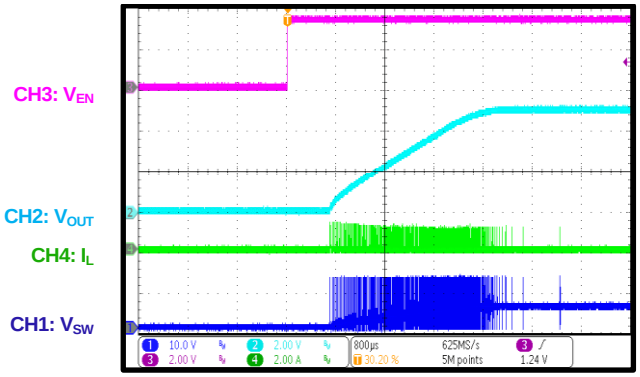
Shutdown through VIN
FCCM, I_{OUT} = 0A



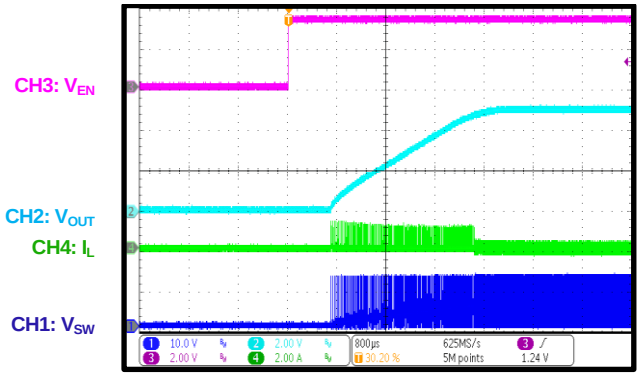
Shutdown through VIN
I_{OUT} = 4A



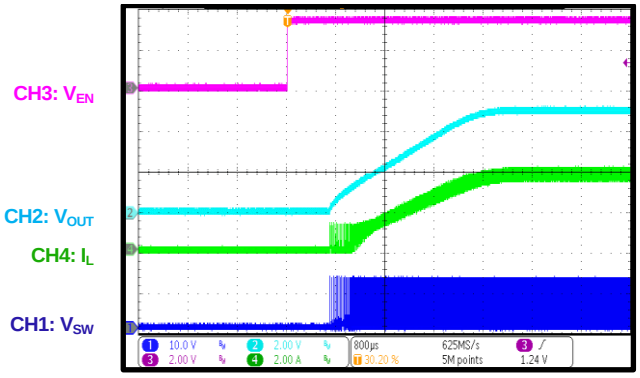
Start-Up through EN
AAM mode, I_{OUT} = 0A



Start-Up through EN
FCCM, I_{OUT} = 0A



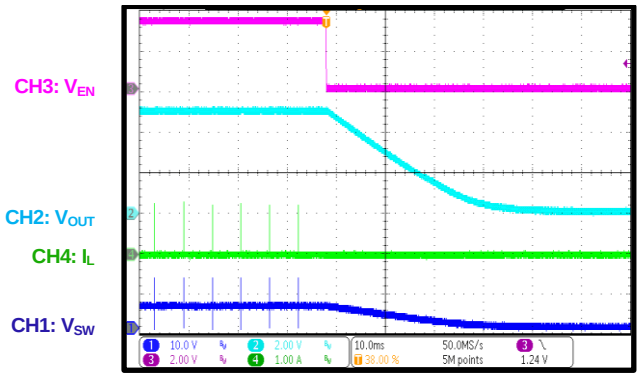
Start-Up through EN
I_{OUT} = 4A



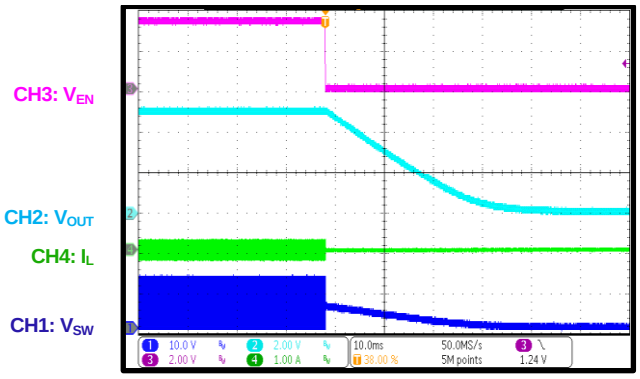
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

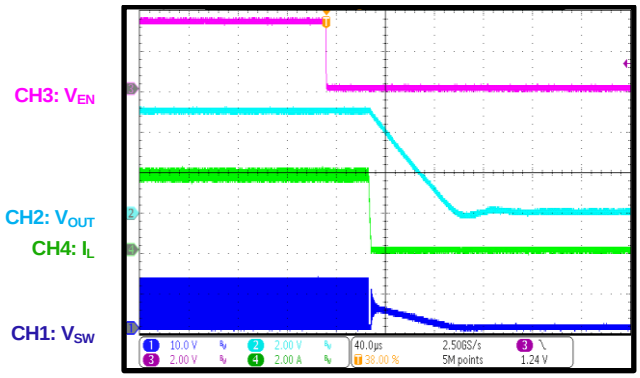
Shutdown through EN
AAM mode, I_{OUT} = 0A



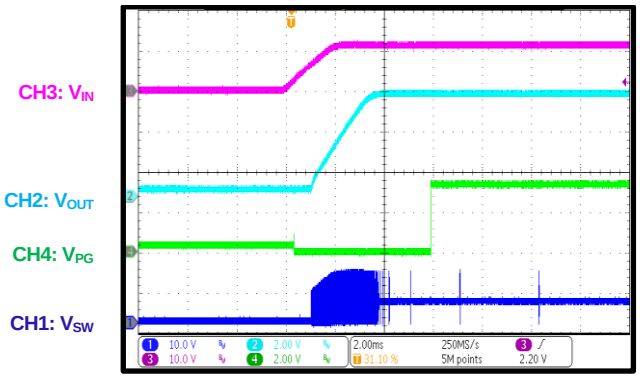
Shutdown through EN
FCCM, I_{OUT} = 0A



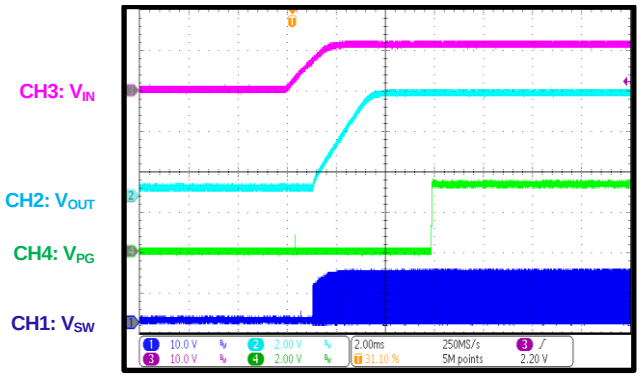
Shutdown through EN
I_{OUT} = 4A



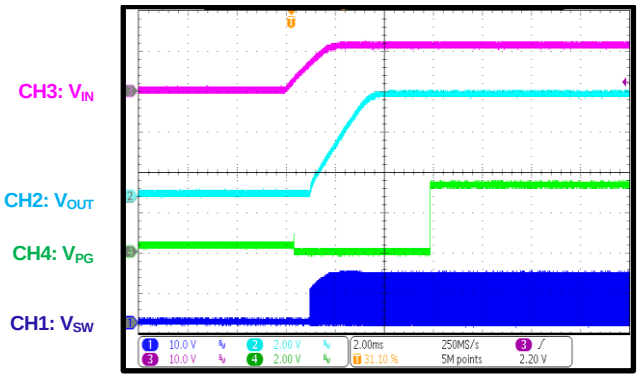
PG Start-Up through VIN
AAM mode, I_{OUT} = 0A



PG Start-Up through VIN
FCCM, I_{OUT} = 0A



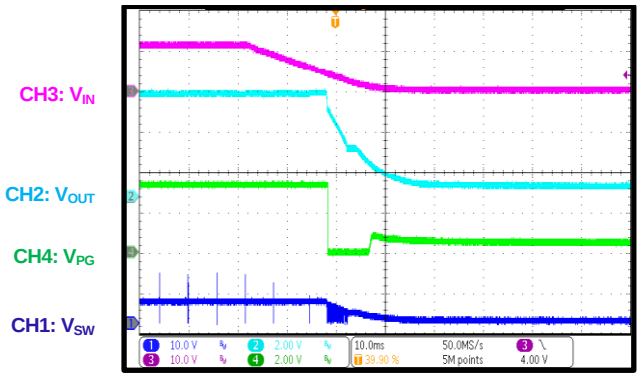
PG Start-Up through VIN
I_{OUT} = 4A



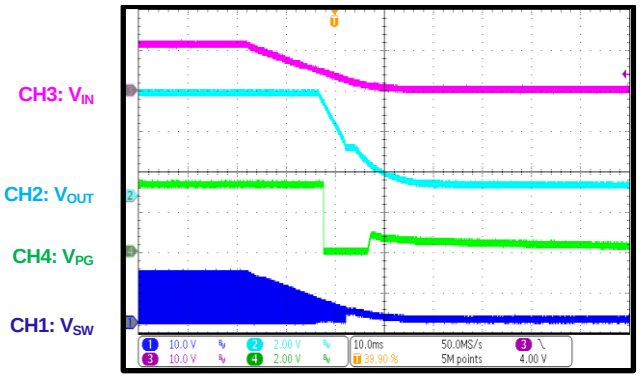
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

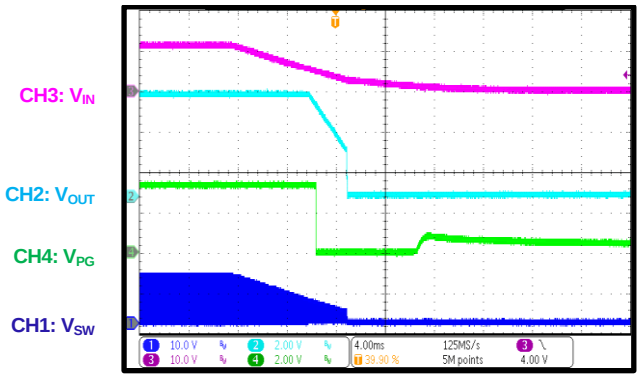
PG Shutdown through VIN
AAM mode, I_{OUT} = 0A



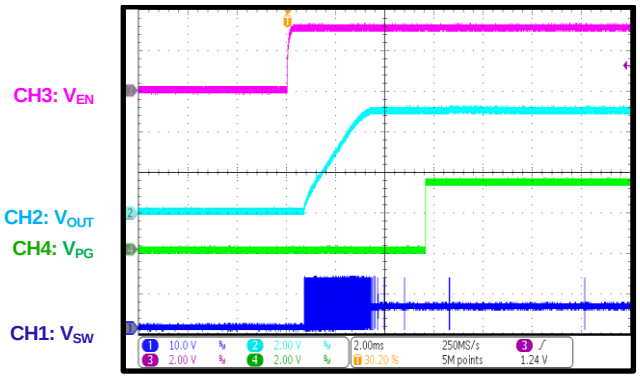
PG Shutdown through VIN
FCCM, I_{OUT} = 0A



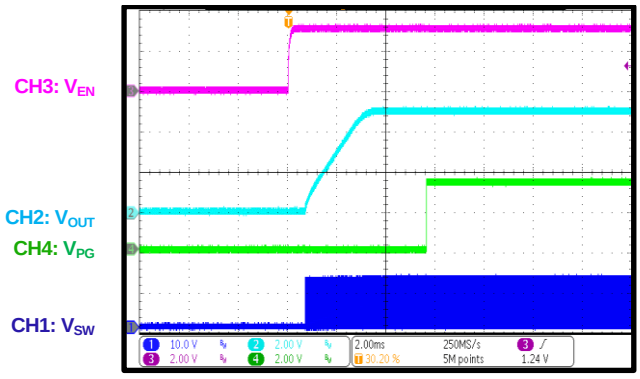
PG Shutdown through VIN
I_{OUT} = 4A



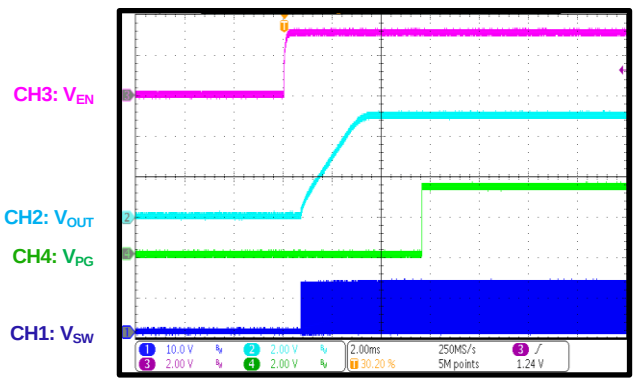
PG Start-Up through EN
AAM mode, I_{OUT} = 0A



PG Start-Up through EN
FCCM, I_{OUT} = 0A



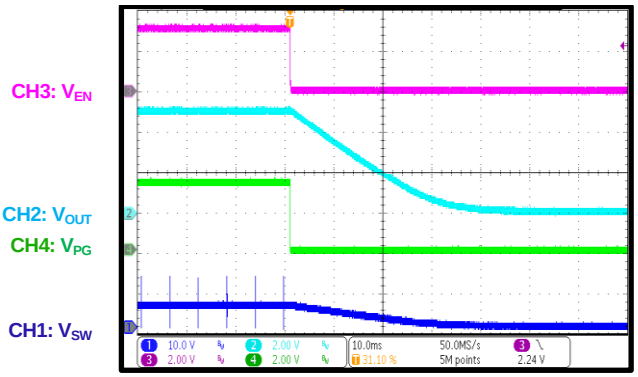
PG Start-Up through EN
I_{OUT} = 4A



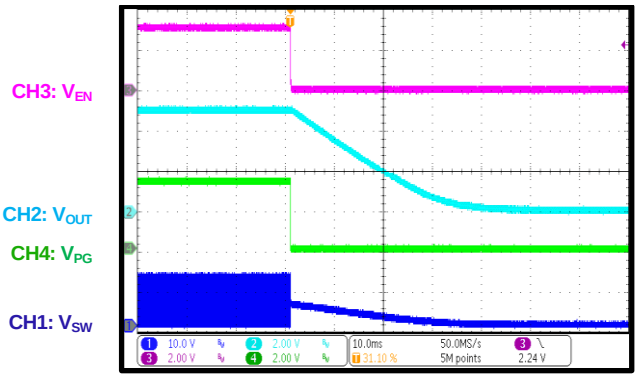
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

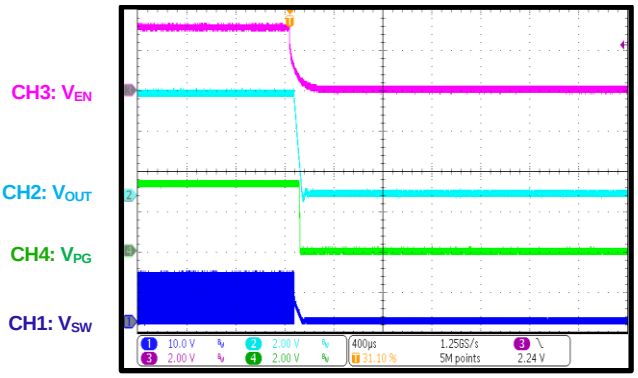
PG Shutdown through EN
AAM mode, I_{OUT} = 0A



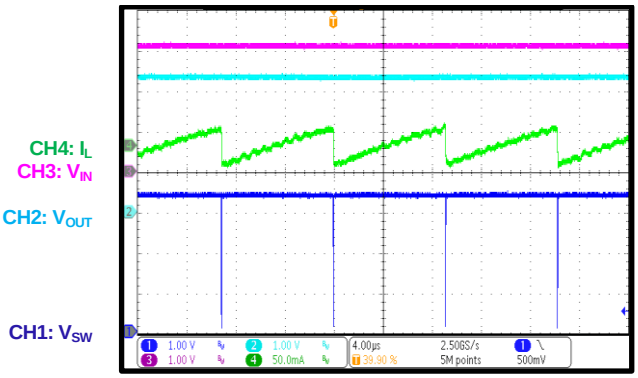
PG Shutdown through EN
FCCM, I_{OUT} = 0A



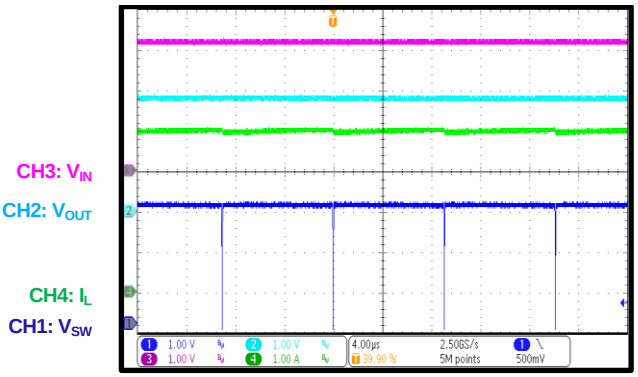
PG Shutdown through EN
I_{OUT} = 4A



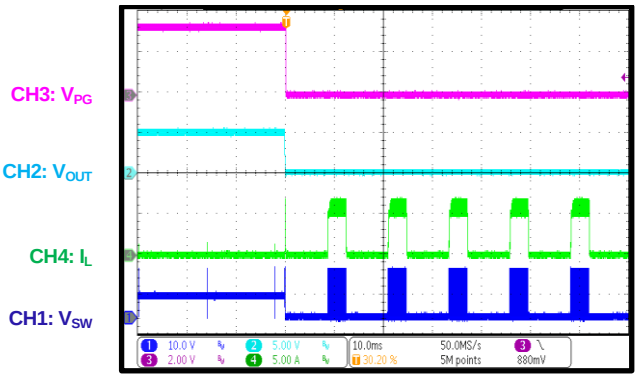
Low-Dropout Mode
I_{OUT} = 0A, V_{IN} = 3.3V



Low-Dropout Mode
I_{OUT} = 4A, V_{IN} = 3.3V



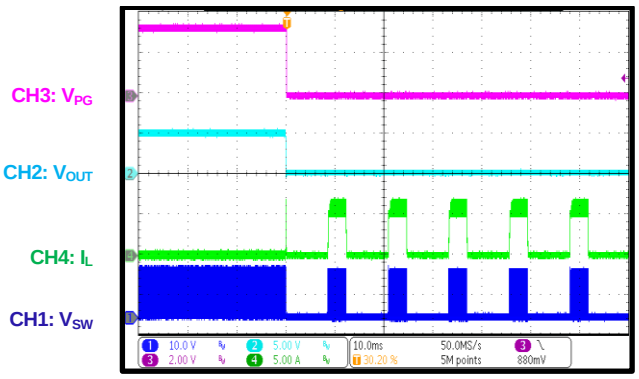
SCP Entry
AAM mode, I_{OUT} = 0A



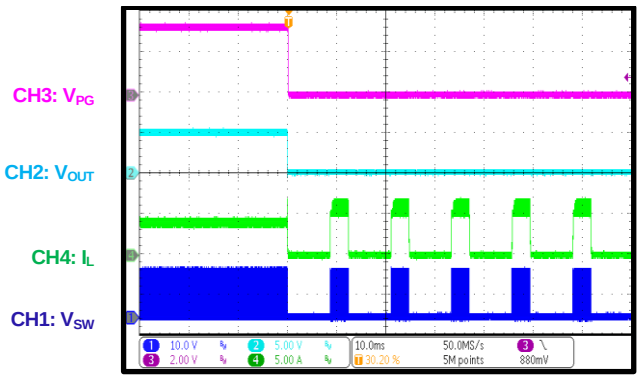
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

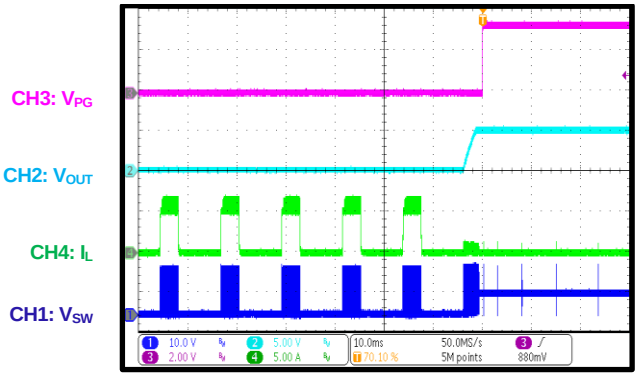
SCP Entry
FCCM, I_{OUT} = 0A



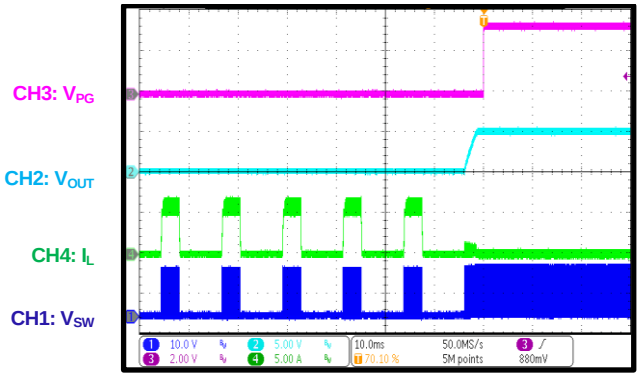
SCP Entry
I_{OUT} = 4A



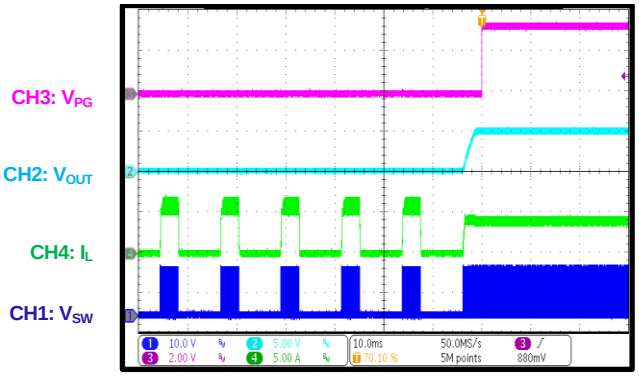
SCP Recovery
AAM mode, I_{OUT} = 0A



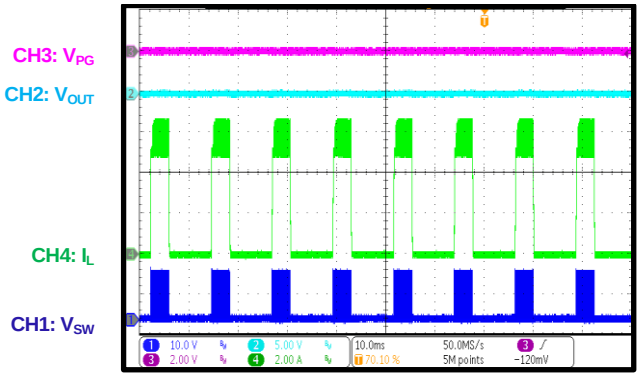
SCP Recovery
FCCM, I_{OUT} = 0A



SCP Recovery
I_{OUT} = 4A



SCP Steady State
I_{OUT} = 0A

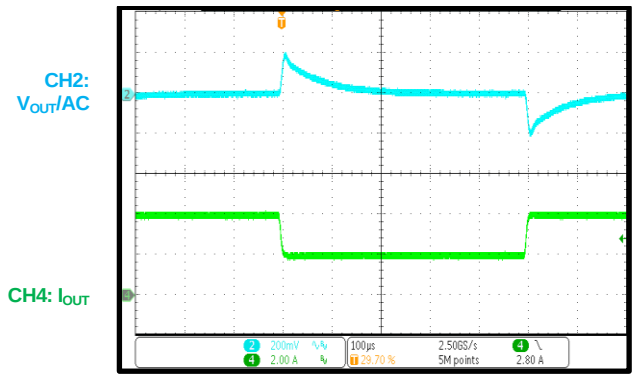


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

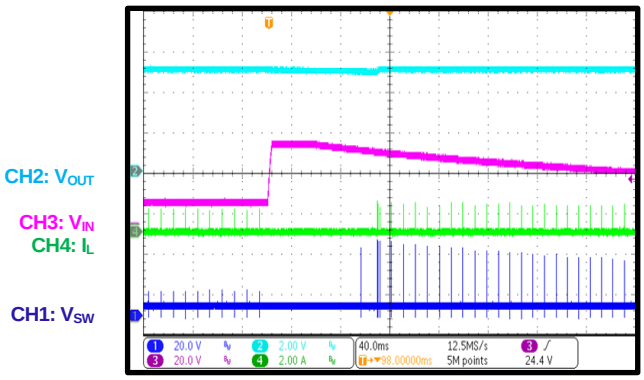
Load Transient

I_{OUT} = 2A to 4A, 1.6A/µs



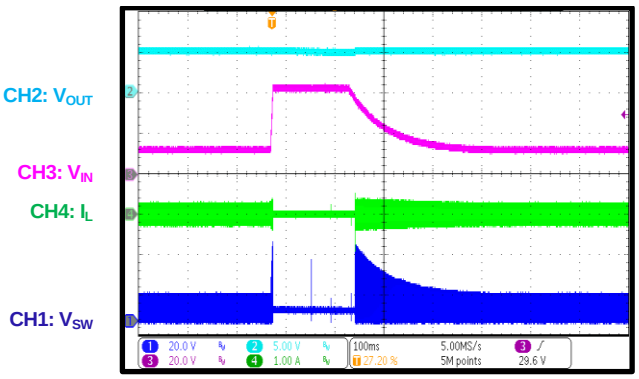
Load Dump

V_{IN} = 12V to 40V, AAM mode, I_{OUT} = 0A



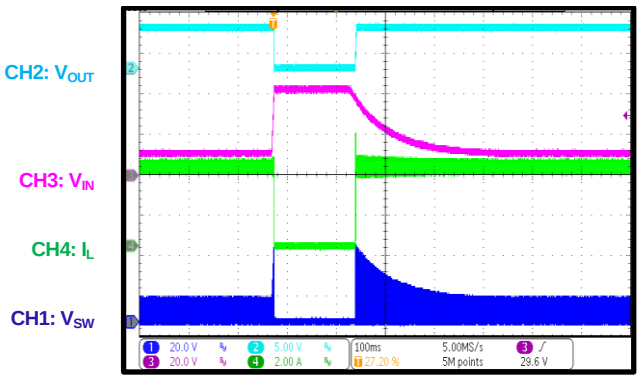
Load Dump

V_{IN} = 12V to 40V, FCCM, I_{OUT} = 0A



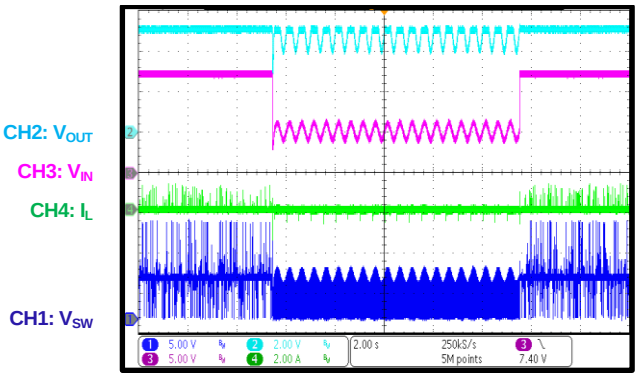
Load Dump

V_{IN} = 12V to 40V, I_{OUT} = 4A



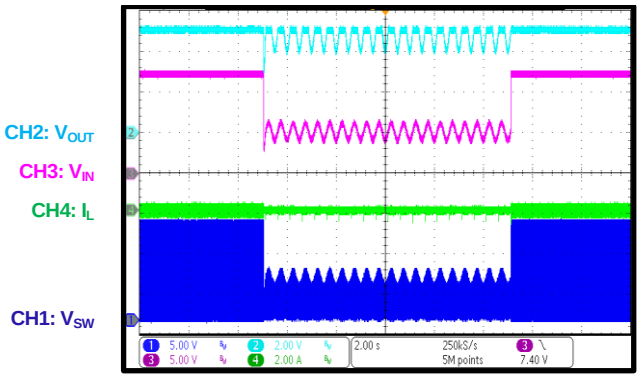
Cold Crank

AAM mode, I_{OUT} = 0A



Cold Crank

FCCM, I_{OUT} = 0A

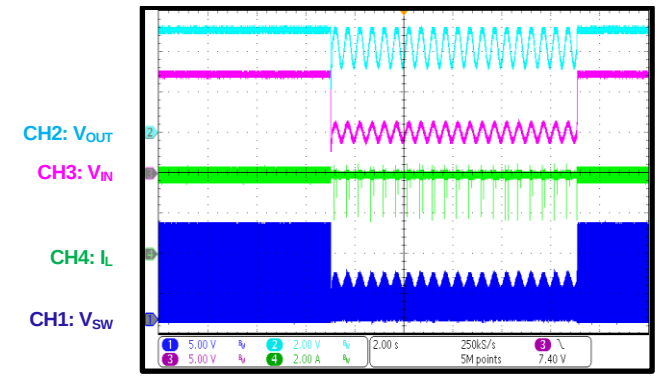


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

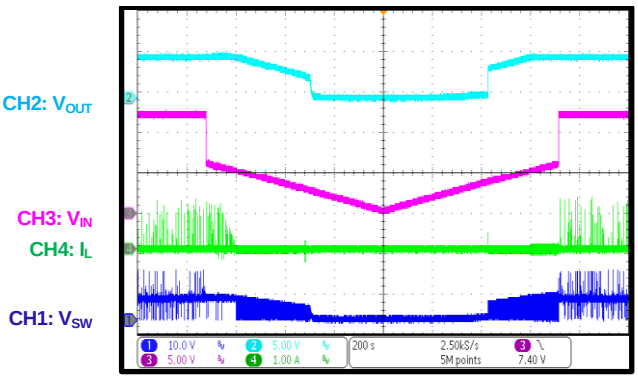
Cold Crank

I_{OUT} = 4A



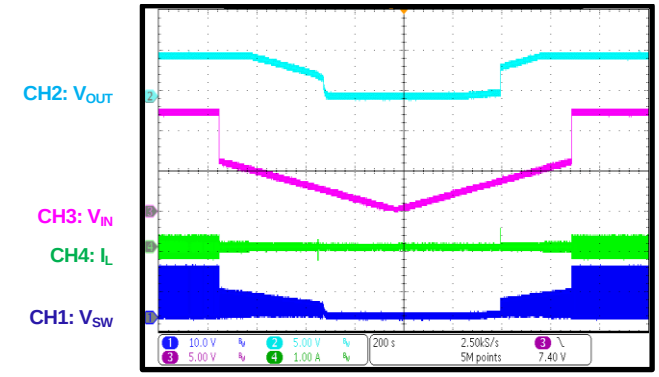
V_{IN} Ramping Down and Up

V_{IN} = 6V to 0V, 0.5V/min, AAM mode, I_{OUT} = 0A



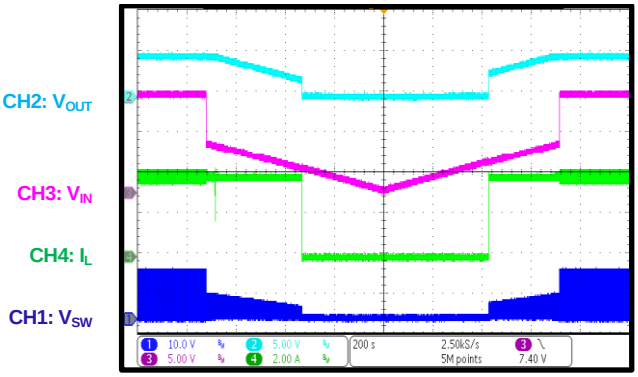
V_{IN} Ramping Down and Up

V_{IN} = 6V to 0V, 0.5V/min, FCCM, I_{OUT} = 0A



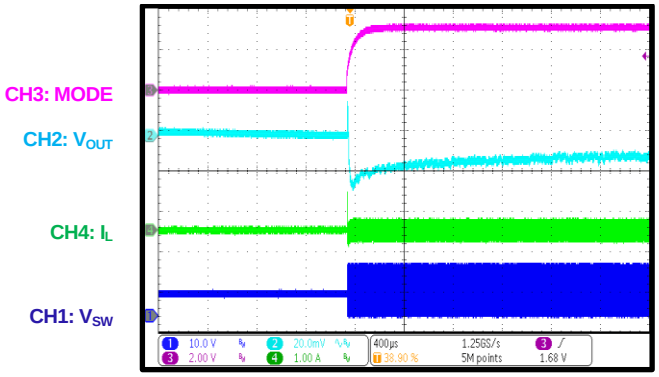
V_{IN} Ramping Down and Up

V_{IN} = 6V to 0V, 0.5V/min, I_{OUT} = 4A



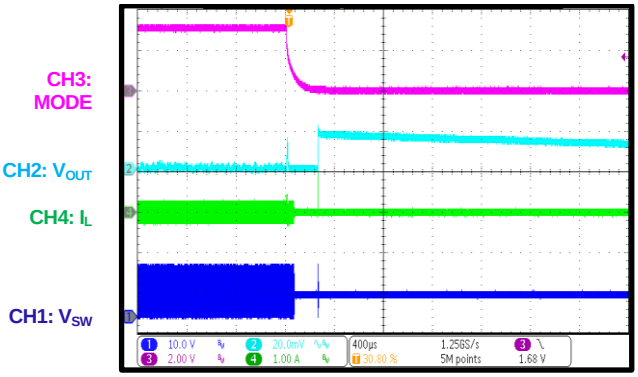
Mode Transient

AAM mode to FCCM, I_{OUT} = 0A



Mode Transient

FCCM to AAM mode, I_{OUT} = 0A

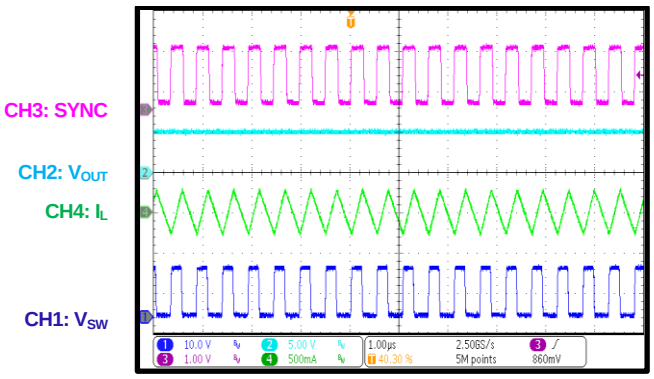


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

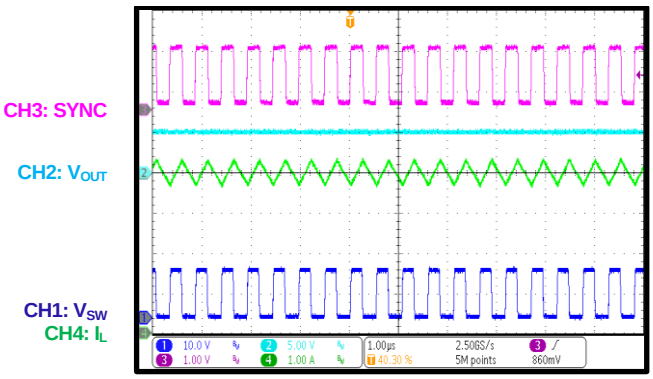
SYNC Function

f_{SYNC} = 1.9MHz, I_{OUT} = 0A



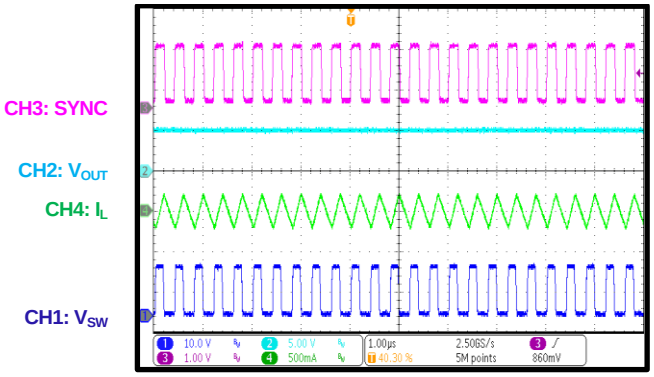
SYNC Function

f_{SYNC} = 1.9MHz, I_{OUT} = 4A



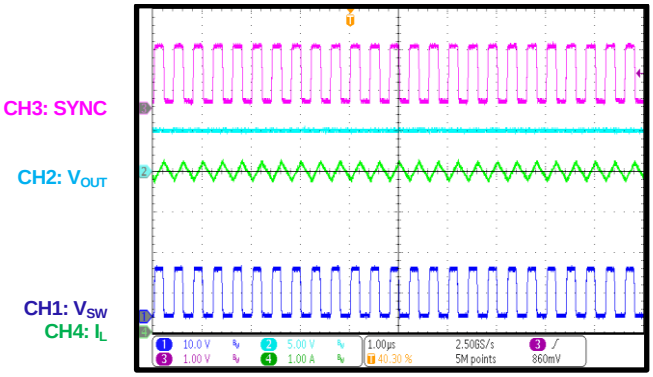
SYNC Function

f_{SYNC} = 2.5MHz, I_{OUT} = 0A



SYNC Function

f_{SYNC} = 2.5MHz, I_{OUT} = 4A



FUNCTIONAL BLOCK DIAGRAMS

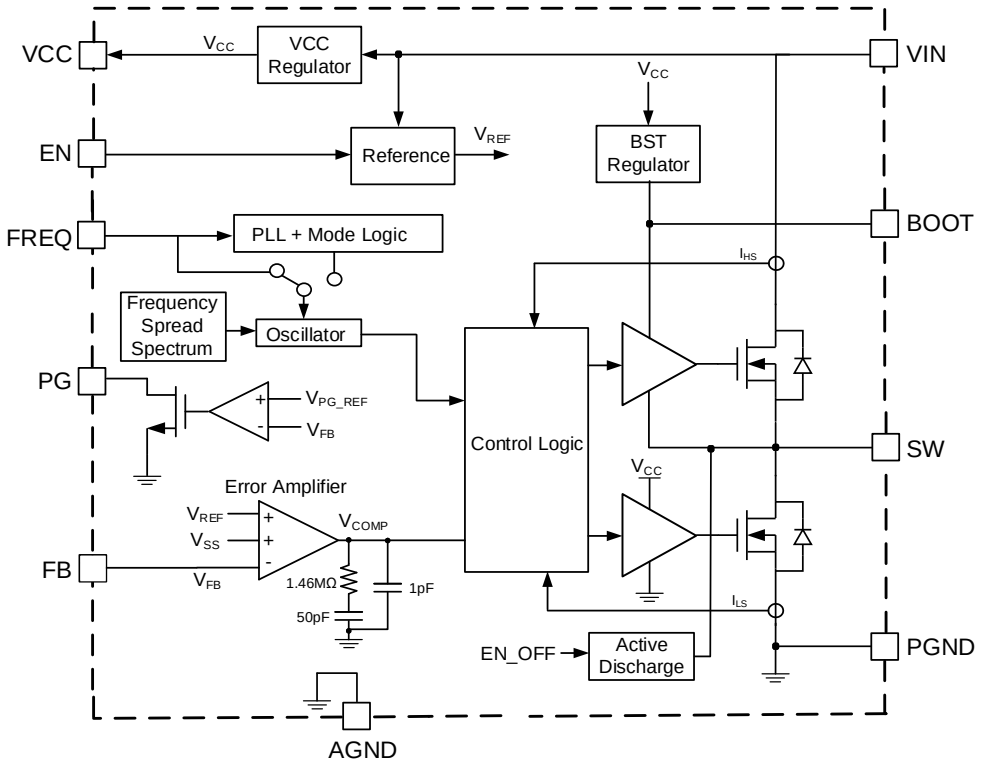


Figure 5: Functional Block Diagram (Adjustable-Output Version)

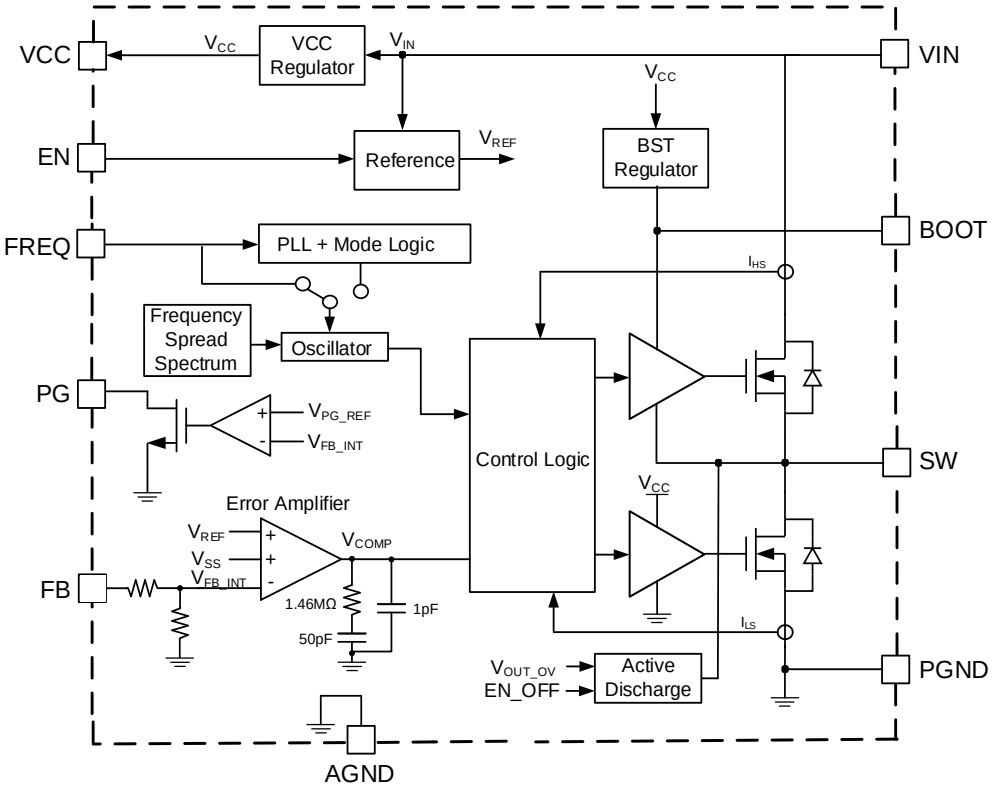


Figure 6: Functional Block Diagram (Fixed-Output Version)

FUNCTIONAL BLOCK DIAGRAMS *(continued)*

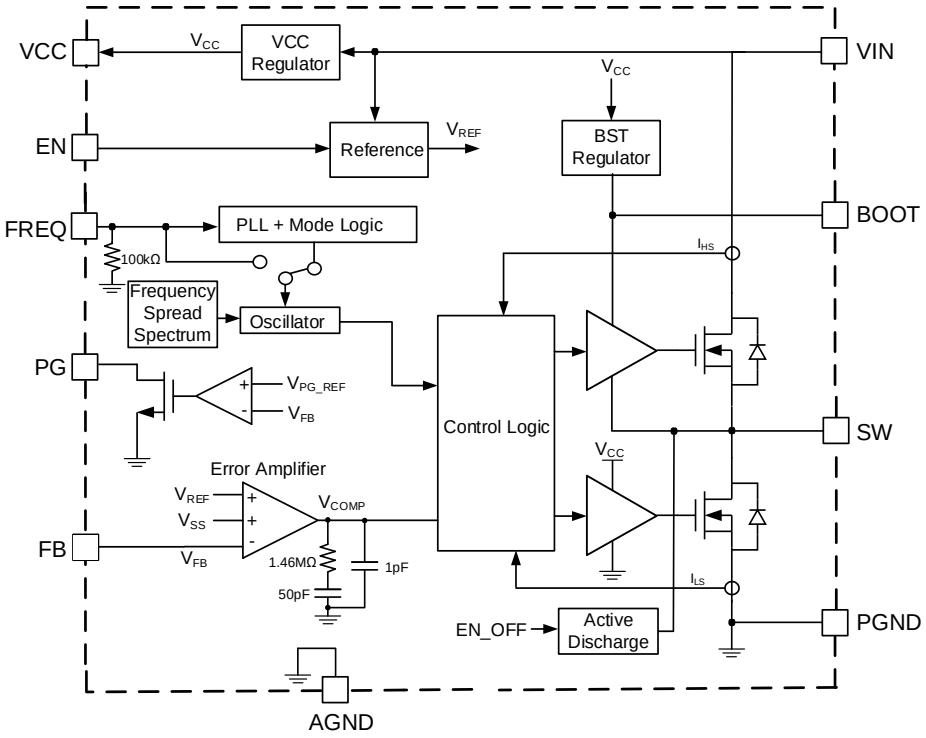


Figure 7: Functional Block Diagram (FREQ as SYNC/MODE, Adjustable-Output Version)

TIMING SEQUENCE DIAGRAM

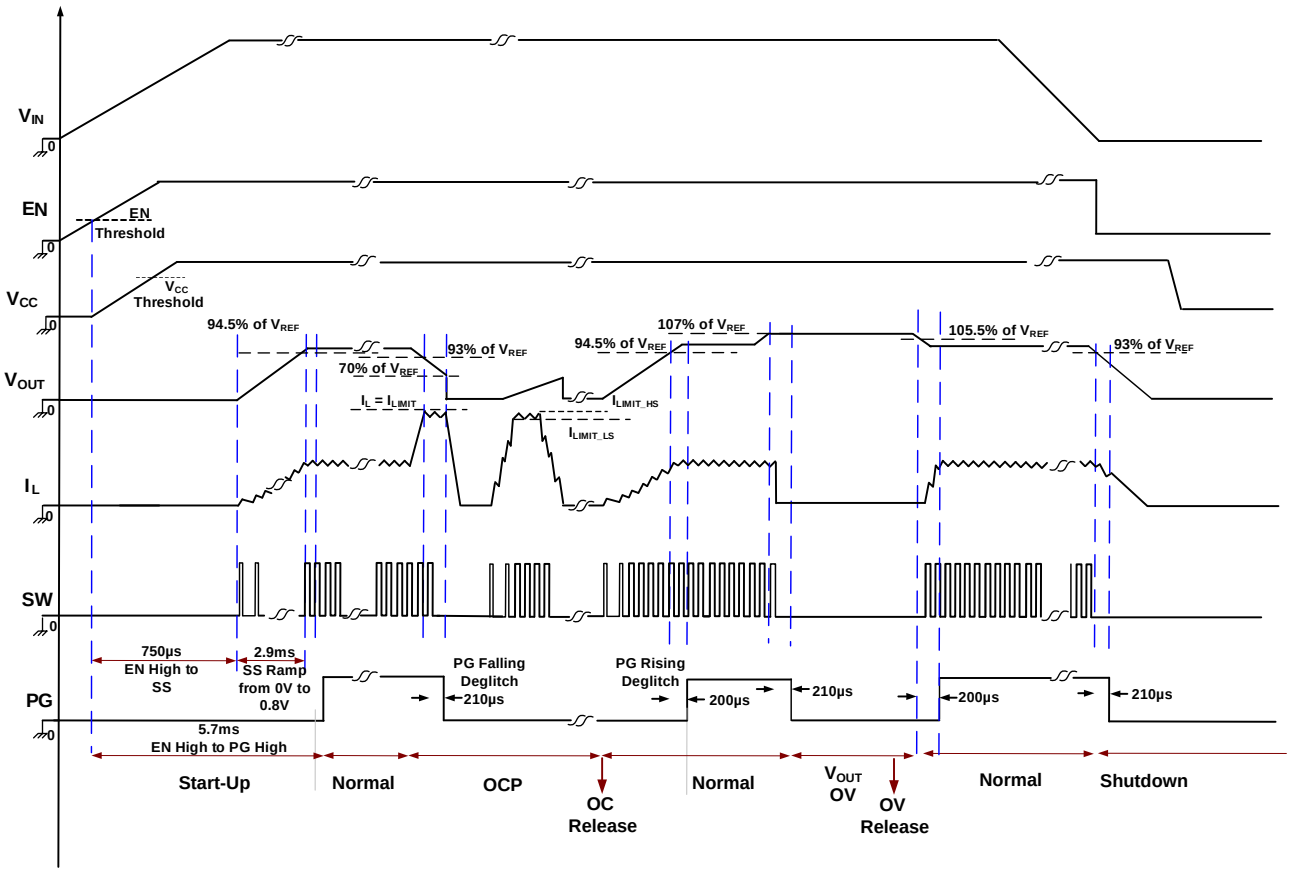


Figure 8: Timing Sequence Diagram

OPERATION

The MPQ4334 is a synchronous, step-down switching converter with integrated internal high-side and low-side power MOSFETs (HS-FETs and LS-FETs, respectively). The device provides 0.5A to 4A of continuous, highly efficient output current (I_{OUT}) with peak current mode control.

The device features a wide input voltage range, (V_{IN}) configurable 200kHz to 2.5MHz switching frequency (f_{SW}), internal soft start (SS), and precision current limiting. The MPQ4334's low operational quiescent current (I_Q) makes it well-suited for battery-powered applications.

Pulse-Width Modulation (PWM) Control

At moderate to high output currents, the MPQ4334 operates with fixed-frequency, peak current mode control to regulate the output voltage (V_{OUT}). A pulse-width modulation (PWM) cycle is initiated by the internal clock. At the rising edge of the clock, the HS-FET turns on and remains on until the control signal reaches the value set by the internal COMP voltage (V_{COMP}). If the control signal reaches V_{COMP} within 55ns, the HS-FET remains on for at least 55ns due to the minimum on time.

When the HS-FET is off, the LS-FET turns on immediately. When the part works in forced continuous conduction mode (FCCM), the LS-FET stays on until the next cycle starts. When the part works in advanced asynchronous modulation (AAM) mode, the LS-FET also turns off once the inductor current (I_L) drops below the zero-current detection (ZCD) threshold. The LS-FET remains on for at least the minimum off time (45ns) before the next cycle starts.

If the current in the HS-FET cannot reach the value set by COMP within one PWM period, the HS-FET remains on and skips a turn-off operation. The HS-FET is forced off until it reaches the value set by COMP, or its 10µs maximum on time is reached. This operation mode extends the duty cycle, which achieves a low dropout when V_{IN} is almost equal to V_{OUT}.

The MPQ4334 has a mechanism to prevent overshoot when V_{IN} recovers from low-dropout (LDO) mode. When the part works in LDO mode, the error amplifier's (EA's) gain becomes larger, which can make V_{COMP} quickly decrease and optimize the V_{OUT} overshoot when exiting LDO dropout mode. Even if the part exits LDO mode with a very fast V_{IN} rising speed, the I_L spike and V_{OUT} overshoot are small.

Advanced Asynchronous Modulation (AAM) Mode and Forced Continuous Conduction Mode (FCCM)

When the value of "Z" in the four-digit code "XXYZ" is "0" or "3", or if it is "1," "2," "4," "5," or "8" and the FREQ pin is connected to AGND or floating, the MPQ4334 works in AAM mode to optimize efficiency under light-load and no-load conditions (see Table 1 on page 3).

When I_L approaches 0A under light loads, the MPQ4334 first initiates asynchronous operation. If the load decreases further and V_{COMP} drops below the set value, the MPQ4334 enters AAM mode (see Figure 9).

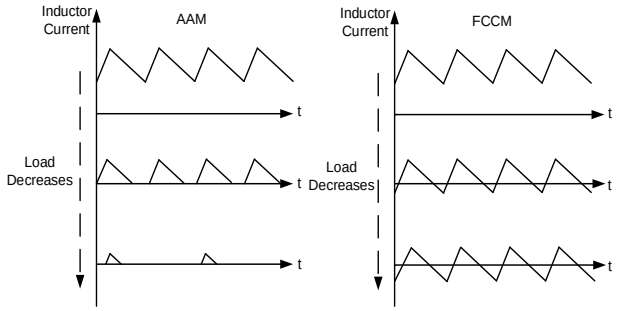


Figure 9: AAM Mode and FCCM

In AAM mode, the internal clock is reset every time V_{COMP} crosses the set value, and the crossover time is used as a benchmark for the next clock. When the load increases and V_{COMP} exceeds the set value, the device operates in continuous conduction mode (CCM) or discontinuous conduction mode (DCM) with a constant f_{SW}.

When the value of "Z" in the four-digit code "XXYZ" is "6" or 7," or is "1," "2," "4," or "5" and the FREQ pin is connected to a voltage above 1.4V, the MPQ4334 works in FCCM (see Table 1 on page 3). The device works with a fixed frequency across the no-load to full-load range (see Figure 9). The advantages of FCCM are its controllable frequency and lower V_{OUT} ripple under light loads.

Error Amplifier (EA)

The error amplifier (EA) compares the FB pin's voltage (V_{FB}) with the internal reference voltage (V_{REF}, 0.8V) and outputs a current proportional to the difference between the two values. This current is then used to charge the compensation network to form V_{COMP}, which controls the power MOSFET's duty cycle.

During normal operation, the minimum V_{COMP} is clamped at 0.9V, and the maximum V_{COMP} is clamped at 2V. The COMP node is internally pulled down to AGND in shutdown mode.

Frequency Spread Spectrum (FSS)

The MPQ4334 uses a 7.5kHz modulation frequency with a 128-step triangular profile to spread the internal f_{SW} across a 20% (±10%) window. The steps vary with the set f_{SW} to ensure that the exact f_{SW} steps cycle by cycle (see Figure 10).

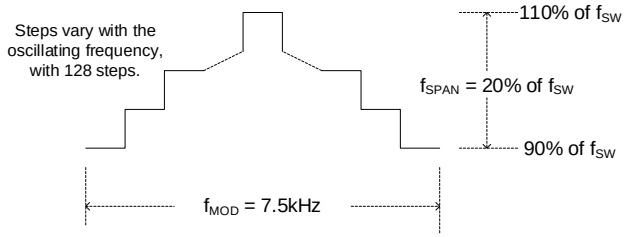


Figure 10: Frequency Spread Spectrum

The emission power of the fundamental f_{SW} and its harmonics is distributed into smaller pieces by creating side-bands when modulating f_{SW} with a triangular modulation waveform. This significantly reduces the amplitude of individual EMI spurs.

Soft Start (SS)

Soft start (SS) is implemented to prevent the converter's V_{OUT} from overshooting during start-up. The soft-start time (t_{SS}) is fixed internally.

When SS starts, the soft-start voltage (V_{SS}) rises from 0V to 1.2V with a specific slew rate. When V_{SS} is below the internal 0.8V reference voltage (V_{REF}), V_{SS} overrides V_{REF} and the EA uses V_{SS} as the reference. When V_{SS} exceeds V_{REF}, the EA uses V_{REF} as the reference.

During t_{SS}, the converter operates in AAM mode for smooth start-up regardless of the MODE setting.

When the IC is enabled by the EN pin, the internal regulator (VCC) starts, and the device is initialized. 0.75ms after EN goes high, the bandgap, oscillator, and control loop are ready. Then the part ramps to the target within 2.7ms. Once V_{OUT} reaches its regulated value, PG is pulled high after a 2.25ms delay. The total time from EN going high to PG going high is typically 5.7ms.

Start-Up and Shutdown

If both V_{IN} and EN exceed their appropriate thresholds, the chip starts up. The reference block starts first, generating a stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

When the internal supply rail is up, the internal circuits start to work. If BOOT does not reach its refresh rising threshold (about 2.4V), the LS-FET turns on to charge BOOT. The HS-FET stays off during this time. When the SS block is enabled, V_{OUT} starts to ramp up slowly. V_{OUT} smoothly reaches its target within 2.9ms.

Three events can shut down the chip: EN going low, V_{IN} falling below its under-voltage lockout (UVLO) threshold, and thermal shutdown. During shutdown, the signaling path is blocked first to avoid any fault triggering. Then V_{COMP} is pulled down and the floating driver works to disable the HS-FET.

Bootstrap Charging

The voltage between BOOT and SW ($V_{BOOT-SW}$) is regulated to about 3.3V by the dedicated internal bootstrap regulator. When $V_{BOOT-SW}$ is below its regulated value, an N-channel MOSFET pass transistor connected from VCC to BOOT turns on to charge the bootstrap capacitor (C_{BOOT}). The external circuit should provide enough voltage headroom to facilitate the charging. When the HS-FET is on, the BOOT voltage (V_{BOOT}) exceeds the VCC voltage (V_{CC}), so C_{BOOT} cannot be charged.

Under conditions with higher duty cycles, the time available for bootstrap charging is shorter, so C_{BOOT} may not be charged sufficiently. In this case, the external circuit has insufficient voltage and time to charge C_{BOOT}. External circuitry can be used to ensure that V_{BOOT} remains in the normal operating range.

If V_{BOOT} reaches its UVLO threshold, the HS-FET turns off and the LS-FET turns on with a minimum off time to refresh V_{BOOT} with the set f_{SW}.

Pre-Biased Start-Up

If V_{FB} exceeds V_{SS} during start-up, this means that the output has a pre-biased voltage. Neither the HS-FET nor LS-FET turn on until V_{SS} exceeds V_{FB}.

Peak and Valley Current Limit

Both the HS-FET and LS-FET have cycle-by-cycle current-limit protection. When I_L reaches the high-side (HS) peak current limit while the HS-FET is on, the HS-FET is forced off immediately to prevent the current from rising further. Then the LS-FET turns on until I_L drops below the valley current limit.

When the LS-FET is on, the next clock's rising edge is held until I_L drops below the low-side (LS) valley current limit. Then I_L can drop to a sufficiently low value when the HS-FET turns on again. This current limit scheme prevents current runaway if an overload or short-circuit event occurs.

Reverse-Current Limit

The reverse current direction is from SW to the PGND node. The reverse current limit ($I_{LIMIT\_REVERSE}$) threshold is 3A. Once I_L reaches the $I_{LIMIT\_REVERSE}$, the LS-FET immediately turns off and the HS-FET turns on. After the control signal reaches V_{COMP}, the HS-FET turns off and the LS-FET turns on again. The current limit prevents the negative current from dropping too low and potentially damaging the components.

Short-Circuit Protection (SCP)

If the output is shorted to ground, and V_{OUT} drops below 70% of its nominal output, the MPQ4334 stop switching and begins discharging V_{SS}. Once V_{SS} is fully discharged, the device restarts with a full SS. This hiccup process repeats until the fault is removed.

V_{IN} Over-Voltage Protection (OVP)

If V_{IN} exceeds its over-voltage (OV) rising threshold (typically 38.5V), the MPQ4334 stops switching. Once V_{IN} drops below the OV falling threshold (typically 37.5V), the device restarts with SS and resumes normal operation.

V_{IN} over-voltage protection (OVP) has a 30µs deglitch time to avoid mistriggering.

Output Over-Voltage Protection (OVP) and Discharge

In AAM mode, the MPQ4334 stops switching when V_{OUT} exceeds its nominal value.

In FCCM, the MPQ4334 stops switching if V_{OUT} exceeds 107% of its nominal regulation value.

When V_{OUT} exceeds 107% of its nominal regulation value, then an internal 100Ω discharge path (with an 8mA saturation current) from SW to PGND is activated to discharge V_{OUT}. For FCCM, the part resumes switching once V_{OUT} drops back to 105.5% of its nominal value, and then the discharge path is disabled. For AAM mode, the discharge path remains disabled when V_{OUT} drops back to 105.5% of its nominal value, and resumes switching only when V_{OUT} drops below its nominal value.

The V_{OUT} discharge path is also activated if EN shutdown occurs and V_{IN} exceeds its UVLO, regardless of whether the device is a fixed-output version or an adjustable-output version.

Thermal Shutdown

Thermal shutdown is implemented to prevent the chip from thermal runaway. If the silicon die temperature exceeds its upper threshold (about 175°C), the device shuts down the power MOSFETs. Once the temperature drops below its lower threshold (about 155°C), thermal shutdown is removed, and the chip is restarts with SS and resumes normal operation.

APPLICATION INFORMATION

Figure 11 shows the MPQ4334's typical application circuit.

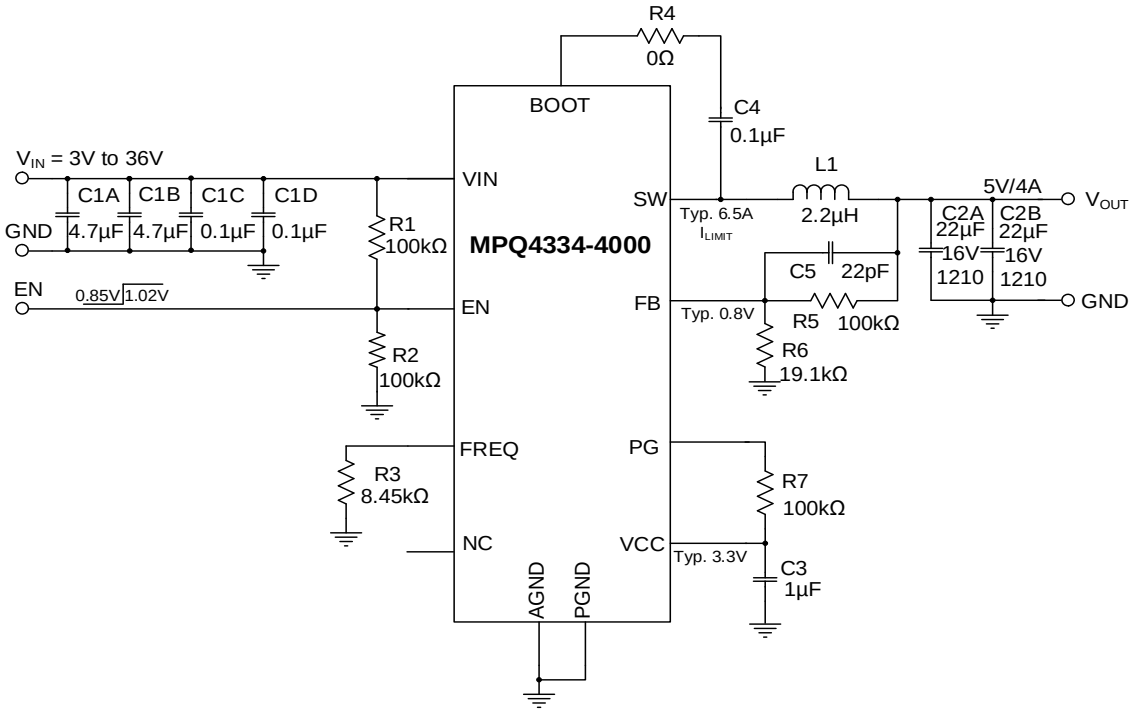


Figure 11: Typical Application Circuit for the MPQ4334-4000 (V_{OUT} = 5V, f_{SW} = 2.2MHz)

Table 2: Design Guide Index

Pin #		Pin Name	Component	Design Guide Index
QFN-12	QFN-14			
1, 11	1, 13	PGND	-	Ground Connection (PGND Pins)
2, 10	3, 11	VIN	C1A, C1B, C1C, C1D	Selecting the Input Capacitors (VIN Pins)
3	4	BOOT	R4, C4	Floating Driver and Bootstrap Charging (BOOT Pin)
4	5	FREQ	R3	Setting the Switching Frequency/SYNC Input and Mode Selection (FREQ Pin)
5	6	VCC	C3	Setting the internal V_{CC} (VCC Pin)
6	7	AGND	-	Ground Connection (AGND Pin)
7	8	FB	R5, R6, C5	Feedback Divider and Feedforward Capacitor (FB) Pin
8	9	PG	R7	Power Good Indicator (PG Pin)
9	10	EN	R1, R2	Enable and Under-Voltage Lockout (UVLO) (EN Pin)
12	14	SW	L1, C2A, C2B	Selecting the Inductor and Output Capacitors (SW Pin)
-	2, 12	NC	-	No connection

Ground Connection (PGND and AGND Pins)

See the PCB Layout Guidelines on page 76 for more details.

Selecting the Input Capacitors (VIN Pins)

The step-down converter has a discontinuous input current, and requires a capacitor to supply AC current to the converter while maintaining the DC V_{IN}. For the best performance, use low-ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients.

For most applications, use a 4.7µF to 10µF capacitor. It is strongly recommended to use an additional lower-value capacitor (e.g. 0.1µF) with a small package size (0603) to absorb high-frequency switching noise. Place the smaller capacitor as close to VIN and PGND as possible.

Since the input capacitor (C_{IN}) absorbs the input switching current, it requires an adequate ripple current rating. The input capacitor's RMS current (I_{CIN}) can be estimated with Equation (1):

$$I_{CIN} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (1)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, calculated with Equation (2):

$$I_{CIN} = \frac{I_{LOAD}}{2} \quad (2)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current. The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g. 0.1µF) placed as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input. The V_{IN} ripple (ΔV_{IN}) caused by the capacitance can be estimated with Equation (3):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (3)$$

Floating Driver and Bootstrap Charging (BOOT Pin)

The BOOT capacitor (C_{BOOT}, also called C4) is recommended to be between 47nF and 220nF. It is recommended for the BOOT resistor (R_{BOOT}, also called R4) to be less than 10Ω.

Place R_{BOOT} in series with C_{BOOT} to reduce the SW rising rate and voltage spikes. This helps enhance EMI performance and reduce voltage stress at high input voltages. A higher resistance improves switching spike reduction but compromises efficiency. A tradeoff must be made between EMI and efficiency.

Setting the Switching Frequency (FREQ Pin Configured as FREQ)

When the value of "Z" in the four-digit code "WXYZ" is "0," "3," "6," or "7," f_{SW} can be configured by an external frequency resistor (R_{FREQ}) connected from the FREQ pin to AGND (see Table 1 on page 3).

R_{FREQ} should be located between the FREQ pin and AGND, placed as close as possible to the device. Table 3 and Switching Frequency vs. Frequency Resistor curves on pages 49-51 shows the relationship between f_{SW} and R_{FREQ}.

Table 3: f_{SW} vs. R_{FREQ}

R_{FREQ} (kΩ)	f_{SW} (kHz)
7.87	2500
8.45	2200
14	1500
19.1	1000
32.4	590
41.2	470
48.7	400
57.6	340
97.6	200

It is not possible to have both a high f_{SW} and high duty cycle due to the HS-FET's limited minimum on time. The MPQ4334 control loop automatically achieves the maximum frequency, which also reduces excessive power loss. V_{OUT} is regulated by varying the duration of the HS-FET's off time, which automatically reduces f_{SW}.

The device is guaranteed to comply with the HS-FET's minimum on time. An advantage of this method is that the device works at the target f_{SW} for as long as possible, and f_{SW} only changes when the device operates at high duty cycles.

When the value of "Z" in the four-digit code "WXYZ" is "1," "2," "4," "5," or "8," f_{SW} is fixed and cannot be configured. See the SYNC/MODE section for more details.

SYNC Input and Mode Selection (FREQ Pin Configured as SYNC/MODE)

Depends on the value of "Z" in the four-digit code "WXYZ," FREQ can be trimmed as SYNC/MODE (see Table 1 on page 3).

f_{SW} can be synchronized to the rising edge of a clock signal applied at SYNC (the FREQ pin). Switching can be synchronized to an external clock within a SYNC clock locking time (128 cycles). When using the SYNC function, the SYNC frequency (f_{SYNC}) should be within a certain range near the internal fixed f_{SW}. And the internal fixed f_{SW} is related to the "Z" code. Table 4 shows the specific range.

Table 4: SYNC Frequency Range

Control Mode Value "Z"	Internal Fixed f_{SW} (kHz)	SYNC frequency (f_{SYNC}) Range (kHz)
1 or 4	400	364 to 428
8	470	428 to 502
2 or 5	2200	2138 to 2226

When this pin is used for mode selection, pull it high to force the part to work in FCCM; pull it pin low to force the part to work in AAM mode (see Table 5). The operation mode can be changed during operation.

Table 5: Mode Selection

SYNC/MODE Input	Operation
<0.4V	AAM Mode
>1.4V	FCCM
External clock in	FCCM

Selecting the Internal VCC Capacitor (VCC Pin)

The VCC capacitor (V_{CC}, also called C3) is recommended to be 1µF.

Most of the internal circuitry is powered by the internal 5V VCC regulator. This regulator uses V_{IN} as its input and operates across the full V_{IN} range. When V_{IN} exceeds 3.3V, VCC is in full regulation. When V_{IN} drops below 3.3V, the VCC output degrades.

Feedback Divider and Feedforward Capacitor (FB Pin)

For an adjustable-output version, the feedback (FB) voltage (V_{FB}) is typically 0.8V. The external resistor divider connected to FB (R_6) sets V_{OUT} (see Figure 12).

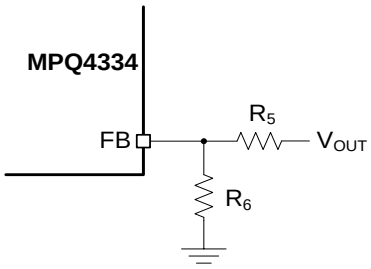


Figure 12: Feedback Divider Network for an Adjustable-Output Version

R_6 can be calculated with Equation (4):

$$R_6 = \frac{R_5}{\frac{V_{OUT}}{0.8V} - 1} \quad (4)$$

For a fixed-output version, the FB resistor divider is integrated internally. This means that FB should be connected directly to the output to set V_{OUT}. The following fixed outputs can be selected: 1V, 1.8V, 2.5V, 3V, 3.3V, 3.8V, or 5V (see Figure 13).

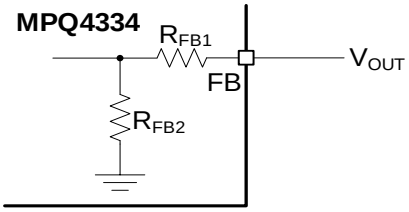


Figure 13: Feedback Divider Network for a Fixed-Output Version

Table 6 shows the relationship between the internal R_{FBx} and V_{OUT}.

Table 6: R_{FB} vs. V_{OUT}

V_{OUT} (V)	R_{FB1} (kΩ)	R_{FB2} (kΩ)
1	64	256
1.8	320	256
2.5	544	256
3	704	256
3.3	800	256
3.8	960	256
5	1344	256

A feed-forward capacitor (C5) improves the phase margin and transient response of circuits that have output capacitors with a low ESR.

Power Good Indicator (PG Pin)

The PG resistor (R_{PG}, also called R7) should have a 10kΩ to 100kΩ resistance. The MPQ4334 includes an open-drain power good (PG) output that indicates whether the regulator's output is within the specific window of its nominal value.

If using PG, connect it to a logic high level power source (e.g. 3.3V) via a pull-up resistor. PG goes high if V_{OUT} is within 94.5% to 105.5% of its nominal voltage; PG goes low if V_{OUT} is above 107% or below 93% of its nominal voltage. Float PG if it is not used.

If V_{OUT} is outside of its nominal range and EN shutdown occurs, PG goes low.

Enable and Under-Voltage Lockout (UVLO) Protection (EN Pin)

EN is a digital control pin that turns the regulator on and off.

Enabled via External Logic High/Low Signal

When the EN voltage (V_{EN}) reaches 0.5V, the bandgap (BG) does not turn on until V_{IN} exceeds 2.7V. BG then provides an accurate reference voltage for the EN threshold. Forcing EN above its rising threshold (about 1.02V) turns the device on. Turn the device off by driving EN below 0.85V. There is no internal pull-up or pull-down resistor connected to the EN pin, so do not float EN. An external pull-up or pull-down resistor is required if the control signal cannot provide accurate high or low logic.

Configurable V_{IN} Under-Voltage Lockout (UVLO) Protection

The MPQ4334 has an internal, fixed under-voltage lockout (UVLO) threshold. The rising threshold is 3.6V, and the falling threshold is about 2.5V. For applications that require a higher UVLO point, an external resistor divider can be placed between VIN and EN to achieve a higher equivalent UVLO threshold (see Figure 14).

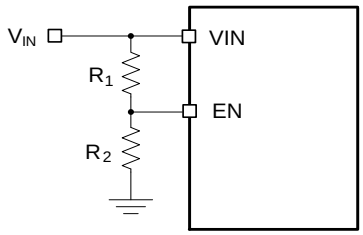


Figure 14: Configurable UVLO via the EN Divider

The UVLO rising threshold ($V_{IN\_UV\_RISING}$) can be calculated with Equation (5):

$$V_{IN\_UV\_RISING} = (1+\frac{R_1}{R_2}) \times V_{EN\_RISING} \quad (5)$$

Where V_{EN_RISING} is 1.02V.

The UVLO falling threshold ($V_{IN\_UV\_FALLING}$) can be calculated with Equation (6):

$$V_{IN\_UV\_FALLING} = (1+\frac{R_1}{R_2}) \times V_{EN\_FALLING} \quad (6)$$

Where $V_{EN\_FALLING}$ is 0.85V.

If EN is not used to control when the device turns on and off, connect EN to a high-voltage source (e.g. VIN) to turn the device on by default.

Selecting the Inductor and Output Capacitors (SW Pin)

The inductance (L) can be estimated with Equation (7):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1-\frac{V_{OUT}}{V_{IN}}) \quad (7)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

A 1µH to 22µH inductor with a DC current rating at least 25% greater than the maximum load current is recommended for most applications. For higher efficiency, choose an inductor with a lower DC resistance. A larger-value inductor results in less ripple current and a lower output ripple voltage, but also has a larger physical size, higher series resistance, and lower saturation current. A good rule to determine the inductance is to allow the inductor ripple current to be approximately 30% of the maximum load current. The peak inductor current (I_{LP}) can be calculated with Equation (8)

$$I_{LP} = I_{LOAD} + \frac{V_{OUT}}{2f_{SW} \times L} \times (1-\frac{V_{OUT}}{V_{IN}}) \quad (8)$$

Choose an inductor that does not saturate under I_{LP}.

The V_{OUT} ripple (ΔV_{OUT}) can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (9)$$

Where L is the inductance, R_{ESR} is C_{OUT}'s equivalent series resistance (ESR), and C_{OUT} maintains the DC V_{OUT}.

Use ceramic, tantalum, or low-ESR electrolytic capacitors. For the best results, use low-ESR capacitors to keep ΔV_{OUT} low.

For ceramic capacitors**,** the capacitance dominates the impedance at f_{SW} and causes the majority of ΔV_{OUT}. For simplification, ΔV_{OUT} can be calculated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (10)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at f_{SW}. For simplification, ΔV_{OUT} can be estimated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (11)$$

When selecting C_{OUT}, consider the allowable overshoot in V_{OUT} if the load is suddenly removed. In this scenario, energy stored in the inductor is transferred to C_{OUT}, causing its voltage to rise. To achieve an optimal overshoot relative to the regulated voltage, C_{OUT} can be estimated with Equation (12):

$$C_{OUT} = \frac{I_{OUT}^2 \times L}{V_{OUT}^2 \times ((V_{OUTMAX} / V_{OUT})^2 - 1)} \quad (12)$$

Where V_{OUTMAX} / V_{OUT} is the allowable maximum overshoot.

After calculating the capacitance that meets both the ripple and overshoot requirements, choose the larger capacitance.

The characteristics of C_{OUT} also affect the stability of the regulation system. The MPQ4334 can be optimized for a wide range of capacitances and ESR values.

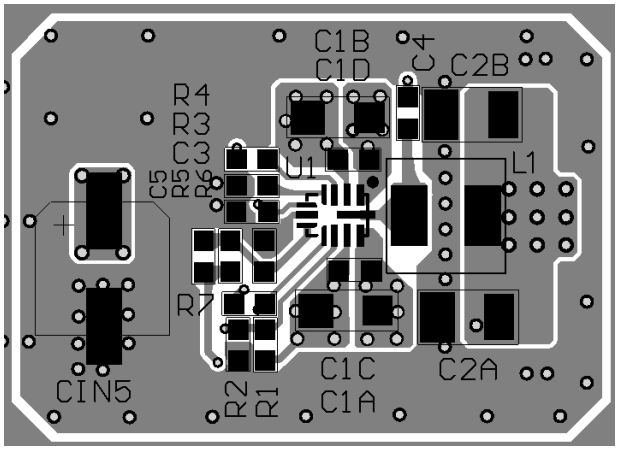
PCB Layout Guidelines [15]

Efficient PCB layout, especially input capacitor placement, is critical for stable operation. A 4-layer layout is strongly recommended to improve thermal performance. For the best results, refer to Figure 15 and follow the guidelines below:

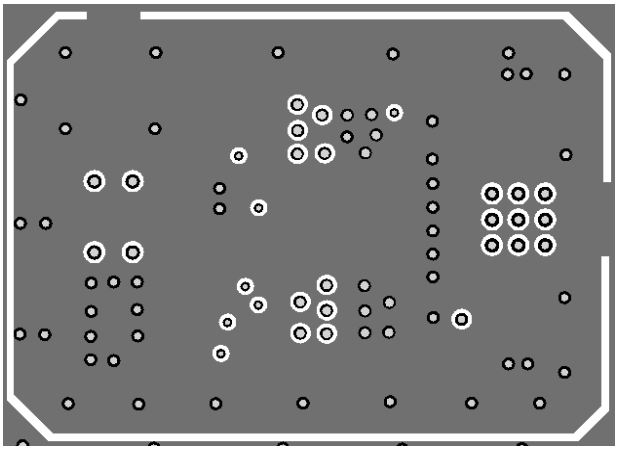
1. Place symmetric input capacitors as close to the VIN and PGND pins as possible.
2. Connect a large ground plane directly to PGND.
3. Add vias near PGND if the bottom layer is a ground plane.
4. Ensure that the high-current paths at PGND and VIN have short, direct, and wide traces.
5. Place the ceramic input capacitor, especially the small package size (0603) input bypass capacitor, as close to the VIN and PGND pins as possible to minimize high-frequency noise.
6. Keep the connection between C_{IN} and VIN as short and wide as possible.
7. Place C_{VCC} as close to the VCC and AGND pins as possible.
8. Route SW and BOOT away from sensitive analog areas, such as FB.
9. Place the FB resistors close to the chip to ensure the trace connecting to FB is as short as possible.
10. Use multiple vias to connect the power planes to the internal layers.

Note:

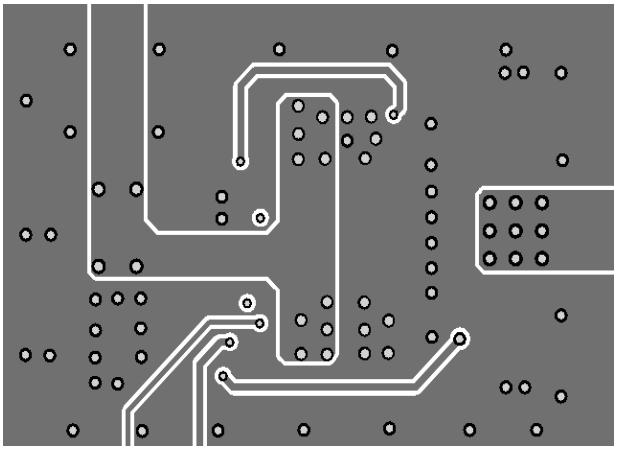
15) The recommended PCB layout is based on Figure 11 on page 71.



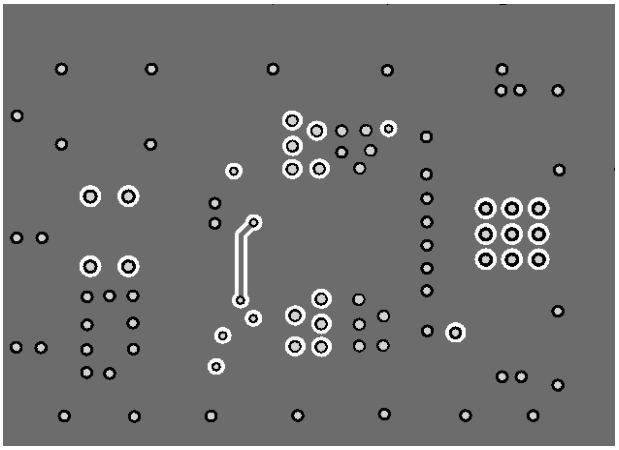
Top Silk and Top Layer



Mid-Layer 1



Mid-Layer 2



Bottom Layer and Bottom Silk

Figure 15: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

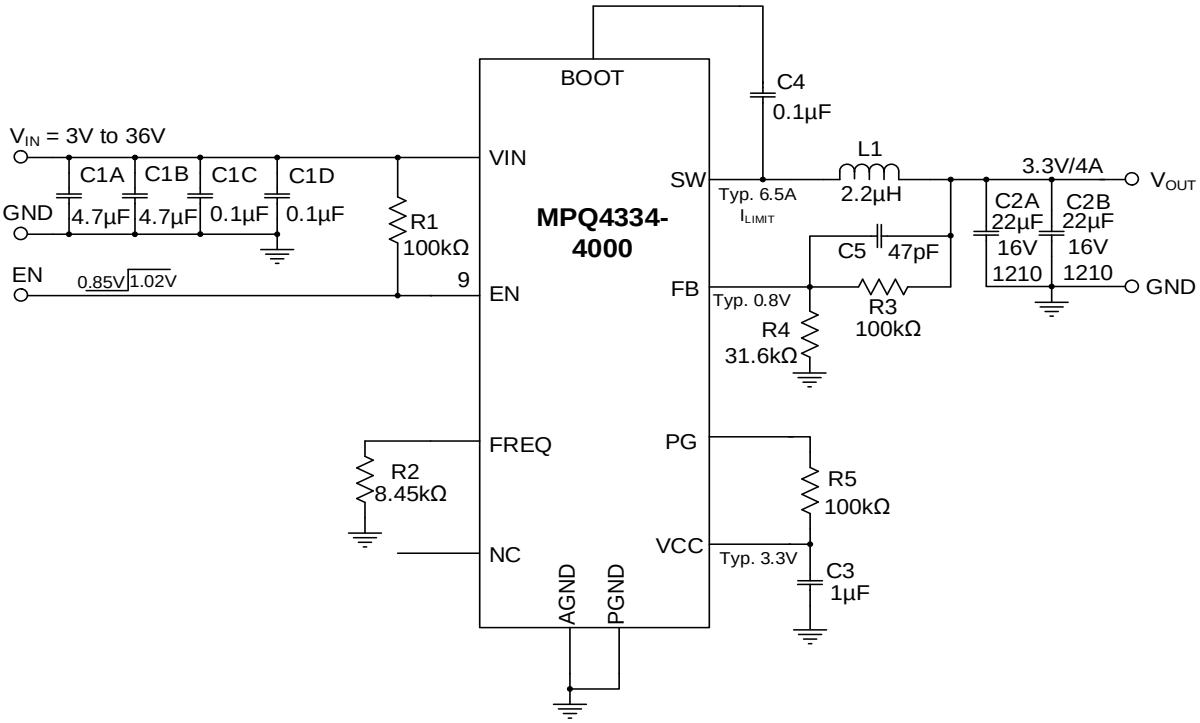


Figure 16: Typical Application Circuit (V_{OUT} = 3.3V, f_{SW} = 2.2MHz, 4A Version)

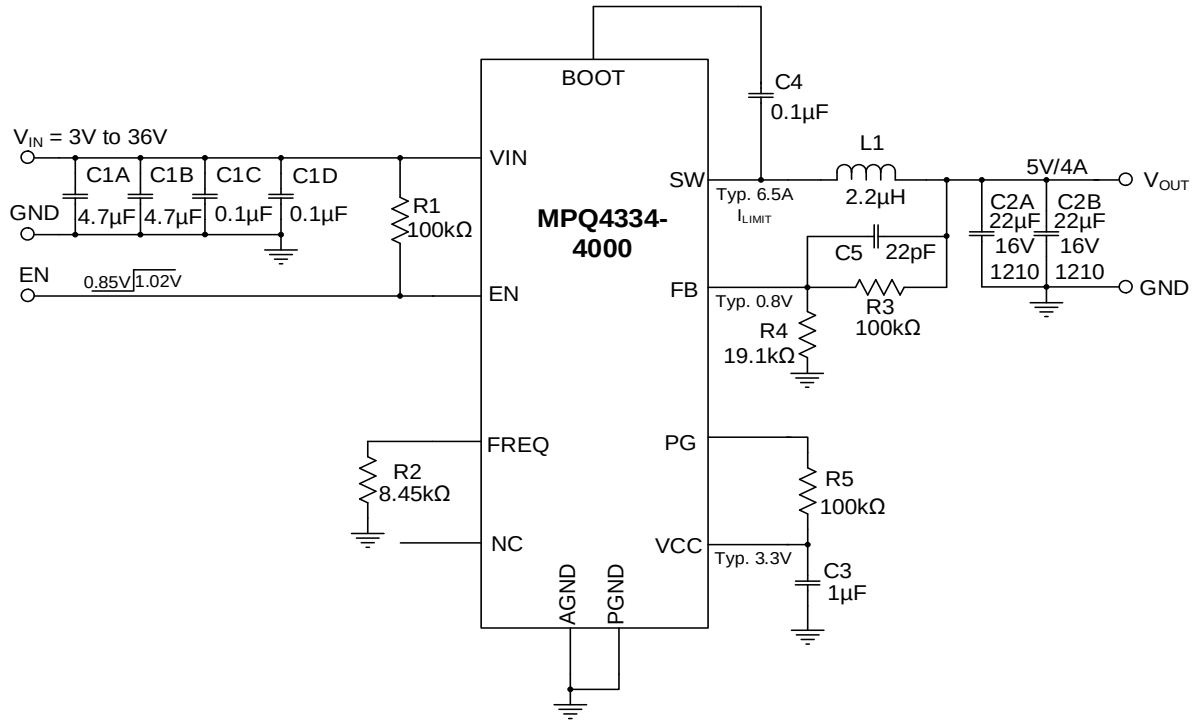


Figure 17: Typical Application Circuit (V_{OUT} = 5V, f_{SW} = 2.2MHz, 4A Version)

TYPICAL APPLICATION CIRCUITS *(continued)*

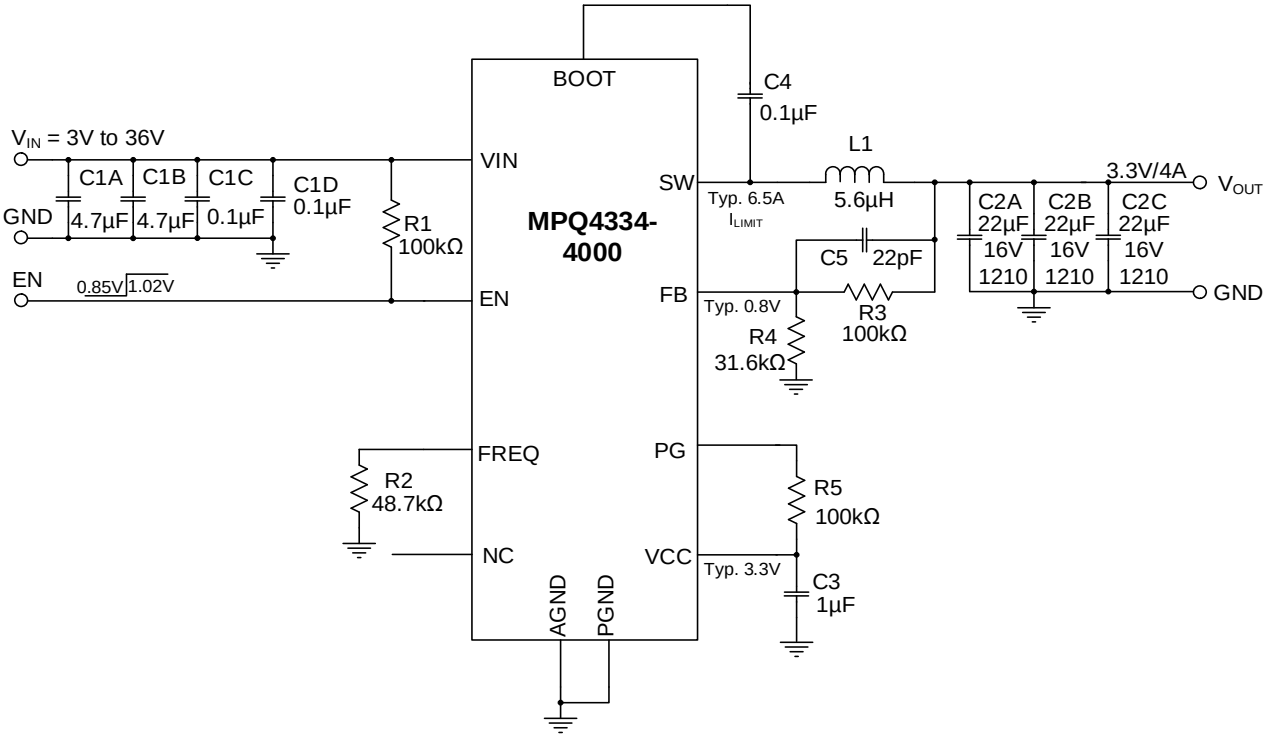


Figure 18: Typical Application Circuit (V_{OUT} = 3.3V, f_{SW} = 415kHz, 4A Version)

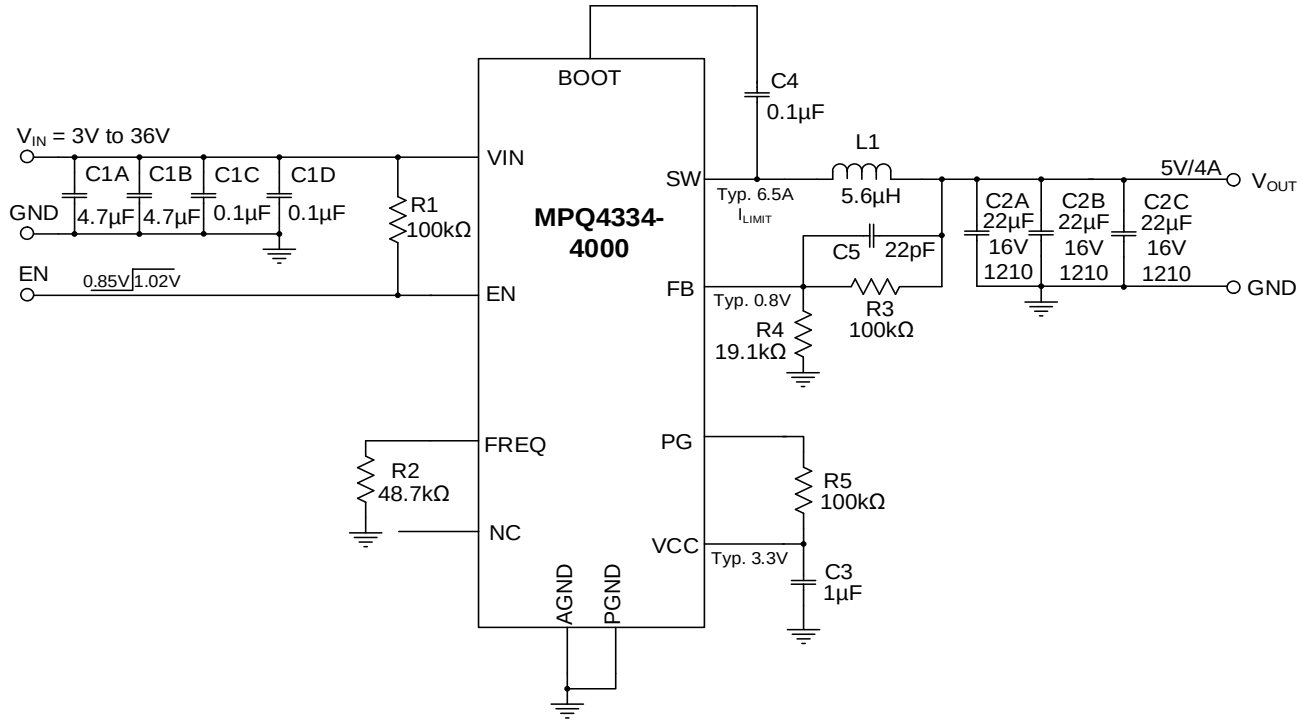


Figure 19: Typical Application Circuit (V_{OUT} = 5V, f_{SW} = 415kHz, 4A Version)

TYPICAL APPLICATION CIRCUITS *(continued)*

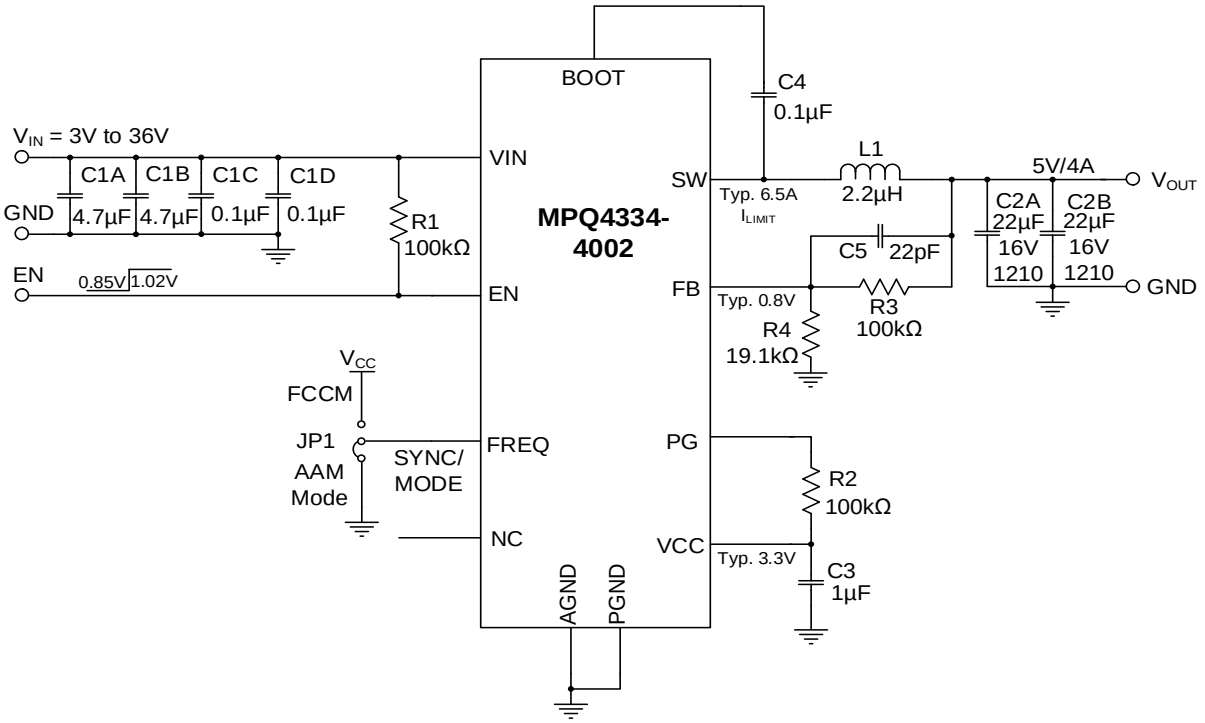


Figure 20: Typical Application Circuit (V_{OUT} = 5V, Internal f_{SW} = 2.2MHz, FREQ as SYNC/MODE, 4A Version)

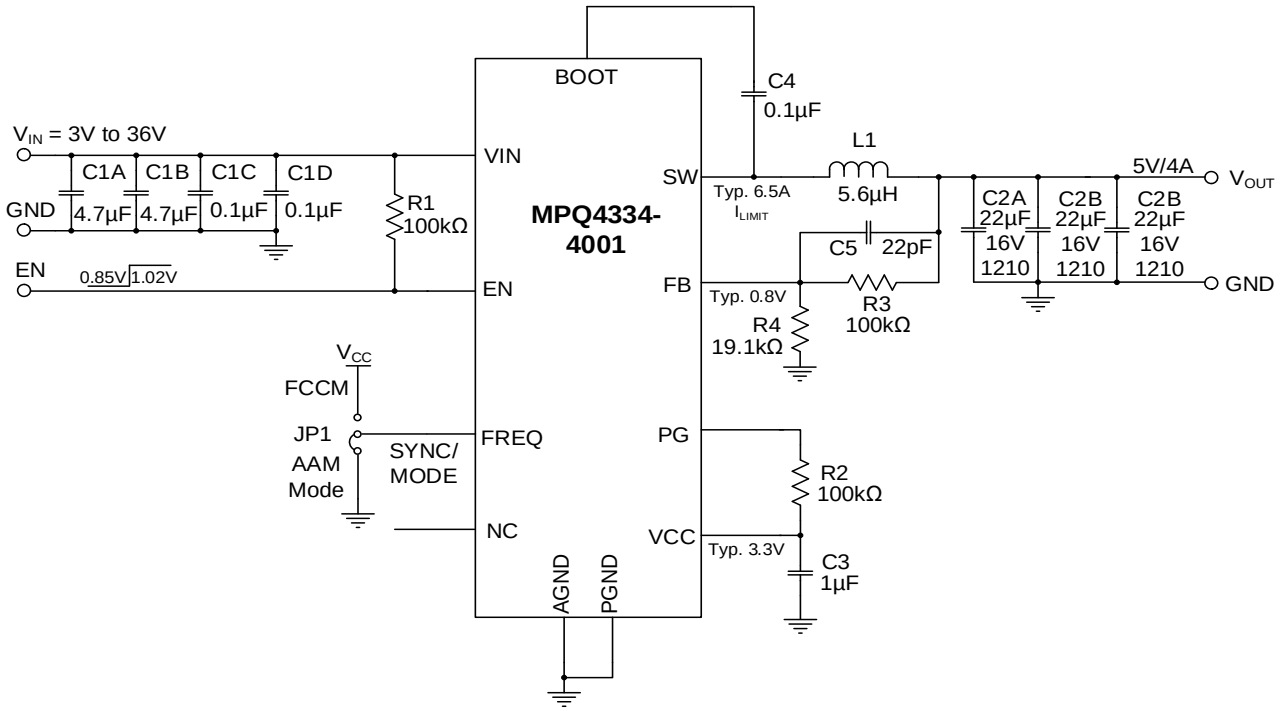


Figure 21: Typical Application Circuit (V_{OUT} = 5V, Internal f_{SW} = 400kHz, FREQ as SYNC/MODE, 4A Version)

TYPICAL APPLICATION CIRCUITS *(continued)*

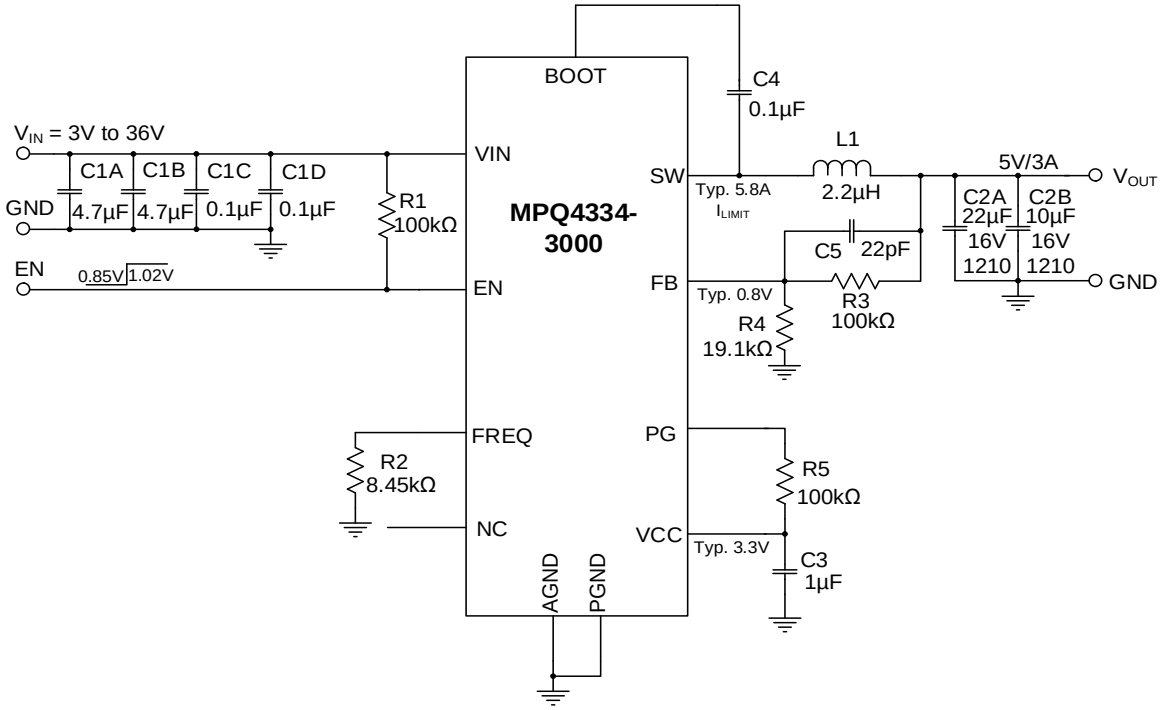


Figure 22: Typical Application Circuit (V_{OUT} = 5V, f_{SW} = 2.2MHz, 3A Version)

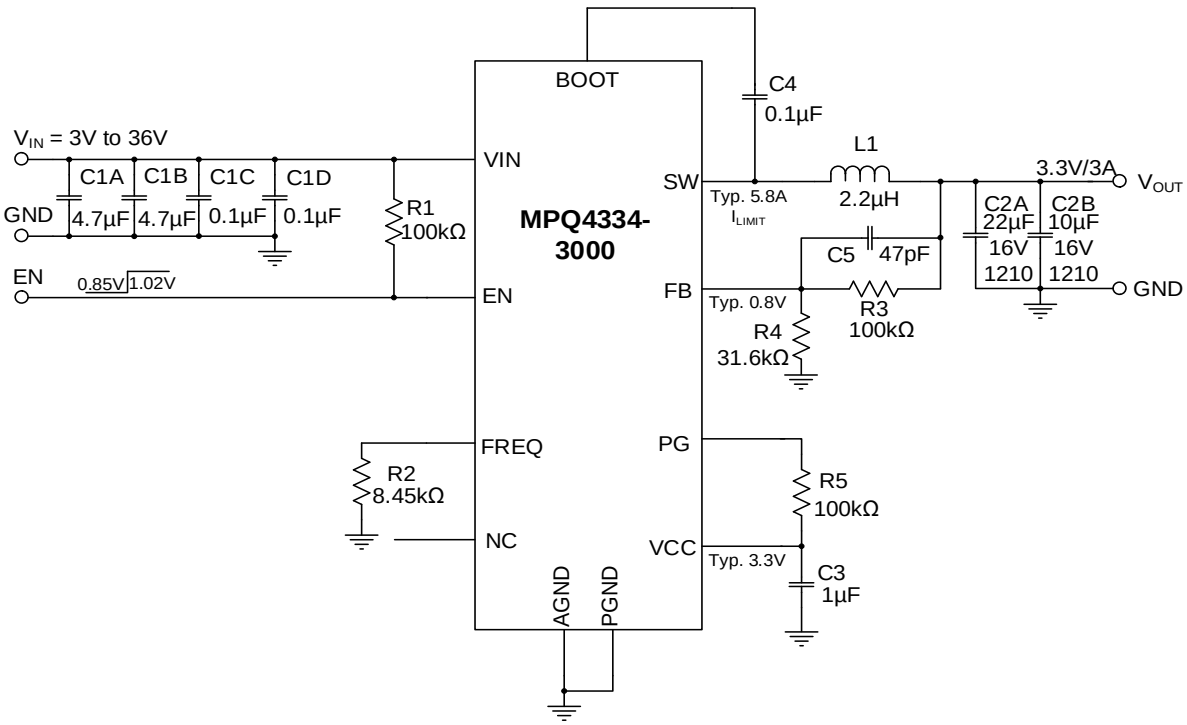


Figure 23: Typical Application Circuit (V_{OUT} = 3.3V, f_{SW} = 2.2MHz, 3A Version)

TYPICAL APPLICATION CIRCUITS *(continued)*

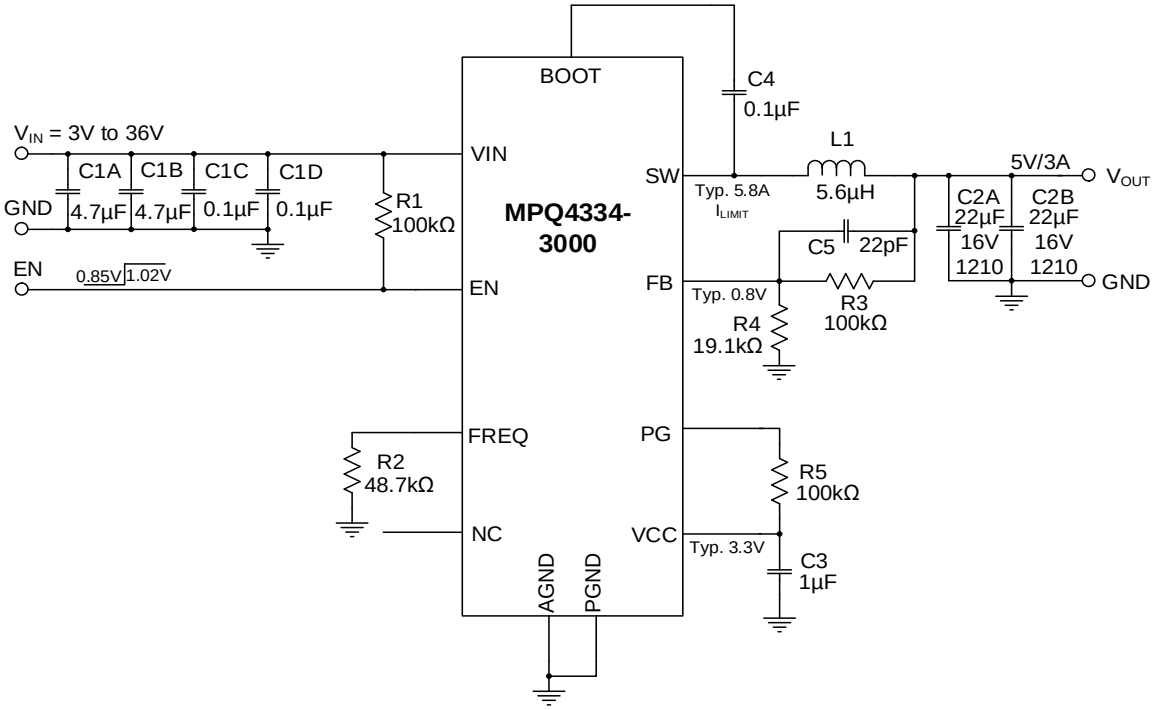


Figure 24: Typical Application Circuit (V_{OUT} = 5V, f_{SW} = 415kHz, 3A Version)

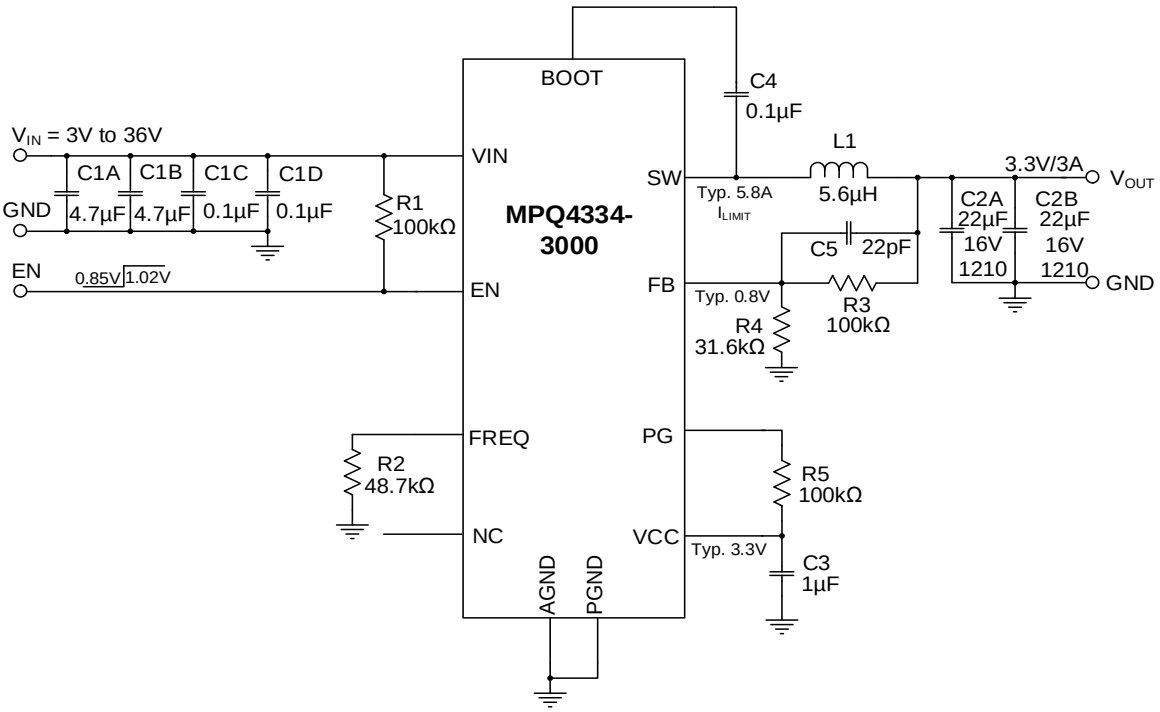


Figure 25: Typical Application Circuit (V_{OUT} = 3.3V, f_{SW} = 415kHz, 3A Version)

TYPICAL APPLICATION CIRCUITS *(continued)*

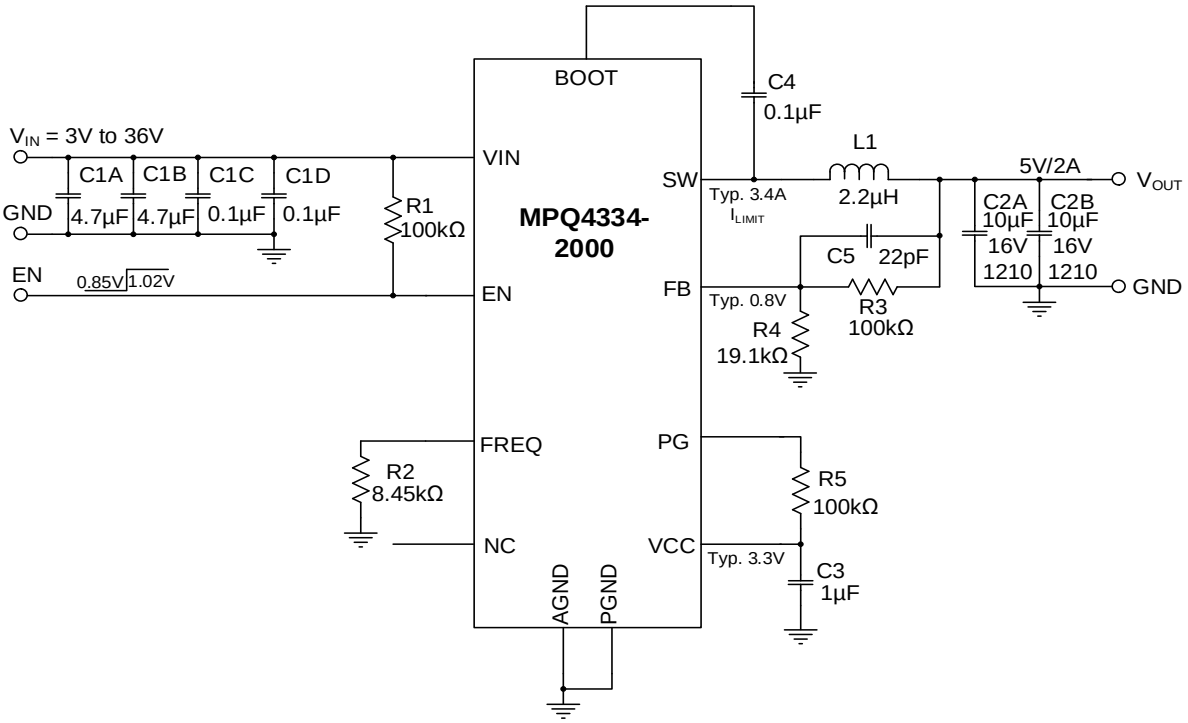


Figure 26: Typical Application Circuit (V_{OUT} = 5V, f_{SW} = 2.2MHz, 2A Version)

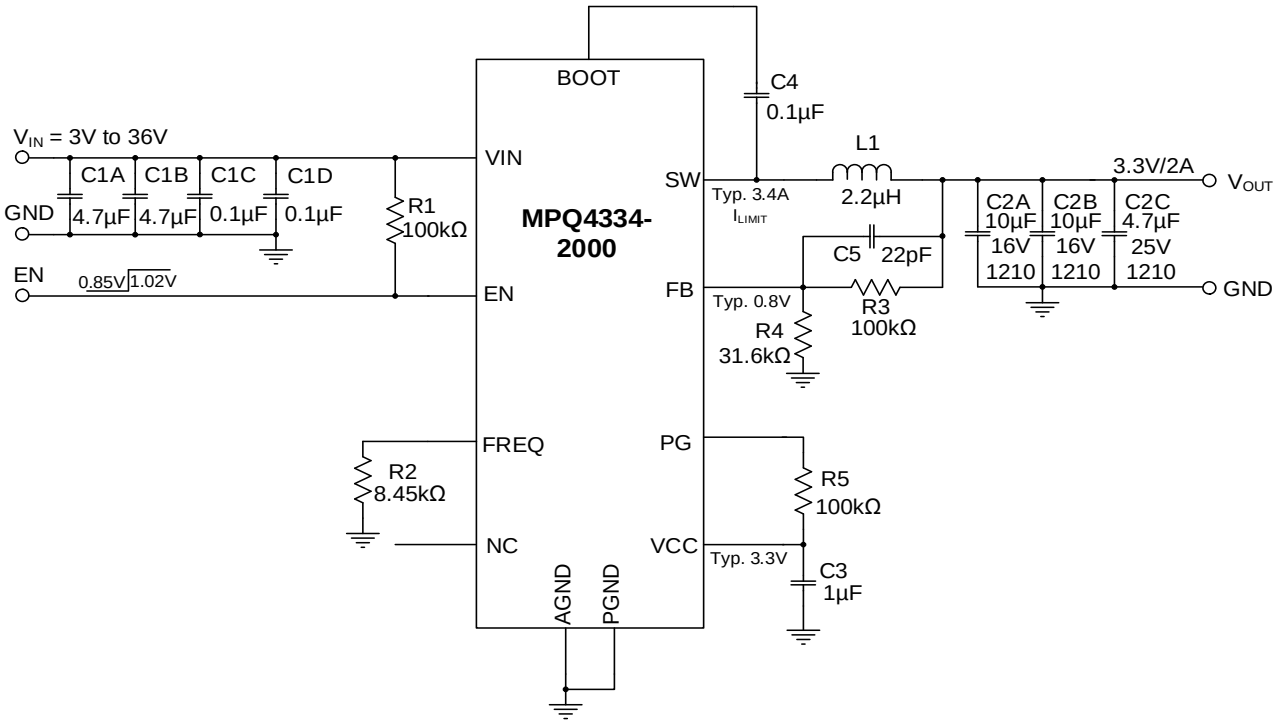


Figure 27: Typical Application Circuit (V_{OUT} = 3.3V, f_{SW} = 2.2MHz, 2A Version)

TYPICAL APPLICATION CIRCUITS *(continued)*

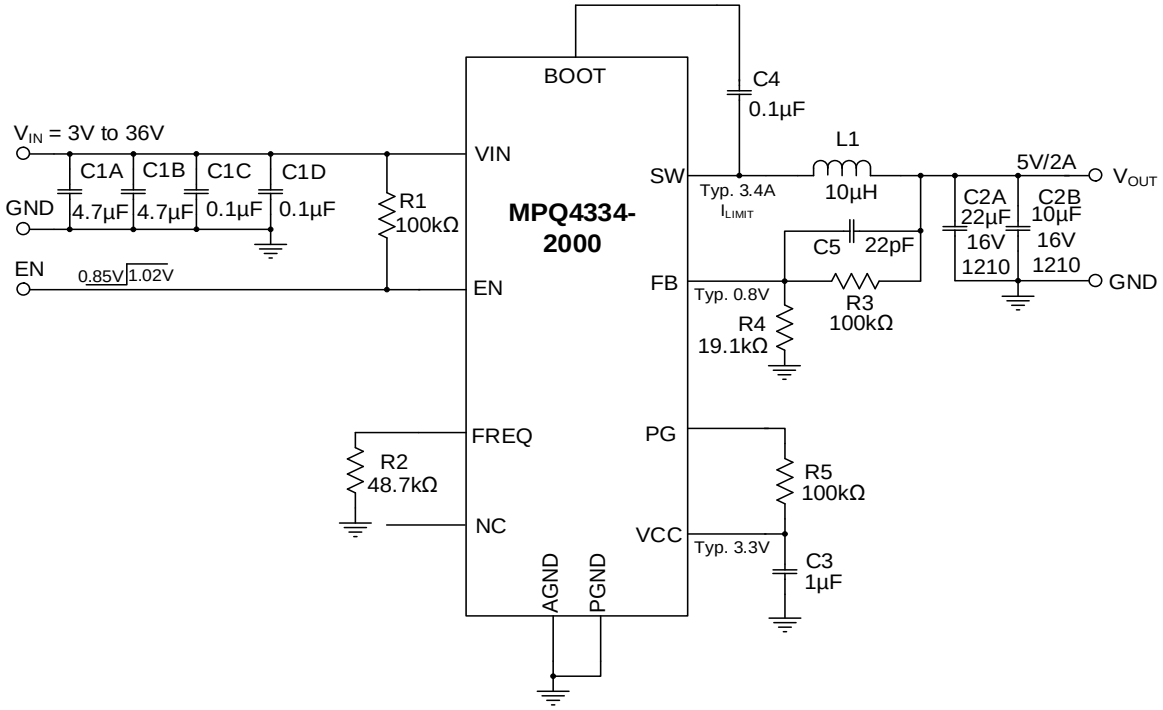


Figure 28: Typical Application Circuit (V_{OUT} = 5V, f_{SW} = 415kHz, 2A Version)

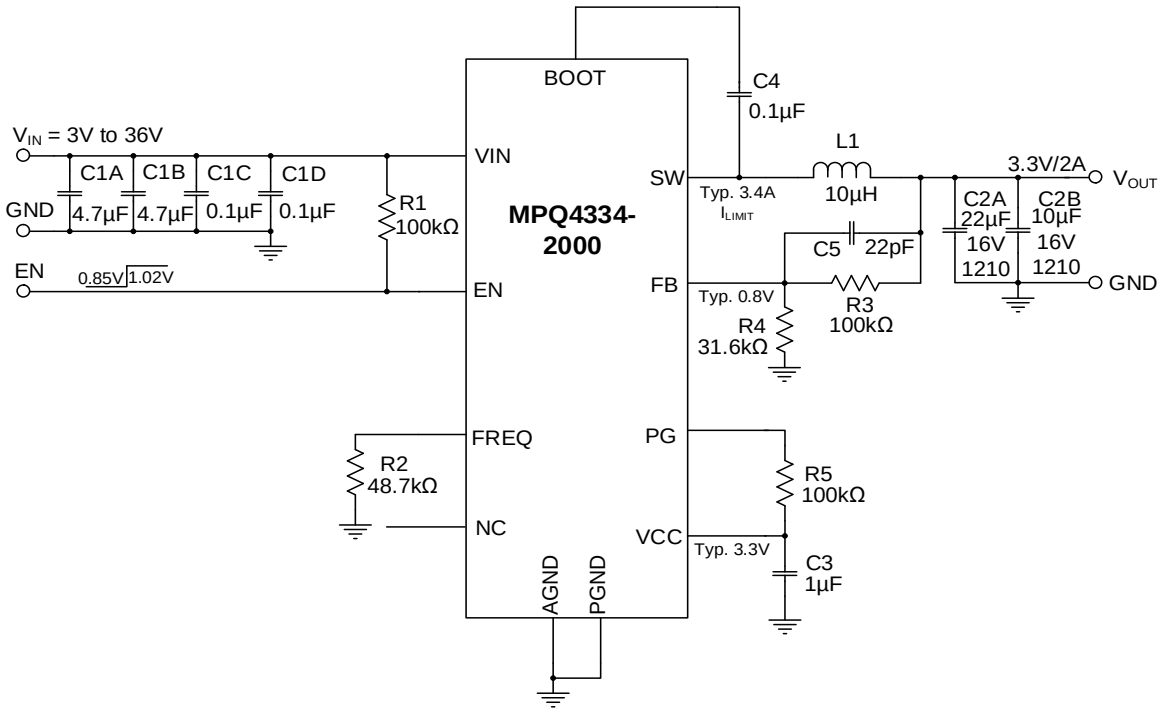


Figure 29: Typical Application Circuit (V_{OUT} = 3.3V, f_{SW} = 415kHz, 2A Version)

TYPICAL APPLICATION CIRCUITS *(continued)*

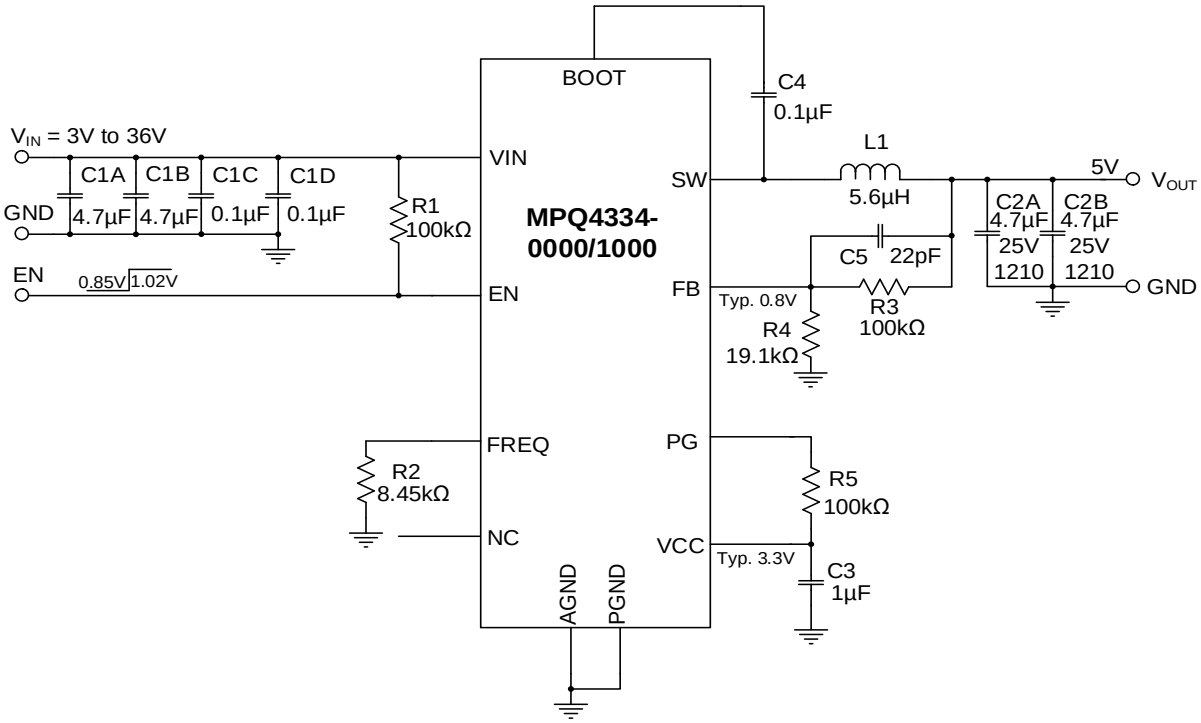


Figure 30: Typical Application Circuit (V_{OUT} = 5V, f_{SW} = 2.2MHz, 0.5A/1A Version)

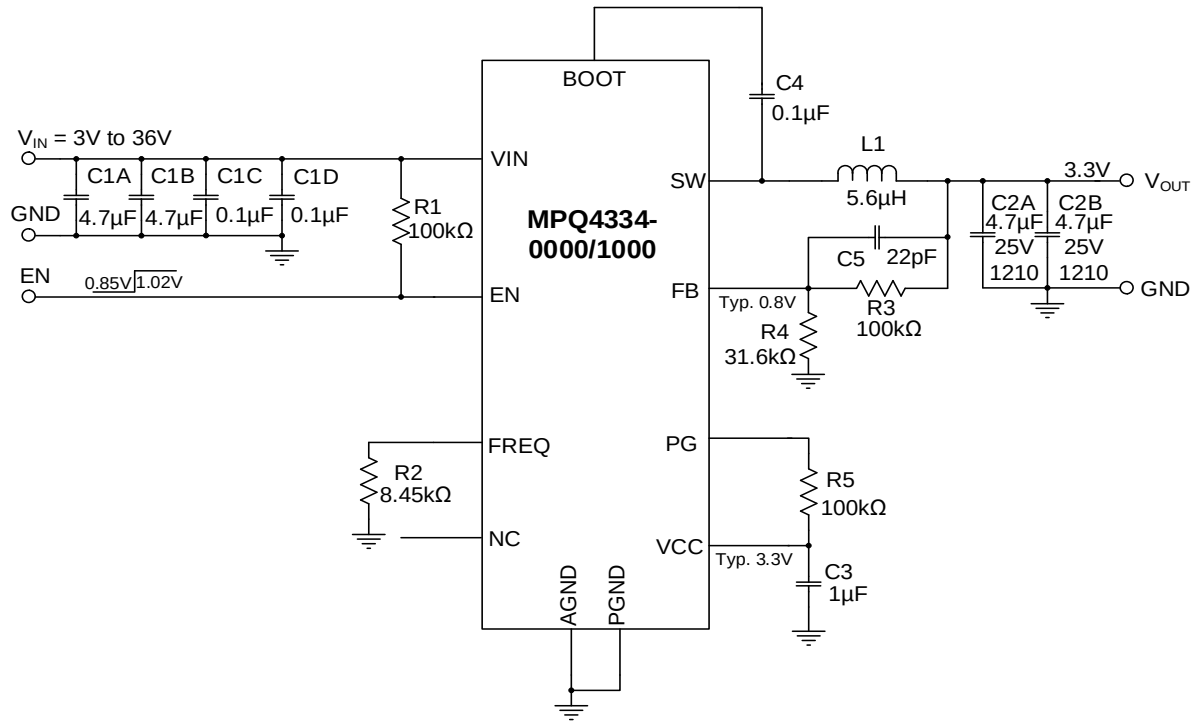


Figure 31: Typical Application Circuit (V_{OUT} = 3.3V, f_{SW} = 2.2MHz, 0.5A/1A Version)

TYPICAL APPLICATION CIRCUITS *(continued)*

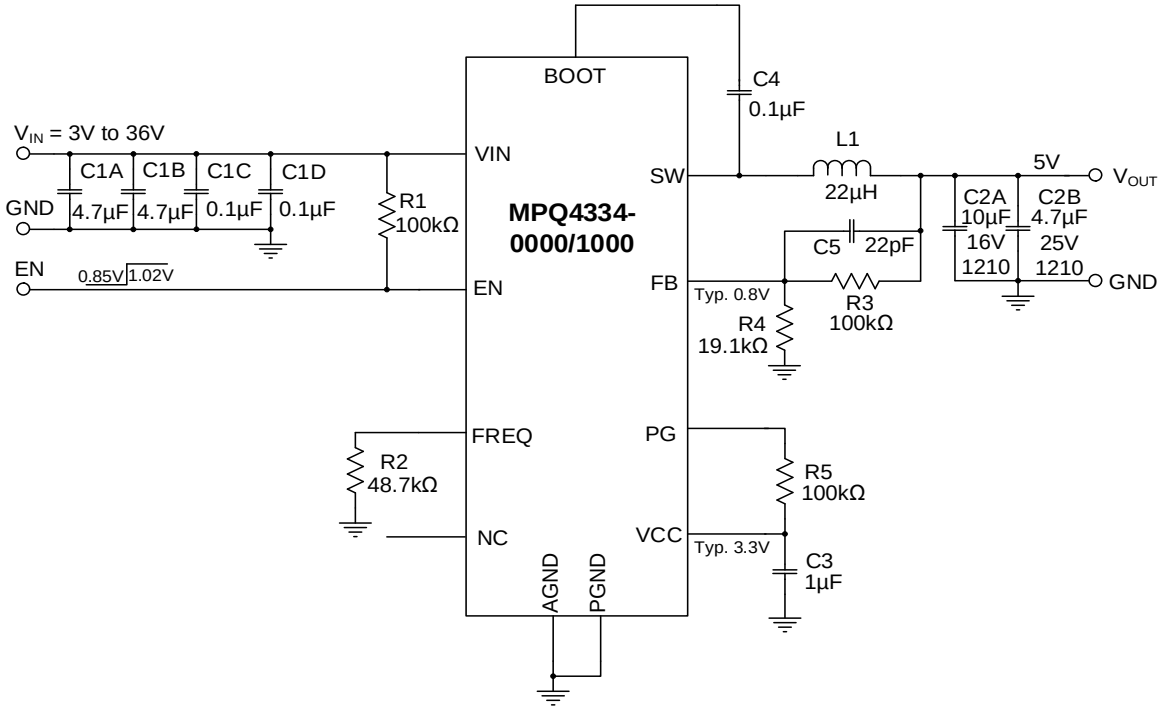


Figure 32: Typical Application Circuit (V_{OUT} = 5V, f_{SW} = 415kHz, 0.5A/1A Version)

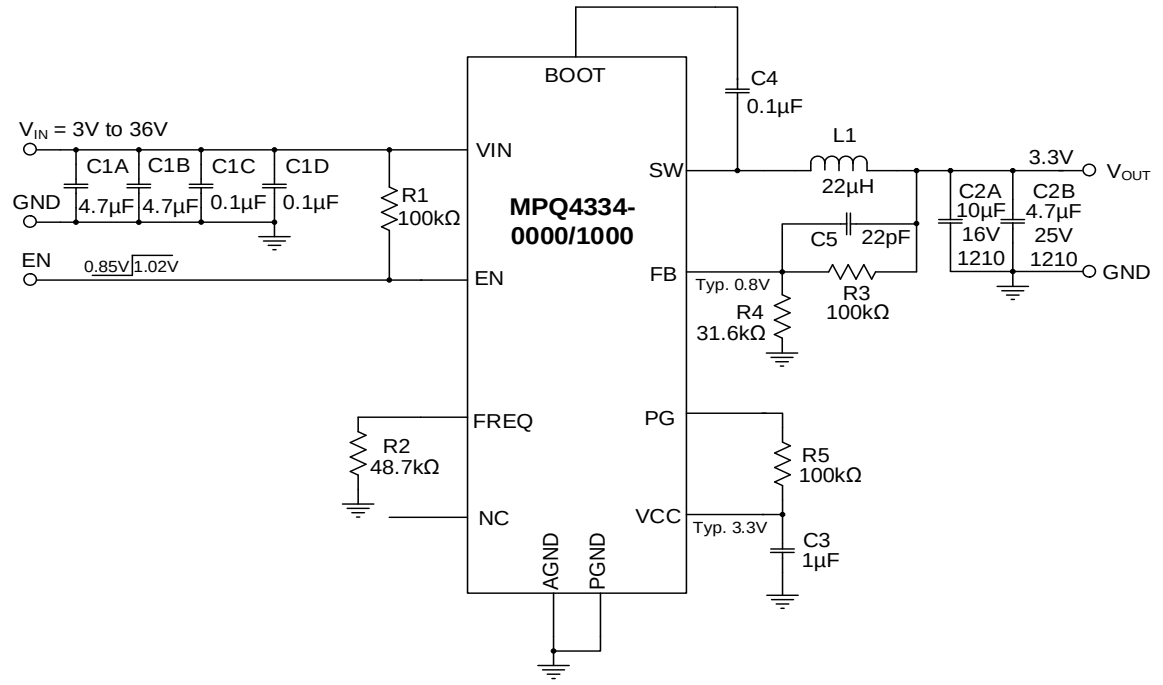


Figure 33: Typical Application Circuit (V_{OUT} = 3.3V, f_{SW} = 415kHz, 0.5A/1A Version)

TYPICAL APPLICATION CIRCUITS *(continued)*

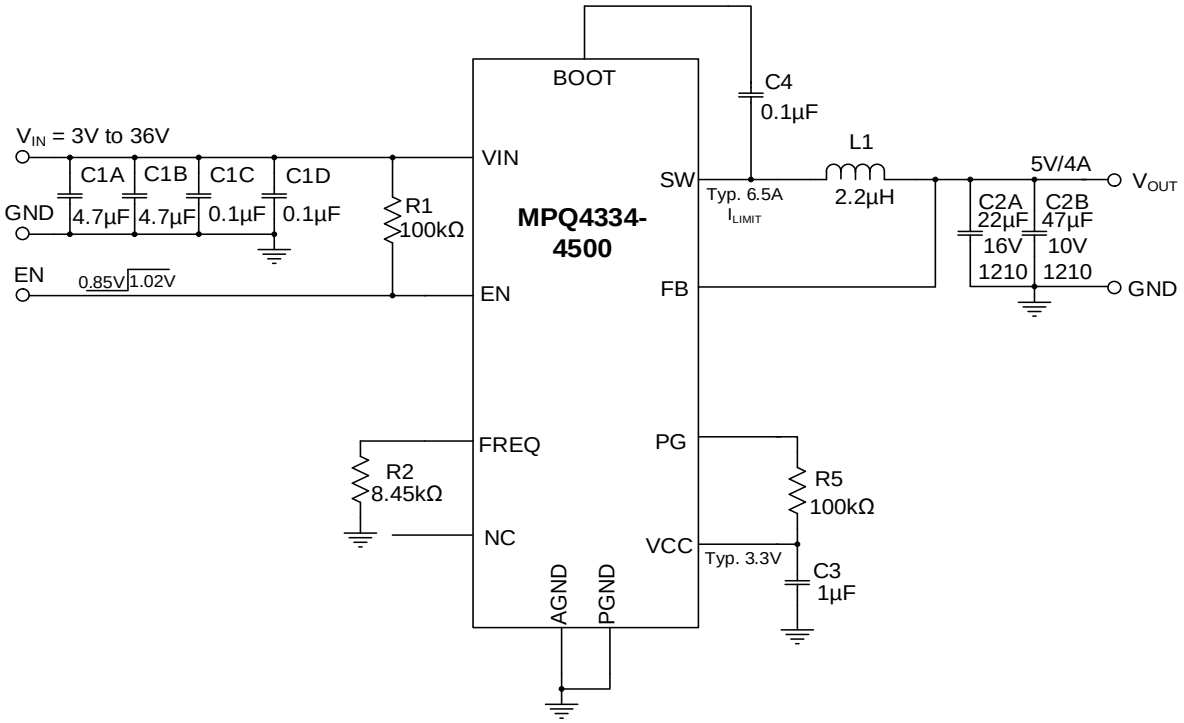


Figure 34: Typical Application Circuit (5V Fixed-Output, f_{SW} = 2.2MHz, 4A Version)

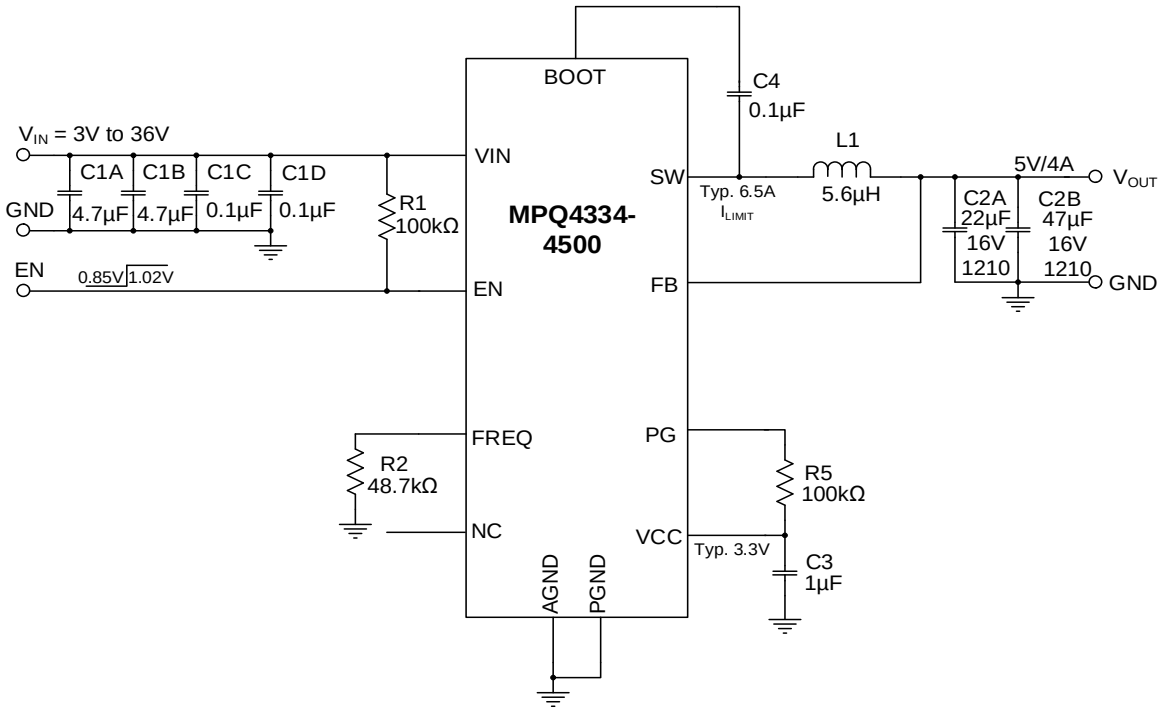


Figure 35: Typical Application Circuit (5V Fixed-Output, f_{SW} = 400kHz, 4A Version)

TYPICAL APPLICATION CIRCUITS *(continued)*

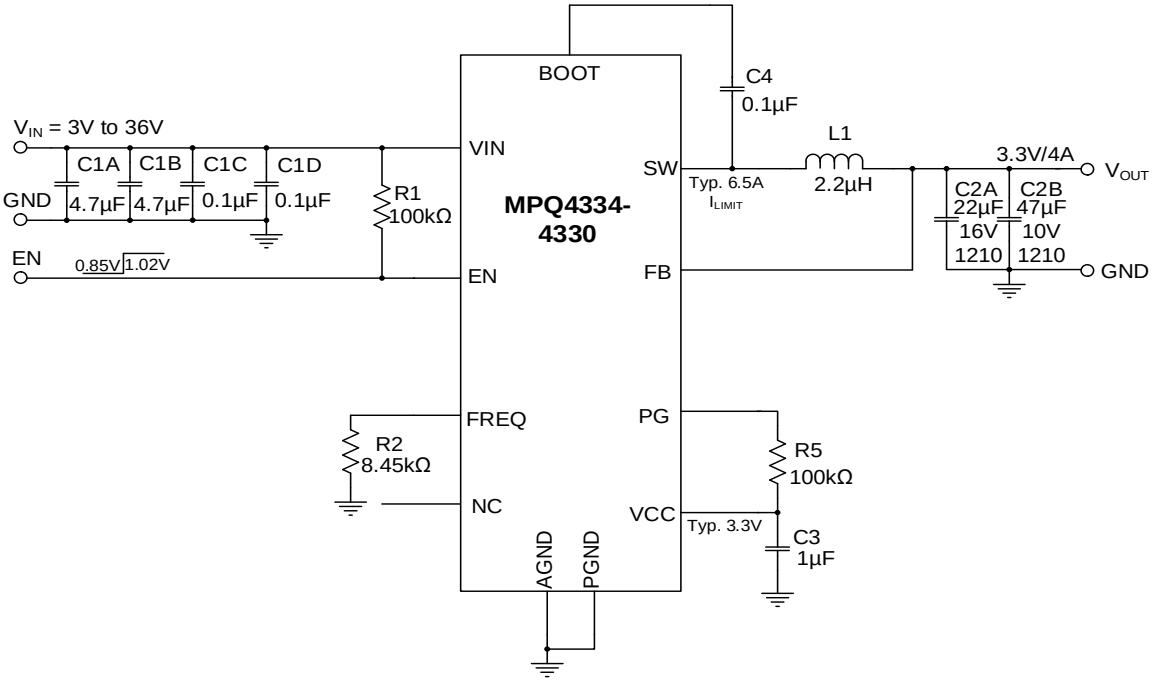


Figure 36: Typical Application Circuit (3.3V Fixed-Output, f_{SW} = 2.2MHz, 4A Version)

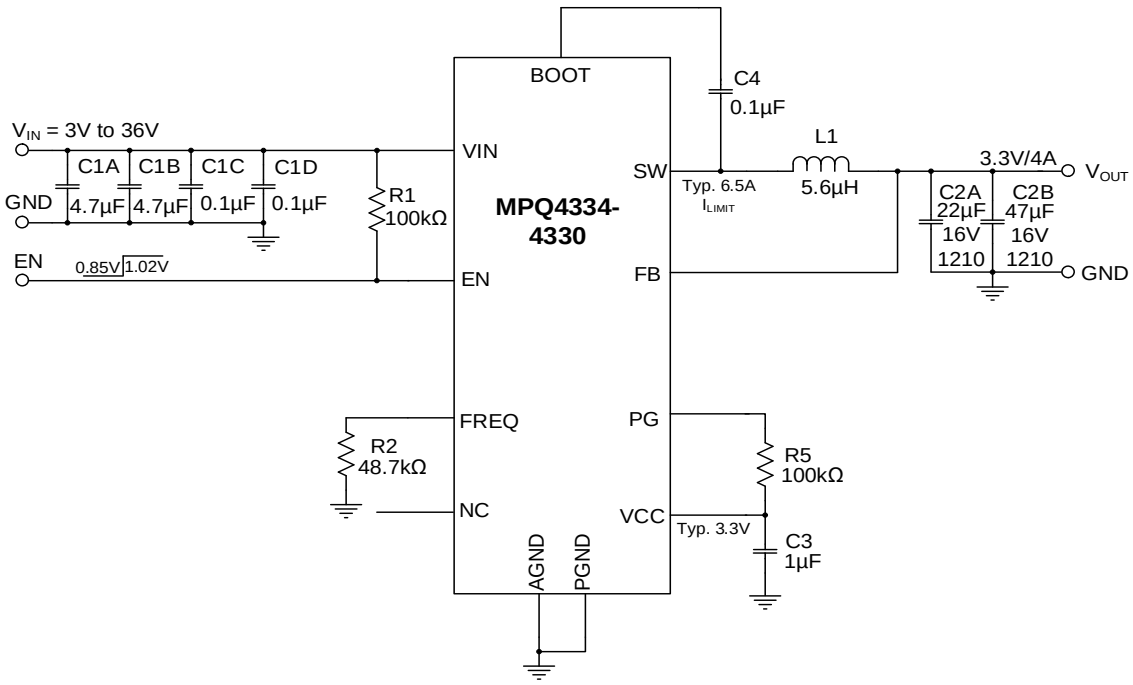


Figure 37: Typical Application Circuit (3.3V Fixed-Output, f_{SW} = 415kHZ, 4A Version)

TYPICAL APPLICATION CIRCUITS *(continued)*

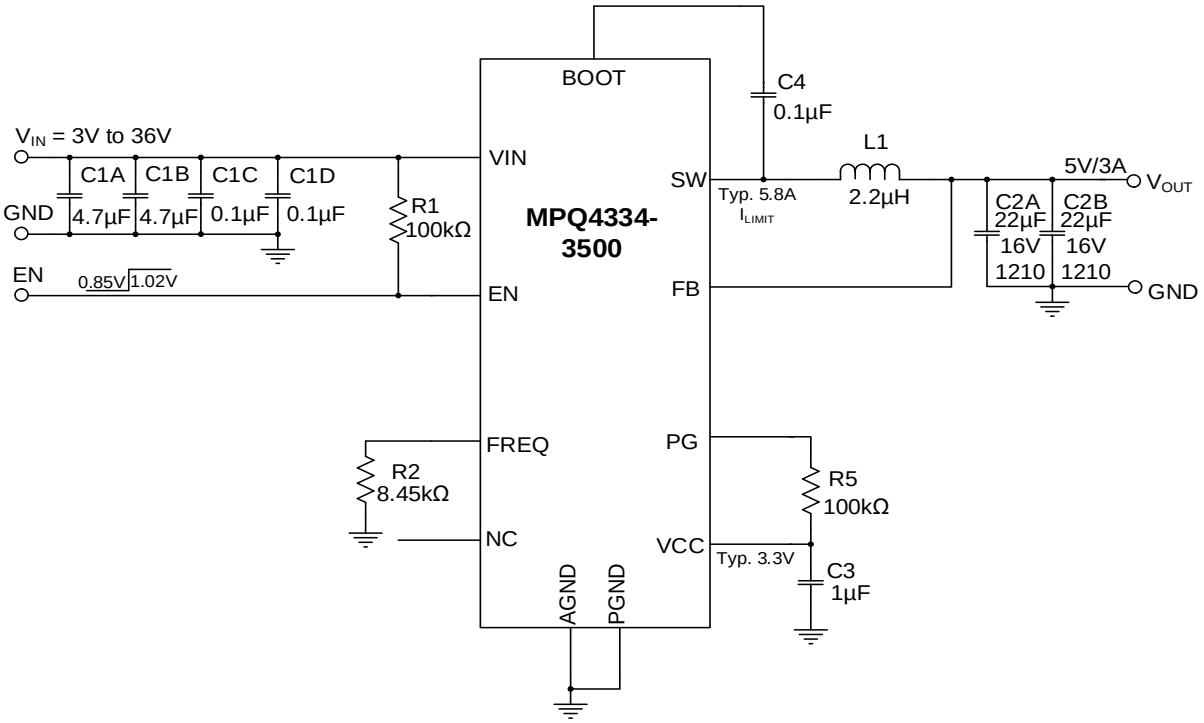


Figure 38: Typical Application Circuit (5V Fixed-Output, f_{SW} = 2.2MHz, 3A Version)

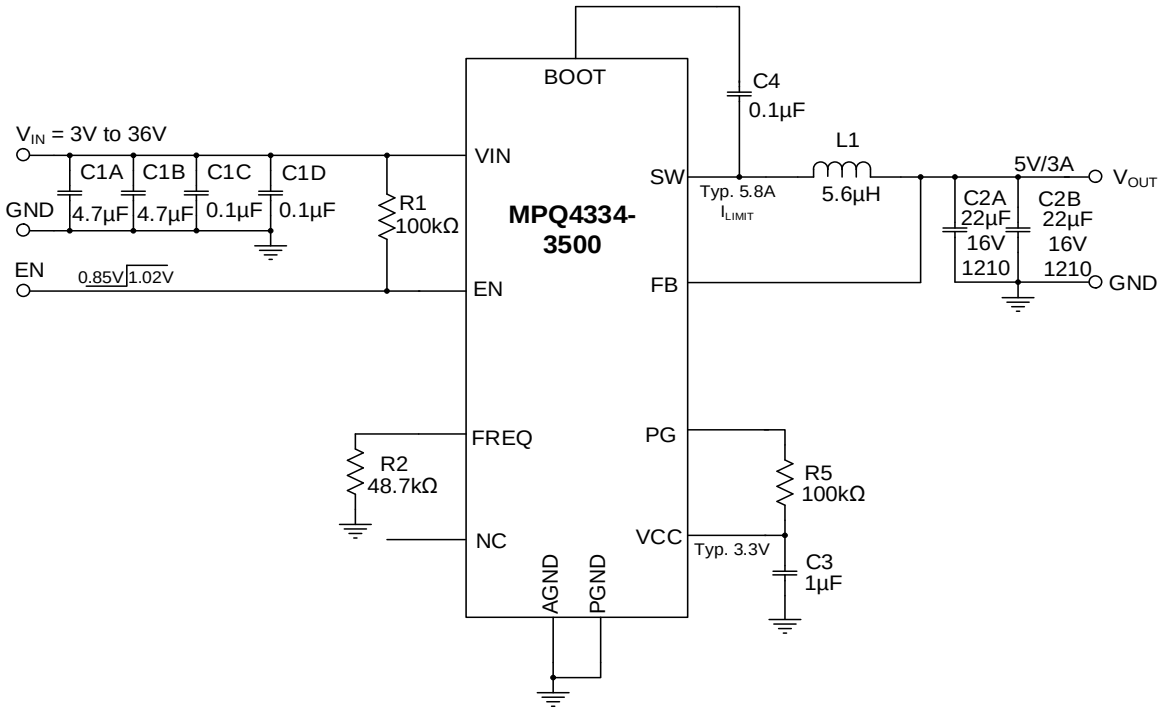


Figure 39: Typical Application Circuit (5V Fixed-Output, f_{SW} = 415kHz, 3A Version)

TYPICAL APPLICATION CIRCUITS *(continued)*

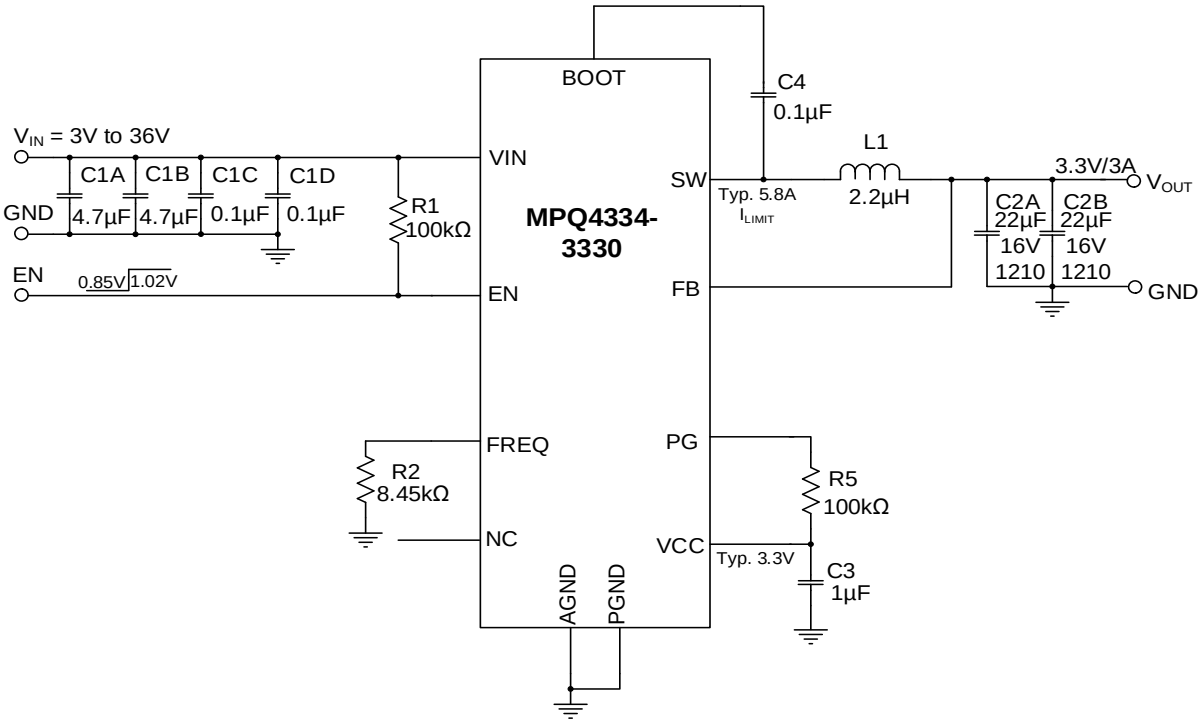


Figure 40: Typical Application Circuit (5V Fixed-Output, f_{SW} = 2.2MHz, 3A Version)

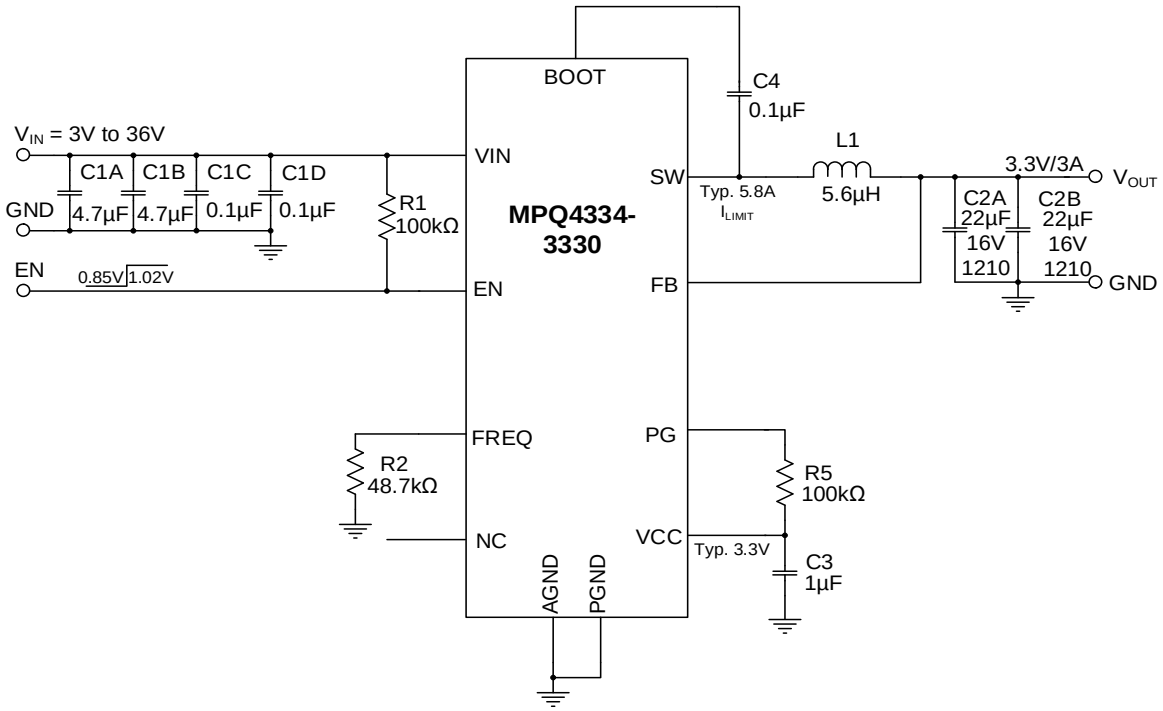


Figure 41: Typical Application Circuit (5V Fixed-Output, f_{SW} = 415kHz, 3A Version)

TYPICAL APPLICATION CIRCUITS *(continued)*

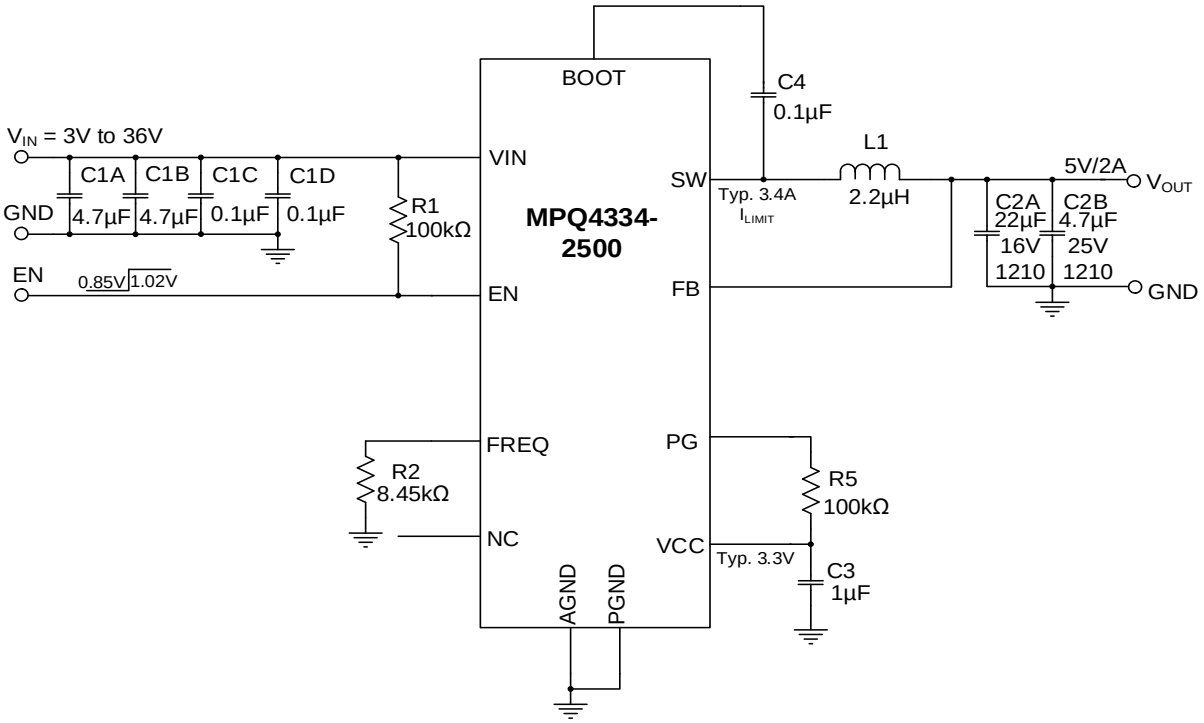


Figure 42: Typical Application Circuit (5V Fixed-Output, f_{SW} = 2.2MHz, 2A Version)

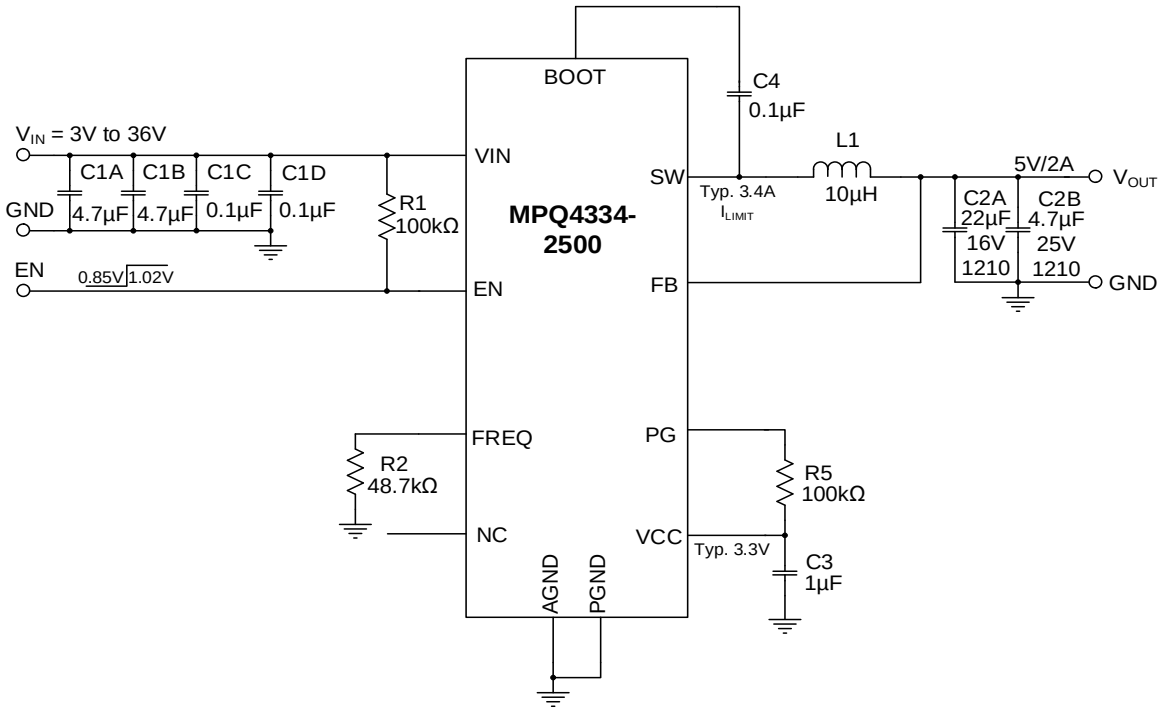


Figure 43: Typical Application Circuit (5V Fixed-Output, f_{SW} = 415kHz, 2A Version)

TYPICAL APPLICATION CIRCUITS *(continued)*

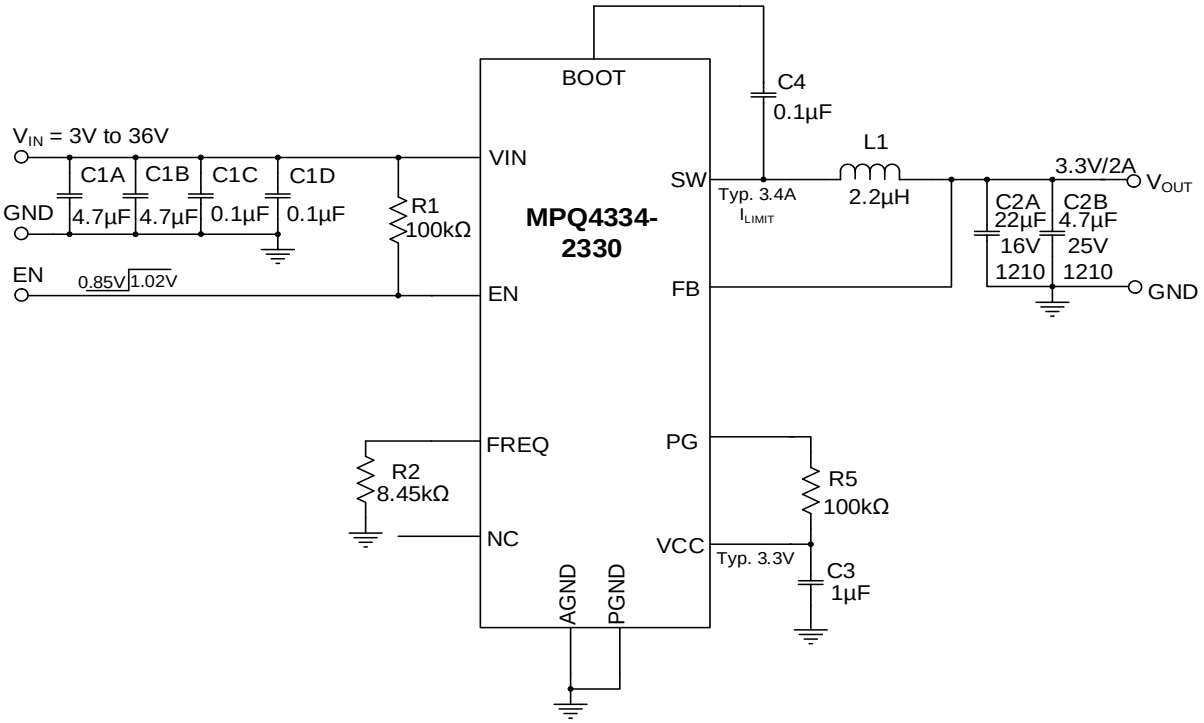


Figure 44: Typical Application Circuit (3.3V Fixed-Output, f_{SW} = 2.2MHz, 2A Version)

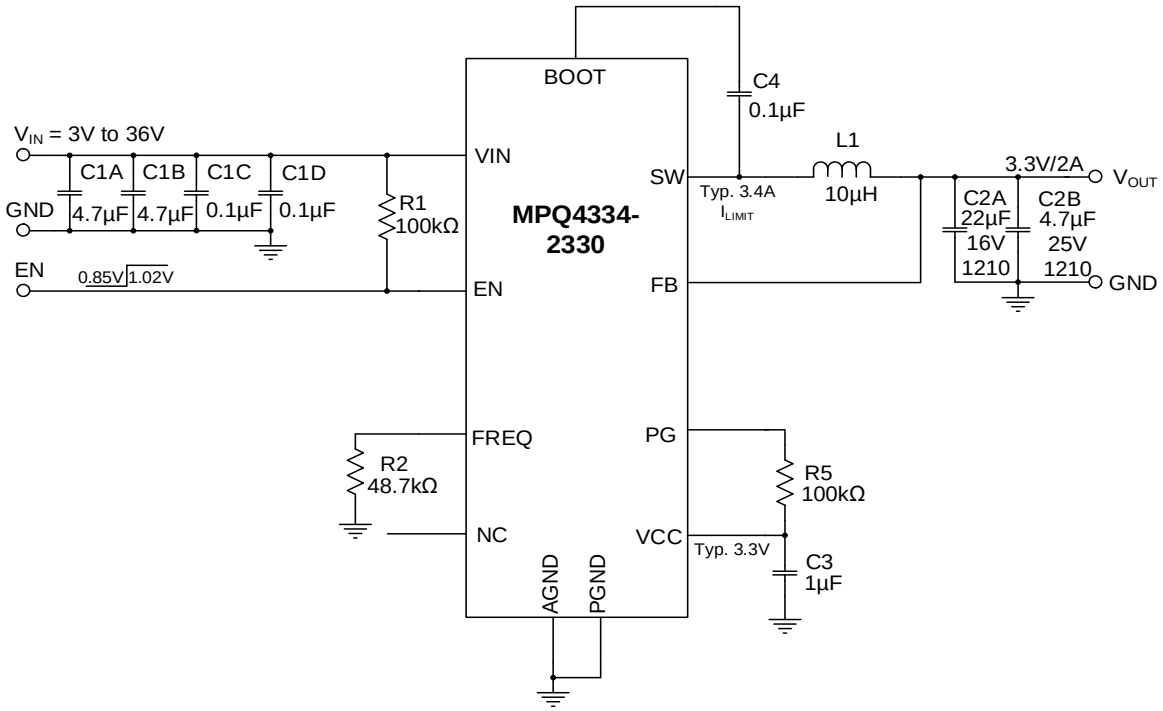


Figure 45: Typical Application Circuit (3.3V Fixed-Output, f_{SW} = 415kHz, 2A Version)

TYPICAL APPLICATION CIRCUITS *(continued)*

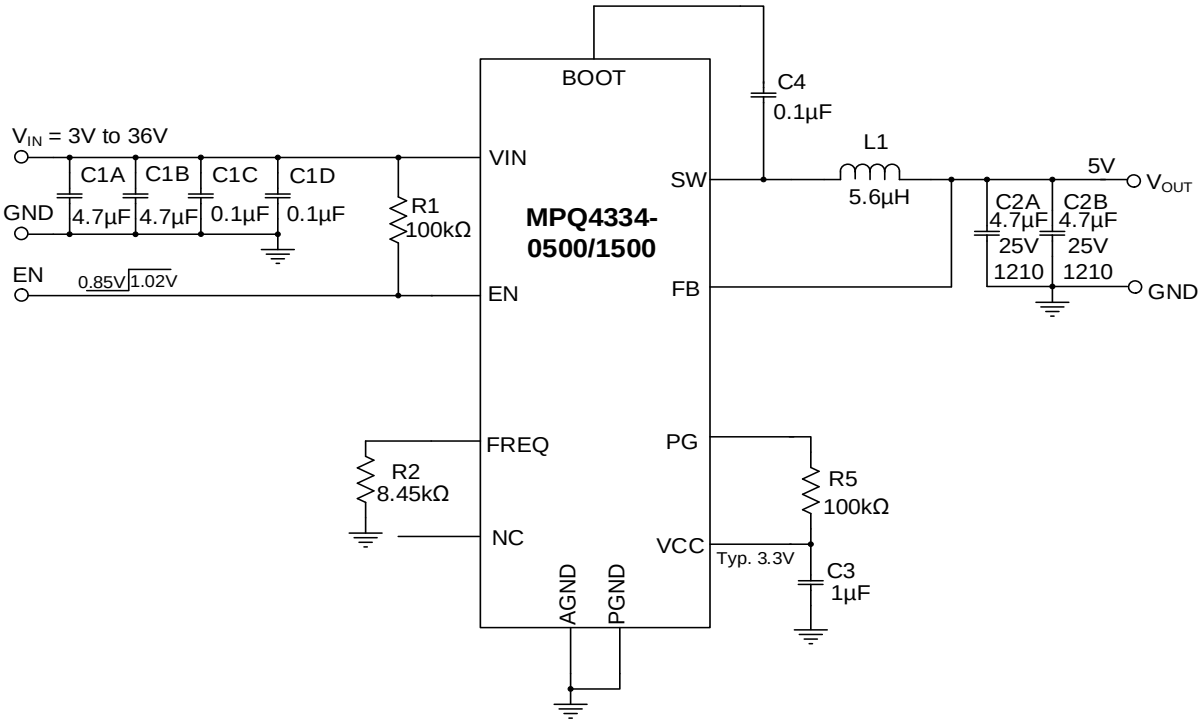


Figure 46: Typical Application Circuit (5V Fixed-Output, f_{SW} = 2.2MHz, 0.5A/1A Version)

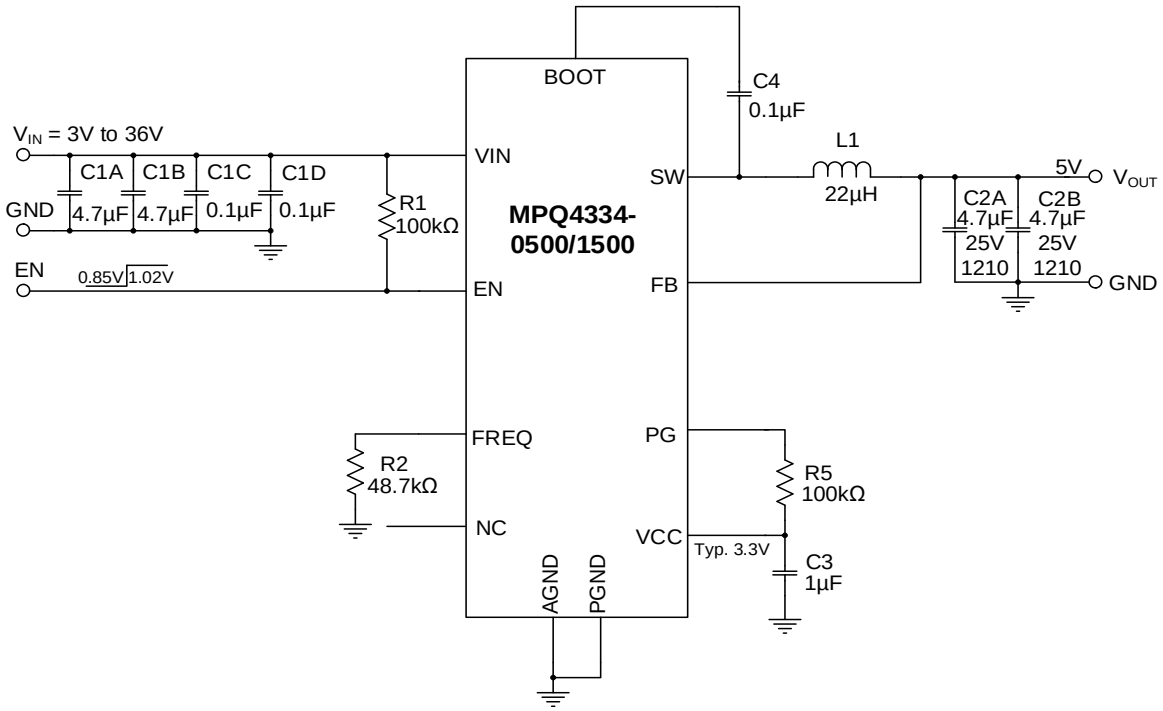


Figure 47: Typical Application Circuit (5V Fixed-Output, f_{SW} = 415kHz, 0.5A/1A Version)

TYPICAL APPLICATION CIRCUITS *(continued)*

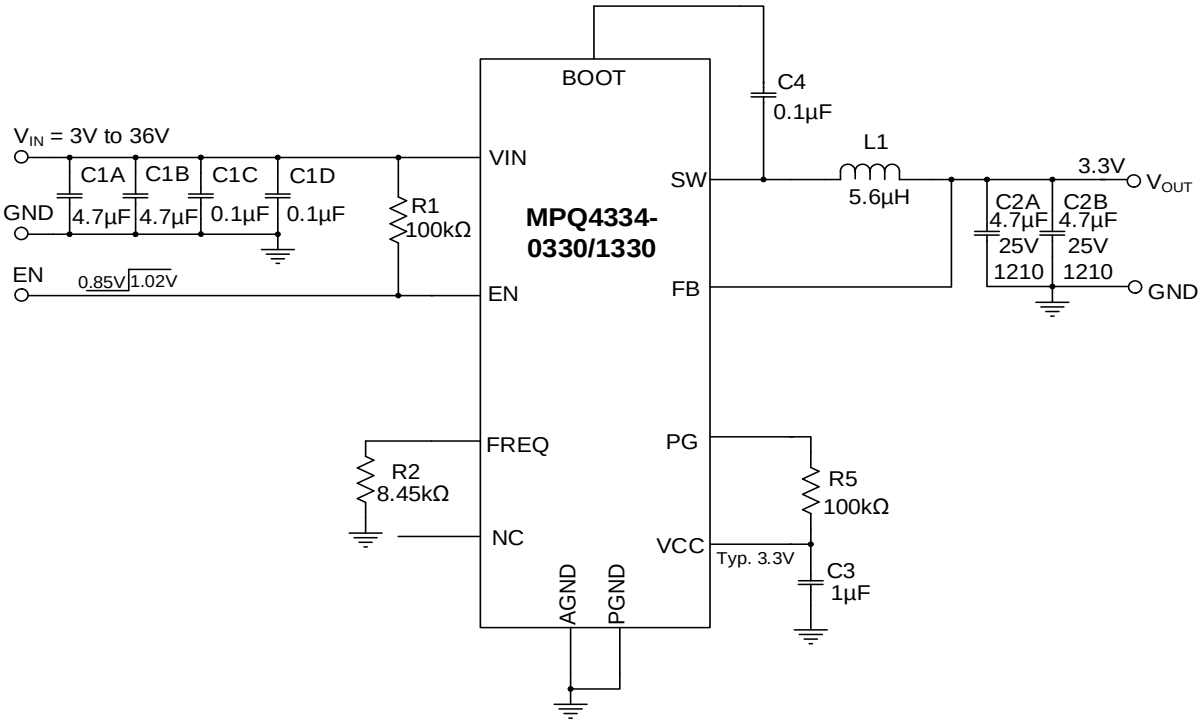


Figure 48: Typical Application Circuit (3.3V Fixed-Output, f_{SW} = 2.2MHz, 0.5A/1A Version)

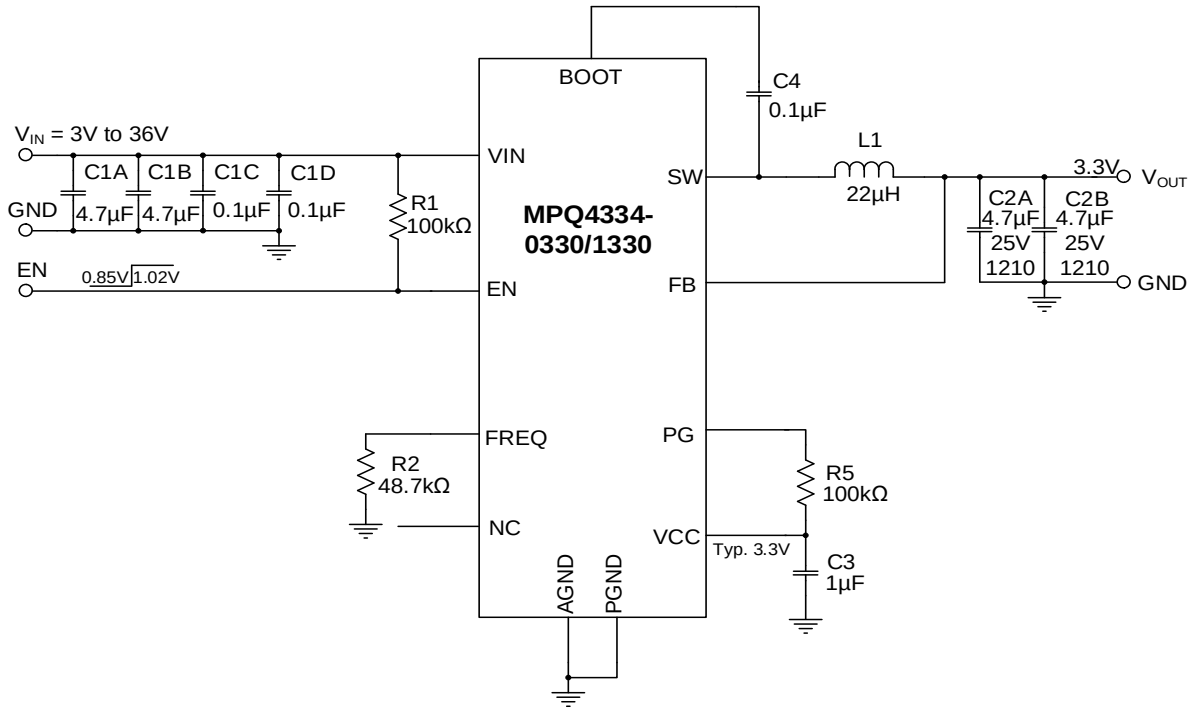


Figure 49: Typical Application Circuit (3.3V Fixed-Output, f_{SW} = 415kHz, 0.5A/1A Version)

TYPICAL APPLICATION CIRCUITS *(continued)*

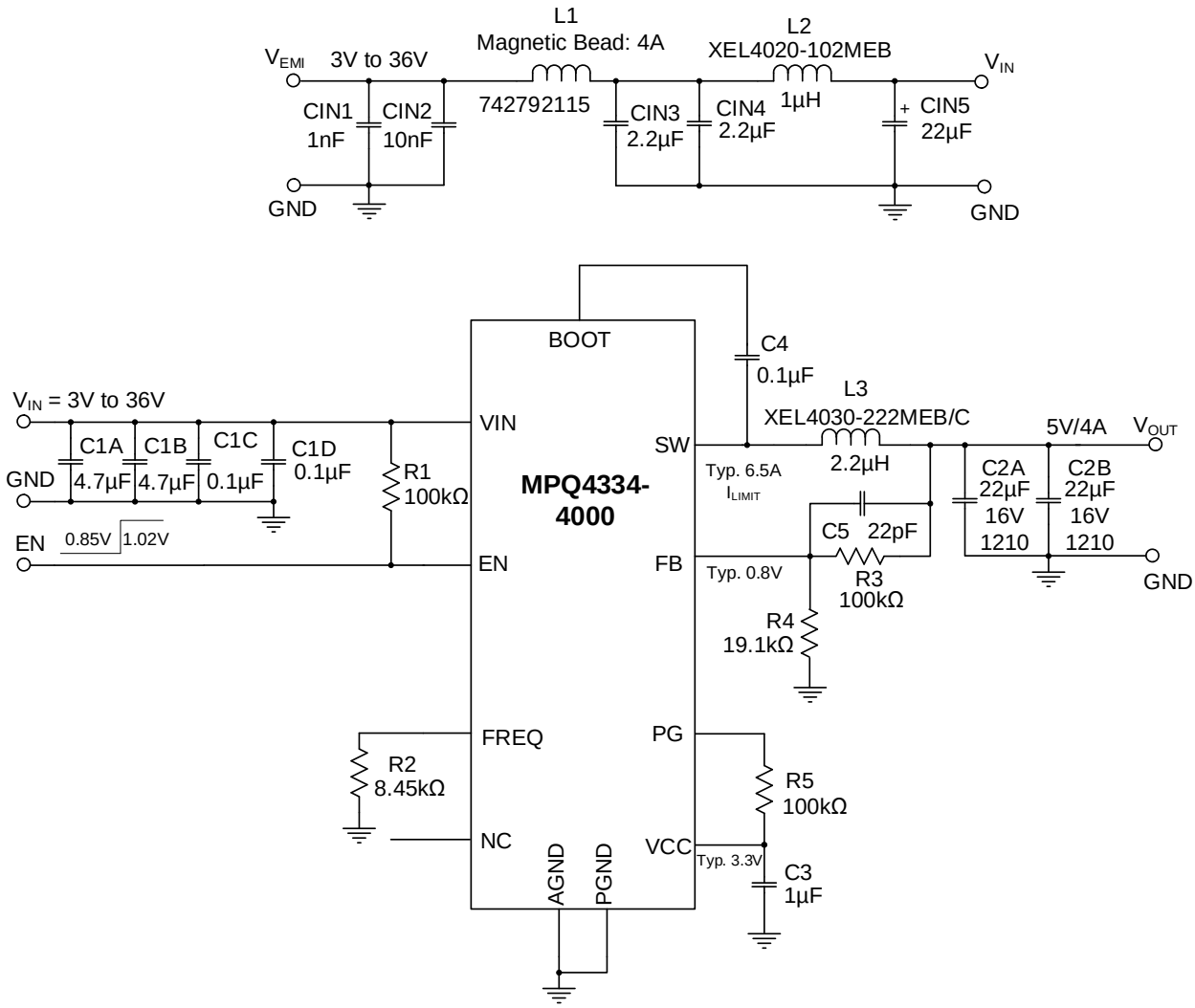


Figure 50: Typical Application Circuit (V_{OUT} = 5V, f_{SW} = 2.2MHz with EMI Filters, 4A Version)

TYPICAL APPLICATION CIRCUITS *(continued)*

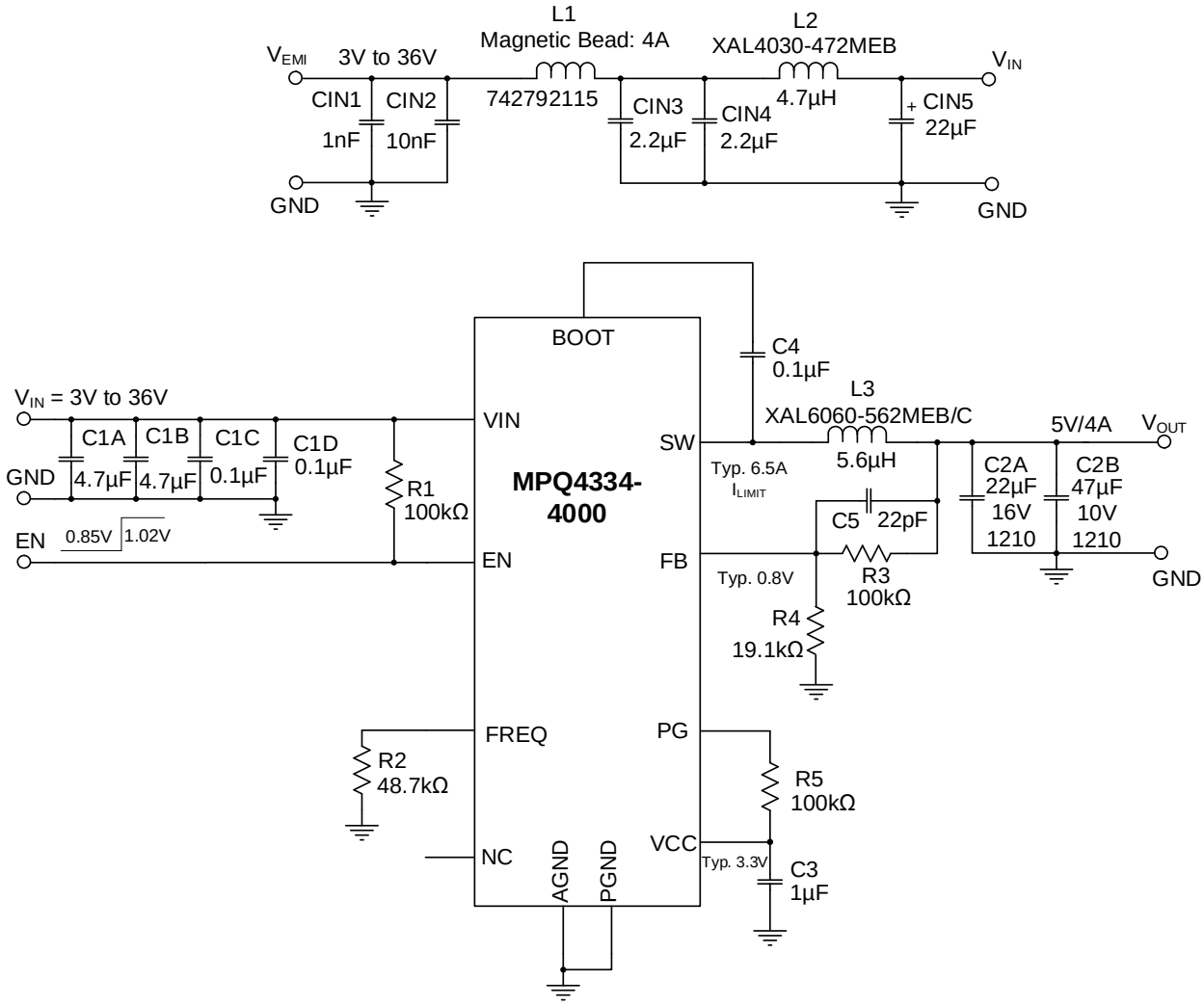
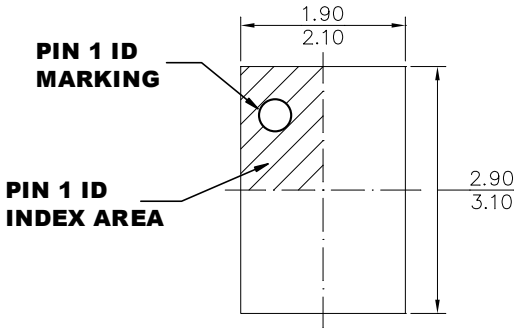


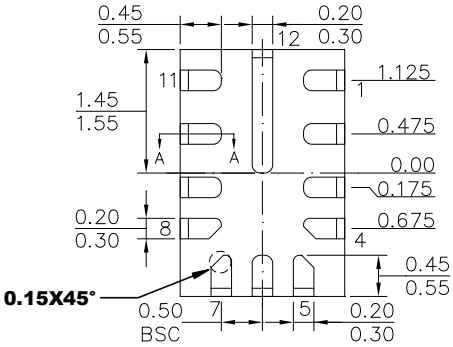
Figure 51: Typical Application Circuit (V_{OUT} = 5V, f_{SW} = 415kHz with EMI Filters, 4A Version)

PACKAGE INFORMATION

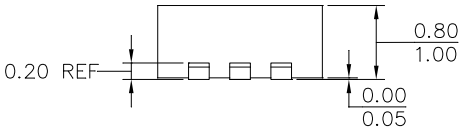
QFN-12 (2mmx3mm)
Wettable Flanks



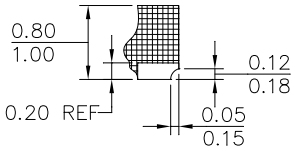
TOP VIEW



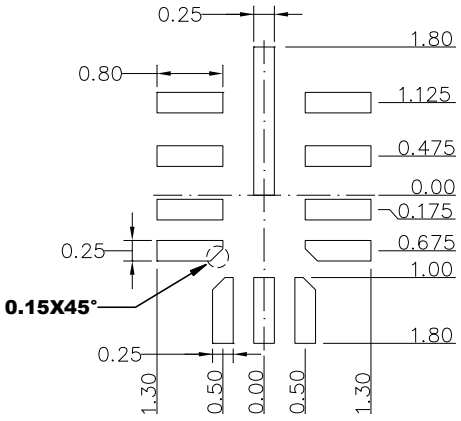
BOTTOM VIEW



SIDE VIEW



SECTION A-A



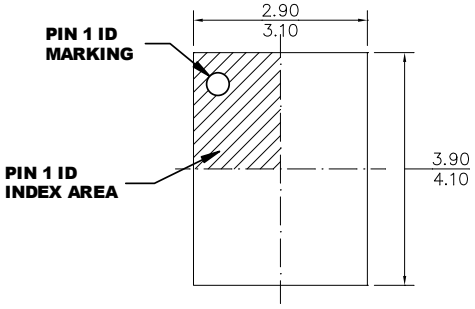
RECOMMENDED LAND PATTERN

NOTE:

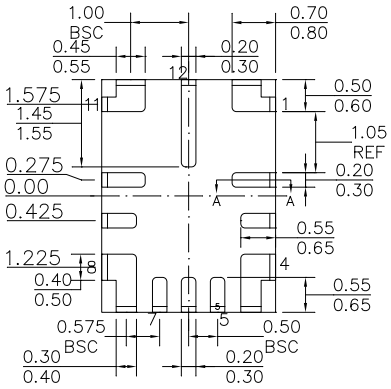
1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

PACKAGE INFORMATION *(continued)*

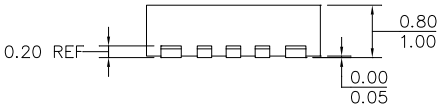
QFN-12 (3mmx4mm)
Wettable Flanks



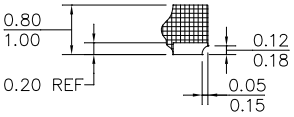
TOP VIEW



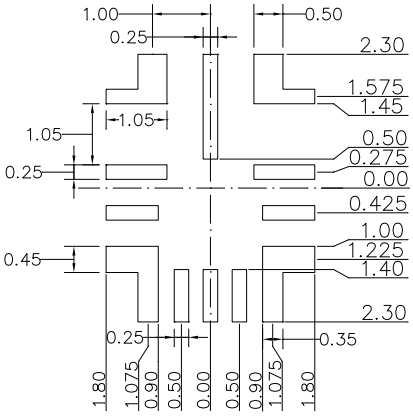
BOTTOM VIEW



SIDE VIEW



SECTION A-A



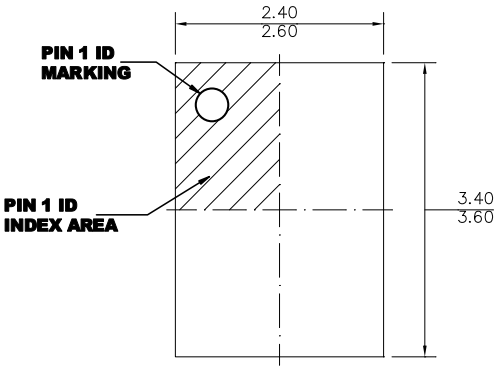
RECOMMENDED LAND PATTERN

NOTE:

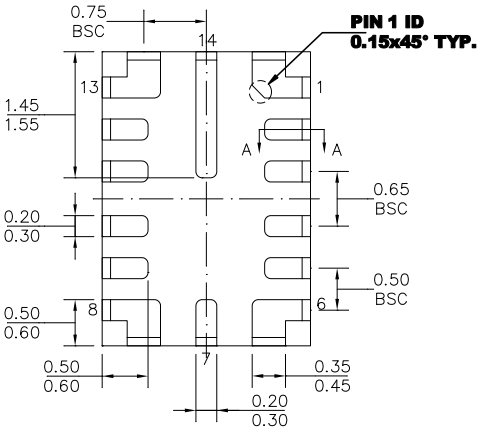
1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

PACKAGE INFORMATION *(continued)*

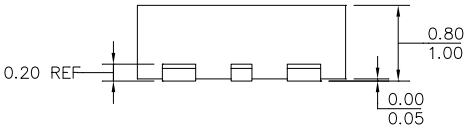
QFN-14 (2.5mmx3.5mm)
Wettable Flanks



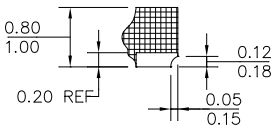
TOP VIEW



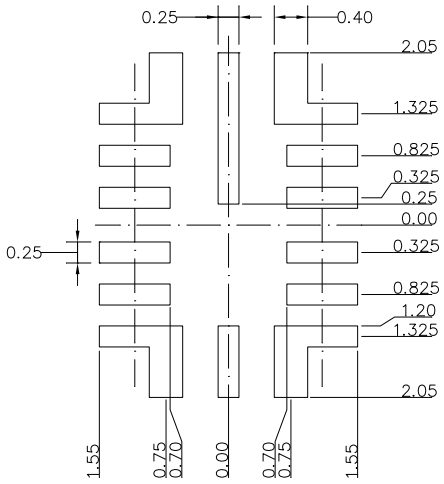
BOTTOM VIEW



SIDE VIEW



SECTION A-A



RECOMMENDED LAND PATTERN

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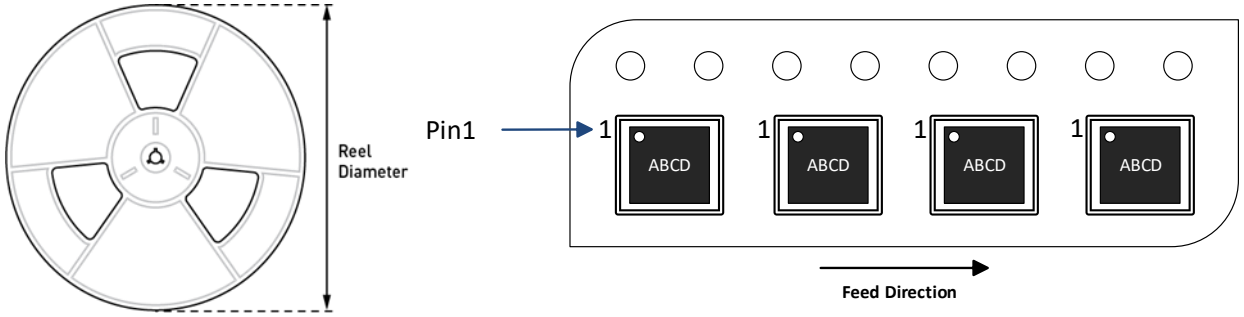
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube (16)	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ4334GDE-xxxx-AEC1-Z	QFN-12 (2mmx3mm)	5000	N/A	N/A	13in	12mm	8mm
MPQ4334GLE-xxxx-AEC1-Z	QFN-12 (3mmx4mm)	5000	N/A	N/A	13in	12mm	8mm
MPQ4334GRHE-xxxx-AEC1-Z	QFN-14 (2.5mmx3.5mm)	5000	N/A	N/A	13in	12mm	8mm

Note:

16) N/A indicates “not available” in tubes. For 500-piece tape & reel prototype quantities, contact the factory. (Order code for 500-piece partial reel is “-P”, tape & reel dimensions remain the same as the full reel.)

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	5/14/2025	Initial Release	-