MPQ77240FS

MPSafe™ ASIL-B/D, 16V, 180mΩ, 0.8A, Quad-Channel, High-Side Switch, AEC-Q100 Qualified

DESCRIPTION

The MPQ77240FS is a quad-channel, smart, high-side power switch for nominal currents up to 0.8A load per channel. The device can support a 5V to 16V input voltage (V_{INx}) range and two different input power rails thanks to its separated power supply design. Back-to-back MOSFET configuration enables short-to-battery protection up to 26V. With a small, 180mΩ on resistance ($R_{DS(ON)}$) in a tiny TQFN-17 (3mmx4mm) package, the MPQ77240FS provides a highly efficient, compact solution for camera load switch applications.

The MPQ77240FS features a configurable, high-accuracy current limit via the I²C interface. This helps to clamp the inrush current under short circuit conditions, which improves system reliability. A selectable start-up slew rate also helps to reduce the inrush current during start-up. In addition, fast-off functionality can quickly turn off the device if the channel current increases sharply. The MPQ77240FS communicates to the MCU via the I²C interface. The device supports up to six addresses, set via an external resistor.

With the help of an internal analog-to-digital converter (ADC), the channel currents, supply voltages, reference voltage (V_{REF}), and output voltages can be obtained without additional external circuitry. Full diagnostics and protection are developed for the device, including input over-voltage (OV) and under-voltage (UV) detection, output OV for each channel, open-load and short-to-battery detection, over-current protection (OCP), fast-off short-circuit protection (SCP) and over-temperature shutdown. Average and peak current detection improves diagnostic reliability in driver monitoring systems (DMS). Fault statuses can be reported via both the FT pin and I²C interface.

As a functional safety device, the MPQ77240FS is AEC-Q100 qualified, designed as an ASIL-B compliant part with well-developed monitoring features, and supports independent power rails. In addition, an 8-bit ADC is integrated to support the readout of real-time current and voltage of each output. With robust diagnostics via the internal 8-bit ADC, the safety coverage can be significantly increased to achieve ASIL-D compliance. Related safety documentation is also provided to aid functional safety design.

FEATURES

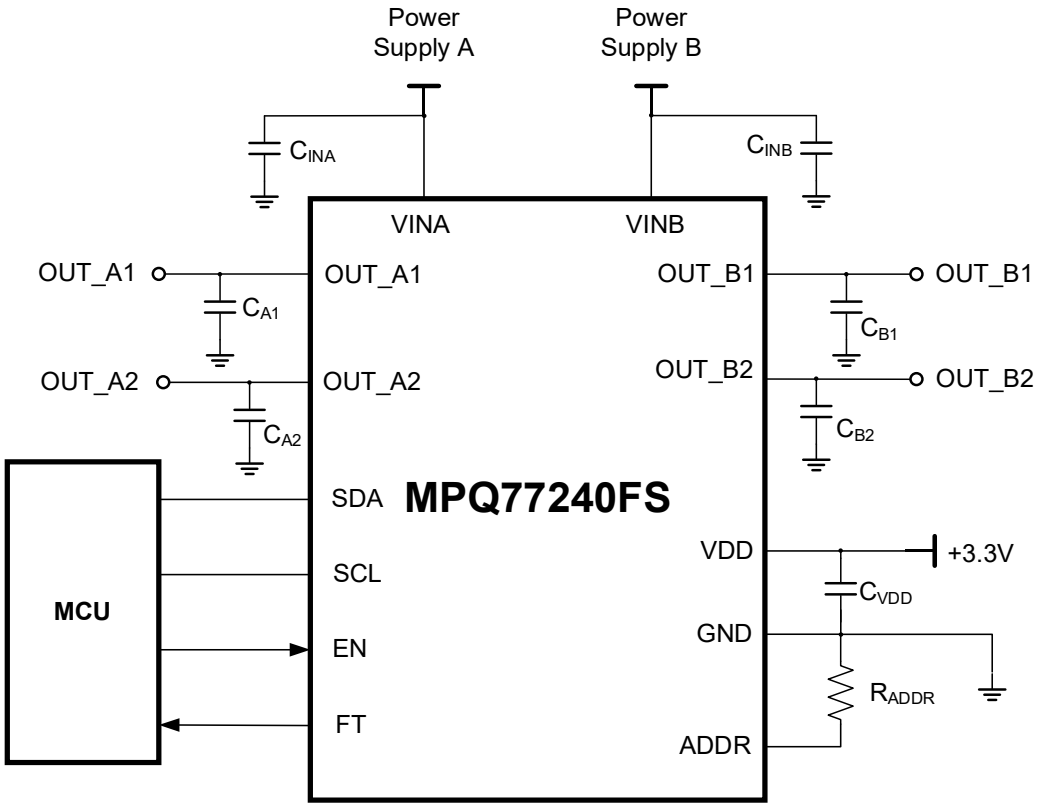
- Designed for Automotive Applications
  - 5V to 16V Input Voltage (V_{INx}) Range
  - 26V Short to Battery Protection with Back-to-Back MOSFET
  - Available in AEC-Q100 Grade 1
- 180mΩ On State Channel Resistance for Cooler Thermals
- Reduces Board Size
  - Available in a TQFN-17 (3mmx4mm) Package with Wettable Flanks
- High-Accuracy Current Sense Capability: ±3% at 1A
- 5μA Low Standby Current Extends Vehicle Battery Life
- Vast Flexibility
  - Separate Power Supply Design Supports Two Power Rails
  - Support Output with Parallel Channels
  - Configurable Current Limit and SS
- Full Diagnostics and Protections
  - Fault Report via FT Pin and I²C
  - I²C Supports 6 Addresses
  - Input OV/UV and Output OV Detection
  - Open-Load and Short-to-Battery Detection
  - Peak and Real-Time Current Sensing
  - Channel Short Circuit and Over-Temperature Protection
  - AEC-Q100-012 Test Grade 1 Compliant
- Functional Safety
  - Integrated 8-Bit ADC to Enhance Diagnostic Coverage
  - ASIL-B/D Compliant
  - ISO 26262 Functional Safety Certified

MPSafe™ Developed for Functional Safety Applications: ISO 26262 Compliant

APPLICATIONS

- Smart High-Side Switch for Cameras and Radars in Infotainment and ADAS Systems
- General Resistive and Capacitive Loads

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating**
MPQ77240FSGLTE-xxxxAEC1***, ****	TQFN-17 (3mmx4mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MPQ77240FSGLTE-xxxxAEC1-Z).

** Moisture Sensitivity Level Rating

*** Wettable Flank

**** “xxxx” is the configuration code identifier for the register settings stored in the OTP register. Each “x” can be a hexadecimal value between 0 and F. The default code is “0000.” Contact an MPS FAE to create this unique number

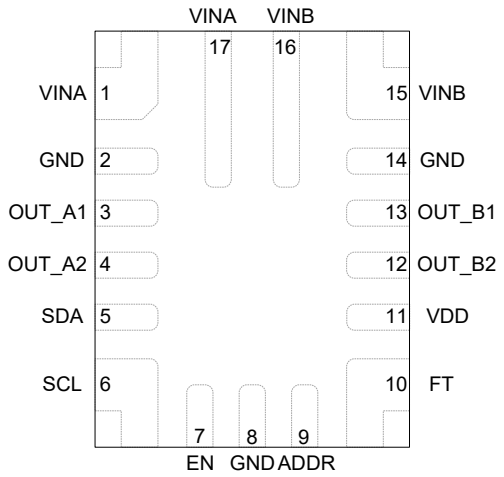
TOP MARKING

MPYW
7724
0LLL
E

MP: MPS prefix
Y: Year code
W: Week code
77240: Part number
LLL: Lot number
E: Wettable Flank

PACKAGE REFERENCE

TOP VIEW



TQFN-17 (3mmx4mm)

PIN FUNCTIONS

Pin #	Name	Description
1, 17	VINA	**Power supply A.** The VINA pins supply power to OUT_A1 and OUT_A2. Connect a 1µF or greater ceramic capacitor between VINA and GND. The VINA and VINB pins can be connected to separate power supplies. If there is only one power rail, connect the VINB pins to the VINA pins.
2, 8, 14	GND	**Device ground.** Connect the GND pins together during PCB layout.
3	OUT_A1	**Channel A1 load output.** Connect a 100nF ceramic capacitor between OUT_A1 and GND.
4	OUT_A2	**Channel A2 load output.** Connect a 100nF ceramic capacitor between OUT_A2 and GND.
5	SDA	**I²C data input/output (I/O).**
6	SCL	**I²C clock input.**
7	EN	**Enable.** Pull EN above the specified threshold (1.2V) to enable the chip; pull EN below threshold (0.9V) to shut down the chip. There is a 500kΩ pull-down resistor internally connected to the EN pin.
9	ADDR	**Address setting pin.** Connect a resistor between the ADDR pin and GND to set the pin address. For more details, see Table 1 on page 25.
10	FT	**Fault output.** The FT pin is an open-drain output. If this pin is used, pull an external power source through a pull-up resistor. When the device is enabled, this pin is pulled low if a fault condition is detected. Float this pin if it is not used.
11	VDD	**Analog supply bypass.** Connect the VDD pin to a 3.3V power rail to supply the internal analog-to-digital converter (ADC) and logic circuit. This pin should also be connected to GND with a 1µF bypass capacitor.
12	OUT_B2	**Channel B2 load output.** Connect a 100nF ceramic capacitor between OUT_B2 and GND.
13	OUT_B1	**Channel B1 load output.** Connect a 100nF ceramic capacitor between OUT_B1 and GND.
15, 16	VINB	**Power supply B.** The VINB pins supply power to OUT_B1 and OUT_B2. Connect a 1µF or greater ceramic capacitor between VINB and GND. The VINA and VINB pins can be connected to separate power supplies. If there is only one power rail, connect the VINB pins to the VINA pins.

ABSOLUTE MAXIMUM RATINGS (1)

VINA/B, OUT_A/B.....-0.3V to +26.5V (2)
VINA/B to OUT_A/B.....-26V to +26.5V (2)
EN.....-0.3V to +20V
All other pins.....-0.3V to +5V
Continuous power dissipation (3) (7).....4.5W
Junction temperature (T_J).....150°C
Lead temperature.....260°C
Storage temperature.....-65°C to +150°C

ESD Ratings

Human body model (HBM).....Class 2 (4)
Charged-device model (CDM).....Class C2b (5)

Recommended Operating Conditions

Supply voltage (V_{INx}).....5V to 16V
Nominal DC load current.....0A to 0.8A
Operating junction temp (T_J).....-40°C to +150°C

Thermal Resistance θ_{JA} θ_{JC}

	θ_{JA}	θ_{JC}	
TQFN-17 (3mmx4mm) (6)	68.7	6.4	°C/W
EVQ77240FS-LT-00A (7)	27.9		°C/W

	Ψ_{JT}	
TQFN-17 (3mmx4mm) (6)	1	°C/W
EVQ77240FS-LT-00A (7)	1.8	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) Absolute maximum ratings are rated under room temperature, unless otherwise noted. Exceeding these ratings may damage the device.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) Per AEC-Q100-002.
5) Per AEC-Q100-011.
6) Obtained based on a JESD51-7, 4-layer PCB. The values given are only valid for comparison with other packages and are not to be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application, and the value of θ_{Jc} shows the thermal resister from junction-to-case bottom. The value of Ψ_{JT} shows the characterization parameter from junction-to-case top.
7) Measured on an MPS standard EVB, 2oz. copper thickness, 4-layer PCB. The value of Ψ_{JT} shows the characterization parameter from junction-to-case top.

ELECTRICAL CHARACTERISTICS

V_{INA} = V_{INB} = 12V, V_{DD} = 3.3V, T_J = -40°C to +150°C, typical values at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Operating and Supply Voltage						
VINA/VINB over-voltage (OV) rising threshold	$V_{IN\_OV\_R}$		16	17	18	V
VINA/VINB OV hysteresis	$V_{IN\_OV\_HYS}$			0.5		V
VINA/VINB under-voltage (UV) falling threshold	$V_{IN\_UV\_F}$	V_{INA} (V_{INB}) < $V_{IN\_UV\_F}$, OUT_A1 (B1) and OUT_A2 (B2) shutdown		2.8	3.8	V
VINA/VINB UV hysteresis	$V_{IN\_UV\_HYS}$			0.3		V
Recommended VDD voltage (V_{DD}) range	V_{DD_REC}		3		3.6	V
V_{DD} UV falling threshold	$V_{DD\_UV\_F}$	V_{DD} < $V_{DD\_UV\_F}$, device shutdown		2.6	2.9	V
V_{DD} UV hysteresis	$V_{DD\_UV\_HYS}$			0.2		V
Operating Current						
Standby current	I_{STBY}	V_{INA} = V_{INB} = 12V, V_{EN} = 0V, T_J = 25°C		5	10	µA
		V_{INA} = V_{INB} = 12V, V_{EN} = 0V, T_J = -40°C to +150°C			28	µA
V_{IN} quiescent current	I_{Q_VIN}	V_{INA} = 12V and V_{INB} = 0V or V_{INA} = 0V and V_{INB} = 12V, V_{EN} = 2V		600	800	µA
V_{DD} quiescent current	I_{Q_VDD}	V_{INA} = 12V and V_{INB} = 0V or V_{INA} = 0V and V_{INB} = 12V, V_{EN} = 2V		1100	1600	µA
MOSFET Parameters						
Channel on resistance	$R_{DS(ON)}$	T_J = 25°C		180	220	mΩ
		T_J = -40°C to +150°C			400	mΩ
EN and FT						
Logic high voltage for EN	$V_{EN,H}$		1	1.2	1.4	V
Logic low voltage for EN	$V_{EN,L}$		0.7	0.9	1.1	V
Hysteresis voltage for EN	$V_{EN,HYS}$			300		mV
Logic low voltage for FT	$V_{FT,L}$	I_{FT} = 1mA			0.2	V
EN pulldown resistor	$R_{EN,pu}$			500		kΩ
Current Limit						
Current limit (8)	CL		1.02	1.2	1.38	A
			0.765	0.9	1.035	
			0.467	0.55	0.633	
			0.175	0.25	0.325	
Soft short circuit deglitch time	t_{SSC_DE}	Current limit triggered, channel shutdown after t_{SSC_DE}		0.5		ms
Short circuit recovery delay	$t_{SC,RST}$	Output short circuit shutdown, channel auto-recovers after $t_{SC,RST}$		300		ms

ELECTRICAL CHARACTERISTICS *(continued)*

V_{INA} = V_{INB} = 12V, V_{DD} = 3.3V, T_J = -40°C to +150°C, typical values at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Diagnostics and Protection						
OUT OV threshold	V_{OOV_STD}	V_{OUT} - V_{IN} > V_{OOV_STD}, channel shutdown	0.05	0.15	0.25	V
OUT OV hysteresis	V_{OOV_HYS}			50		mV
OUT OV deglitch time	t_{OOV_DS}			10		µs
Thermal shutdown threshold (9)	T_{SD}	T_J > T_{SD}, device shutdown		175		°C
Thermal shutdown hysteresis (9)	T_{SD_HYS}			25		°C
Thermal warning threshold (9)	T_{WR}	T_J > T_{WR}, thermal warning is detected via the I^2C interface		140		°C
Thermal warning hysteresis (9)	T_{WR_HYS}			25		°C
Analog-to-Digital Converter (ADC) Configuration						
Normal supply range	V_{DD_ADC}	ADC accuracy is ensured	3	3.3	3.6	V
Parameter Sensing Accuracy (including ADC Error)						
V_{IN} and V_{OUT} reading accuracy	ΔV/V		-3.5%		+3.5%	
V_{DD} reading accuracy	$\Delta V_{DD}/V_{DD}$		-4%		+4%	
OUT_A1, OUT_B1 current reading accuracy	$\Delta I_{A(B)1}/I_{A(B)1}$	I_{OUT} = 1A, T_J = 25°C	-3%		+3%	
		I_{OUT} = 1A, T_J = -40°C to +150°C	-5%		+5%	
		I_{OUT} = 300mA, T_J = 25°C	-5%		+5%	
		I_{OUT} = 300mA, T_J = -40°C to +150°C	-7.5%		+7.5%	
		I_{OUT} = 100mA, T_J = 25°C	-10%		+10%	
		I_{OUT} = 100mA, T_J = -40°C to +150°C	-15%		+15%	
		I_{OUT} = 30mA, T_J = -40°C to +150°C	-67%		+67%	
OUT_A2, OUT_B2 current reading accuracy	$\Delta I_{A(B)2}/I_{A(B)2}$	I_{OUT} = 1A, T_J = 25°C	-3%		+3%	
		I_{OUT} = 1A, T_J = -40°C to +150°C	-7.5%		+7.5%	
		I_{OUT} = 300mA, T_J = 25°C	-5%		+5%	
		I_{OUT} = 300mA, T_J = -40°C to +150°C	-9%		+9%	
		I_{OUT} = 100mA, T_J = 25°C	-10%		+10%	
		I_{OUT} = 100mA, T_J = -40°C to +150°C	-25%		+25%	
		I_{OUT} = 30mA, T_J = -40°C to +150°C	-67%		+67%	
I^2C Configuration (9)						
Input logic high	V_{IH}		1.3			V
Input logic low	V_{IL}				0.5	V
Output logic low	V_{OL}				0.1	V
SCL clock frequency	f_{SCL}				1	MHz
SCL high time	t_{HIGH}		0.26			µs
Scl low time	t_{LOW}		0.5			µs
Data set-up time	$t_{SU,DAT}$		50			ns
Data hold time	$t_{HD,DAT}$		0			µs

ELECTRICAL CHARACTERISTICS *(continued)*

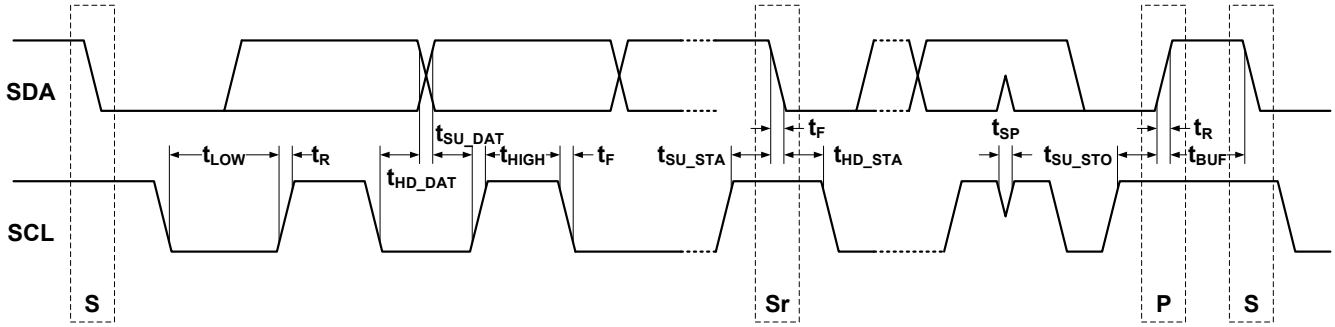
V_{INA} = V_{INB} = 12V, V_{DD} = 3.3V, T_J = -40°C to +150°C, typical values at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
I²C Configuration (9)						
Repeated start set-up time	$t_{SU,STA}$		0.26			µs
Repeated start hold time	$t_{HD,STA}$		0.26			µs
Bus free time between a stop and start condition	t_{BUF}		0.5			µs
Stop set-up time	$t_{SU,STO}$		0.26			µs
SCL and SDA rise time	t_R				120	ns
SCL and SDA fall time	t_F		20 x (V_{DD} / 5.5V)		120	ns
Pulse width for suppressed spike	t_{SP}		0		50	ns
Capacitance for each bus line	C_B				550	pF

Notes:

8) Write to the relevant register to update this parameter.
9) Derived from bench characterization; not tested in production.

I²C TIMING DIAGRAM



S: Start Condition

Sr: Repeated Start Condition

P: Stop Condition

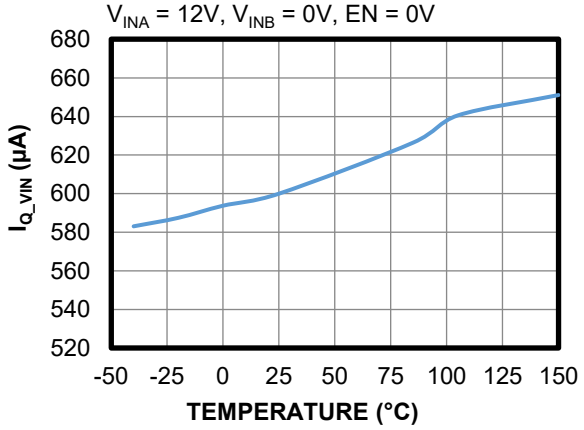
Figure 1: I²C-Compatible Interface Timing Diagram

TYPICAL CHARACTERISTICS

V_{INA} = V_{INB} = 12V, V_{DD} = 3.3V, unless otherwise noted.

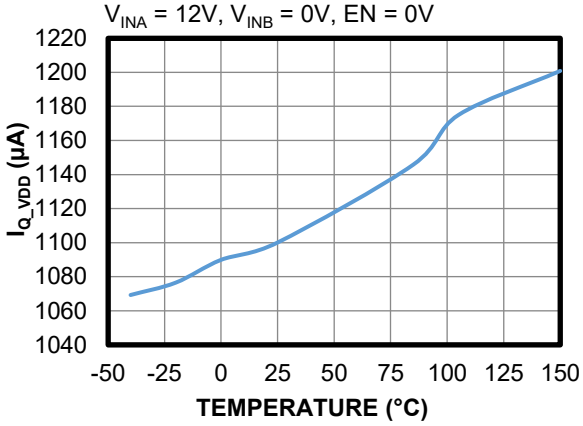
V_{IN} Quiescent Current vs. Temperature

V_{INA} = 12V, V_{INB} = 0V, EN = 0V



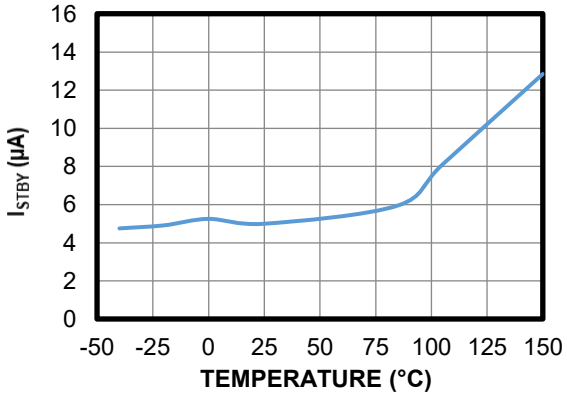
V_{DD} Quiescent Current vs. Temperature

V_{INA} = 12V, V_{INB} = 0V, EN = 0V

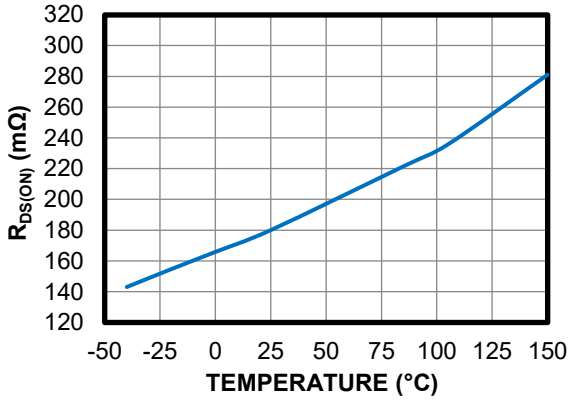


Standby Current vs. Temperature

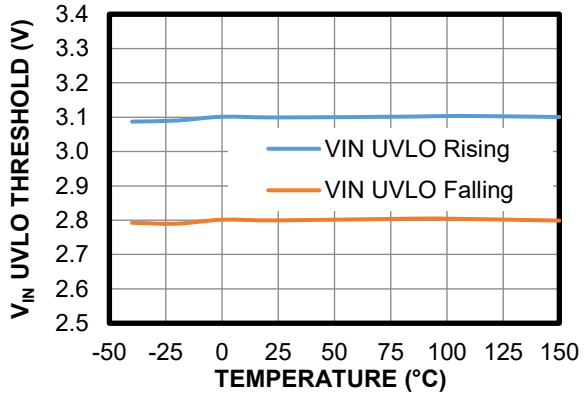
EN = 0V



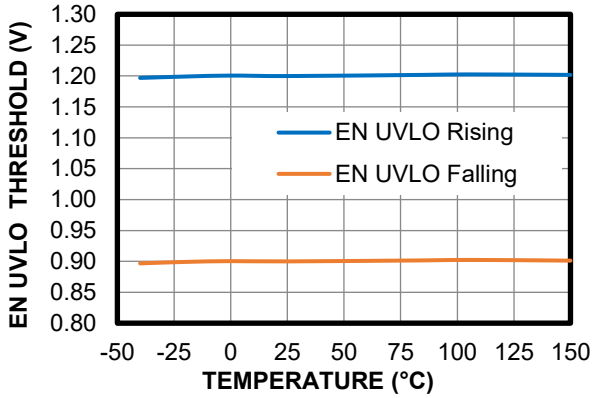
On Resistance vs. Temperature



VINA/VINB UVLO Threshold vs. Temperature



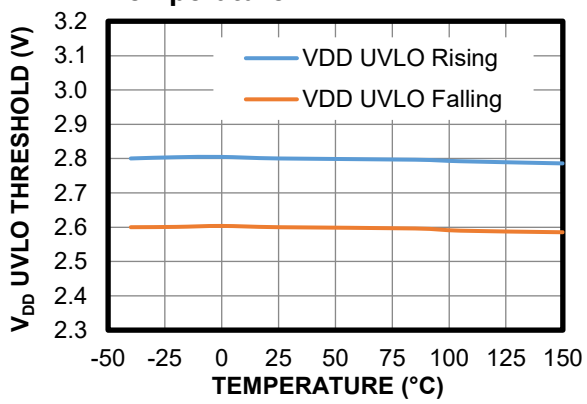
EN UVLO Threshold vs. Temperature



TYPICAL CHARACTERISTICS *(continued)*

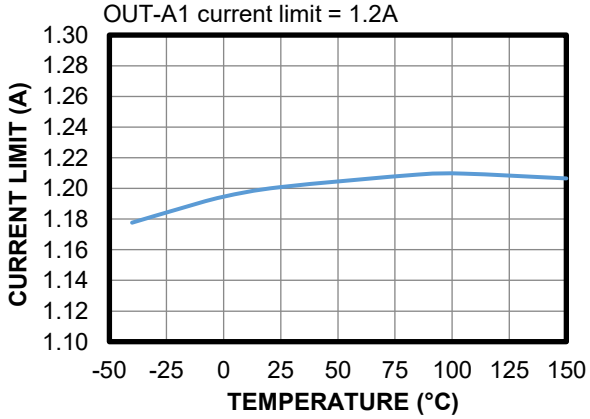
V_{INA} = V_{INB} = 12V, V_{DD} = 3.3V, unless otherwise noted.

V_{DD} UVLO Threshold vs. Temperature



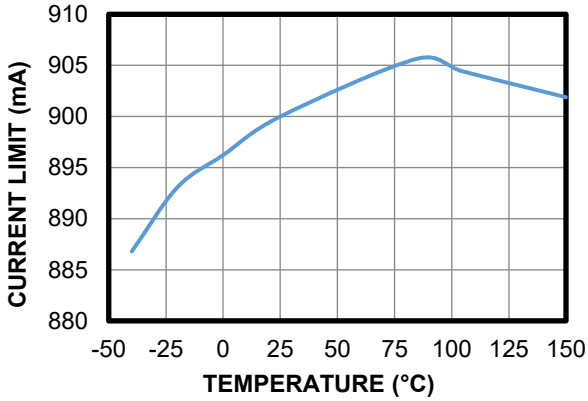
Current Limit vs. Temperature

OUT-A1 current limit = 1.2A



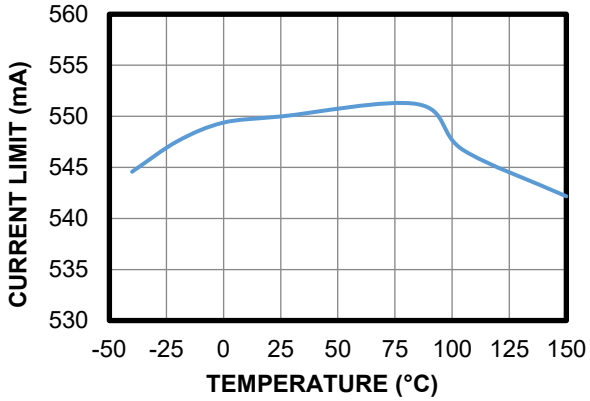
Current Limit vs. Temperature

OUT-A1 current limit = 0.9A



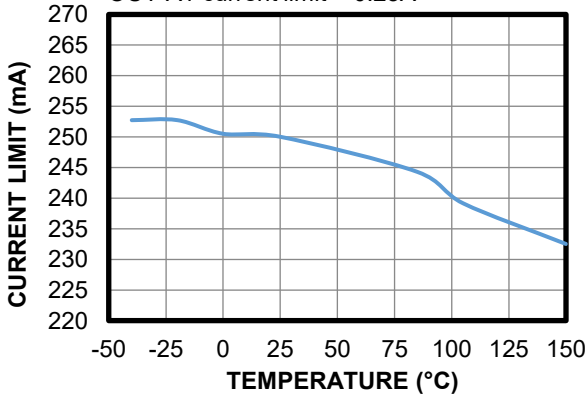
Current Limit vs. Temperature

OUT-A1 current limit = 0.55A

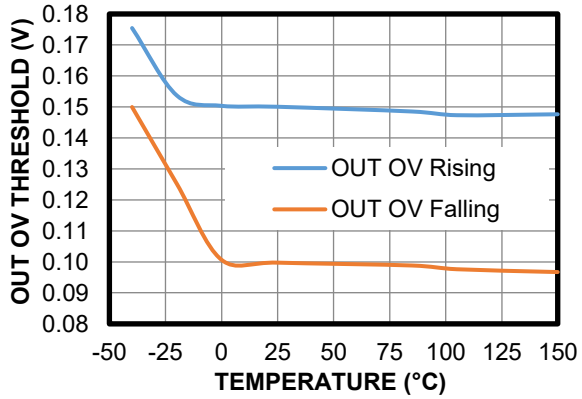


Current Limit vs. Temperature

OUT-A1 current limit = 0.25A



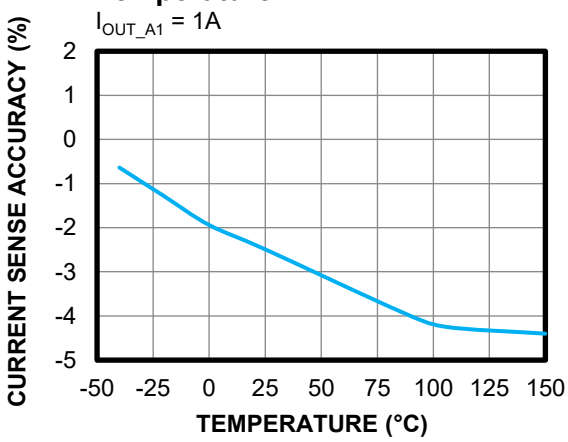
OUT Over-Voltage (OV) Threshold vs. Temperature



TYPICAL CHARACTERISTICS *(continued)*

V_{INA} = V_{INB} = 12V, V_{DD} = 3.3V, T_A = 25°C, unless otherwise noted.

Current-Sence Accuracy vs. Temperature

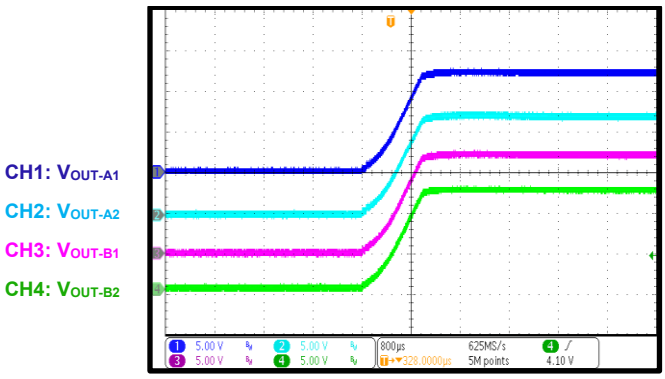


TYPICAL PERFORMANCE CHARACTERISTICS

V_{INA} = V_{INB} = 12V, V_{DD} = 3.3V, t_{SS} = 1ms, T_A = 25°C, unless otherwise noted.

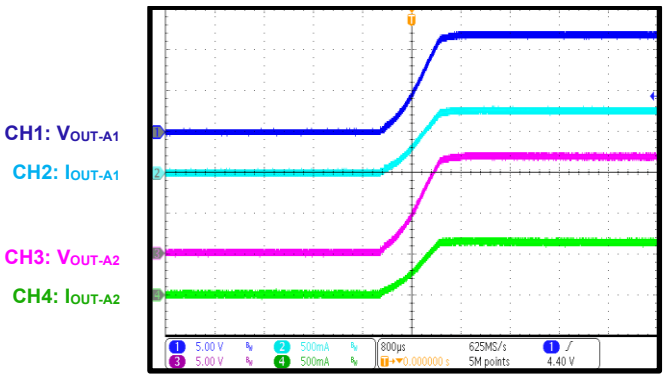
Start-Up through VIN

All I_{OUT} = 0A



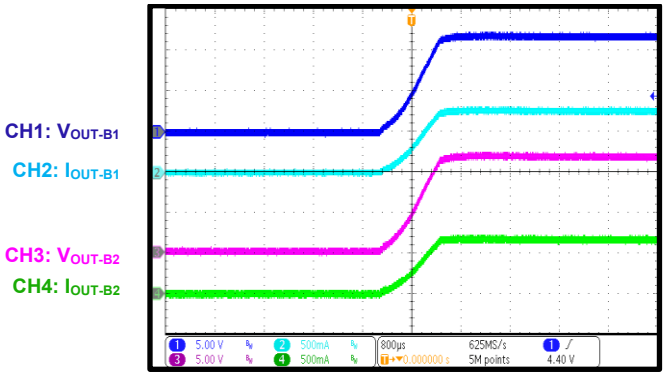
Start-Up through VIN

All I_{OUT} = 0.8A



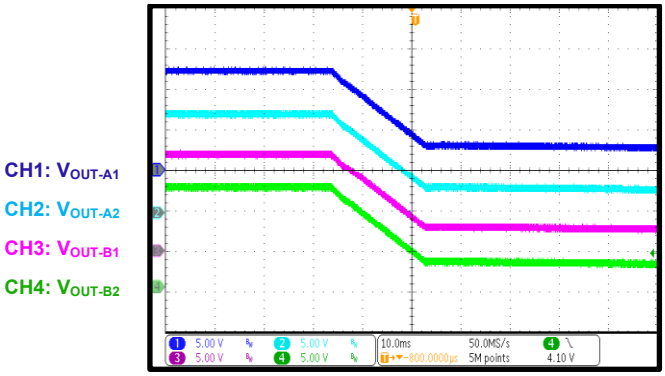
Start-Up through VIN

All I_{OUT} = 0.8A



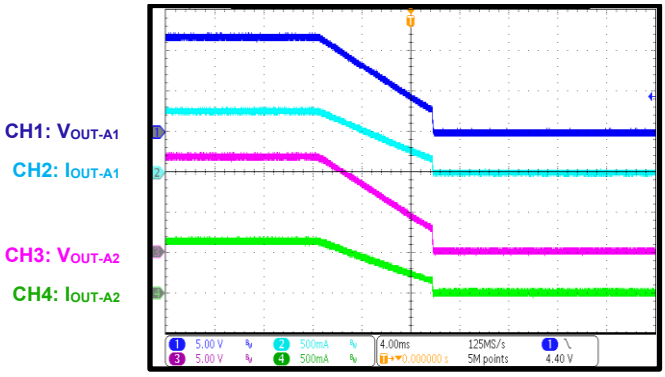
Shutdown through VIN

All I_{OUT} = 0A



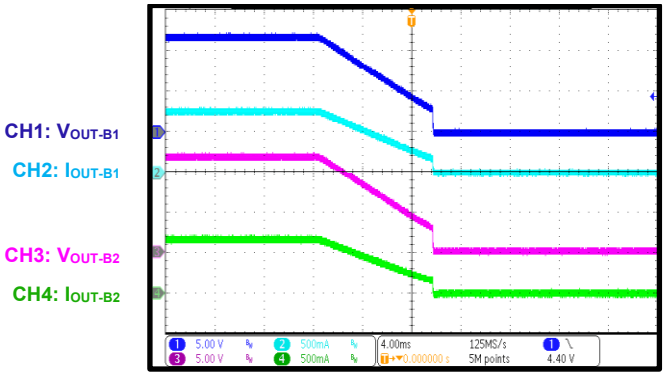
Shutdown through VIN

All I_{OUT} = 0.8A



Shutdown through VIN

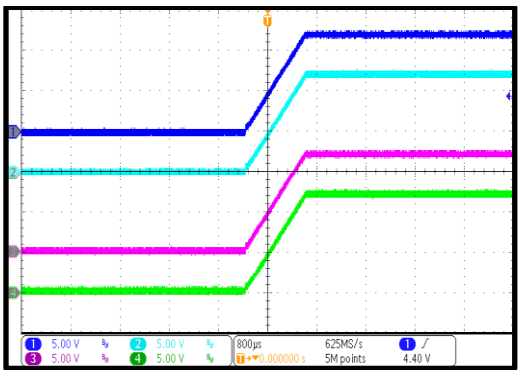
All I_{OUT} = 0.8A



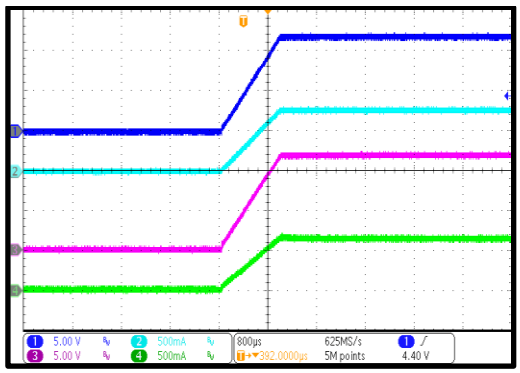
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{INA} = V_{INB} = 12V, V_{DD} = 3.3V, t_{SS} = 1ms, T_A = 25°C, unless otherwise noted.

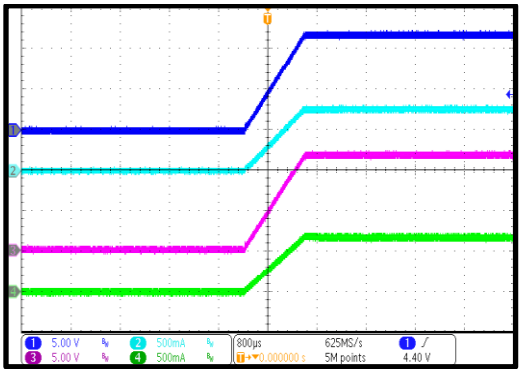
Start-Up through EN Channel
All I_{OUT} = 0A



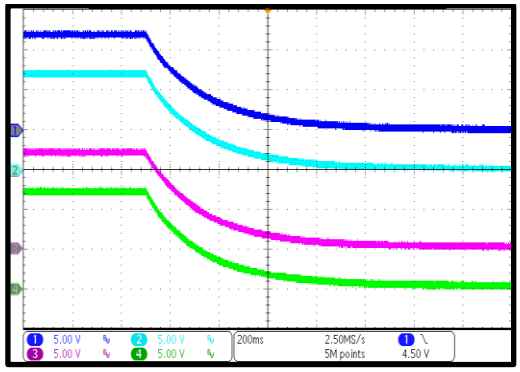
Start-Up through EN Channel
All I_{OUT} = 0.8A



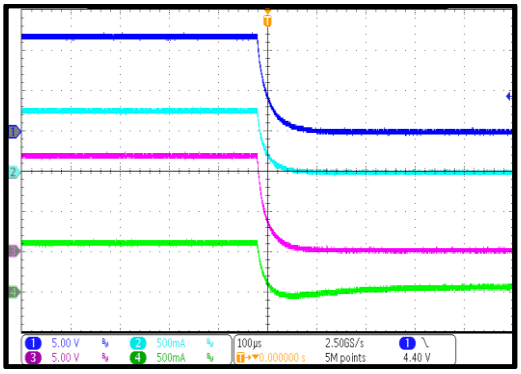
Start-Up through EN Channel
All I_{OUT} = 0.8A



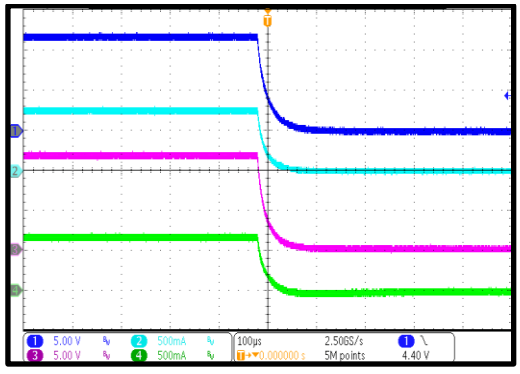
Shutdown through EN Channel
All I_{OUT} = 0A



Shutdown through EN Channel
All I_{OUT} = 0.8A



Shutdown through EN Channel
All I_{OUT} = 0.8A

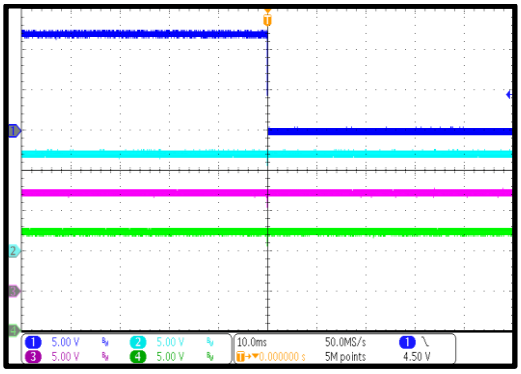


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{INA} = V_{INB} = 12V, V_{DD} = 3.3V, t_{SS} = 1ms, T_A = 25°C, unless otherwise noted.

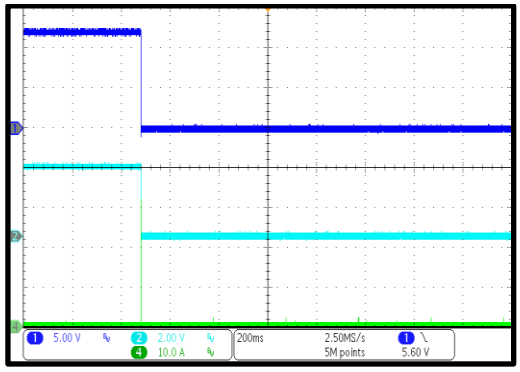
SCP Entry

All I_{OUT} = 0A, OUT_A1 SCP in auto-recovery mode



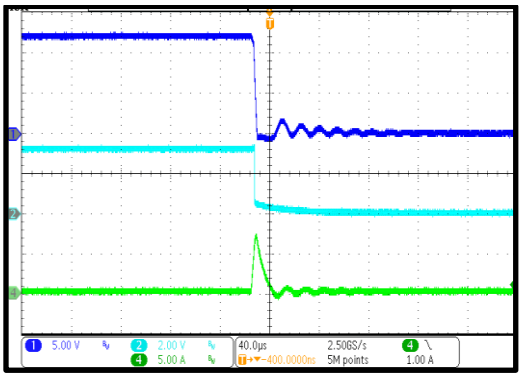
SCP Entry

All I_{OUT} = 0A, OUT_A1 SCP in auto-recovery mode



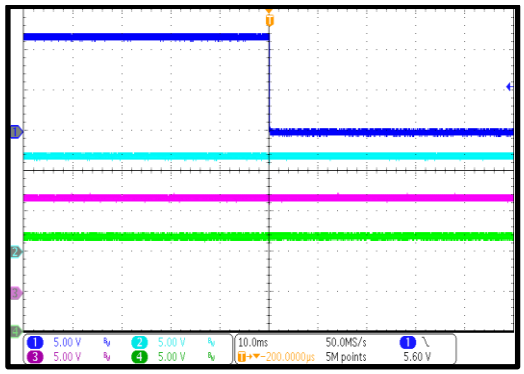
SCP Entry

All I_{OUT} = 0A, OUT_A1 SCP in auto-recovery mode



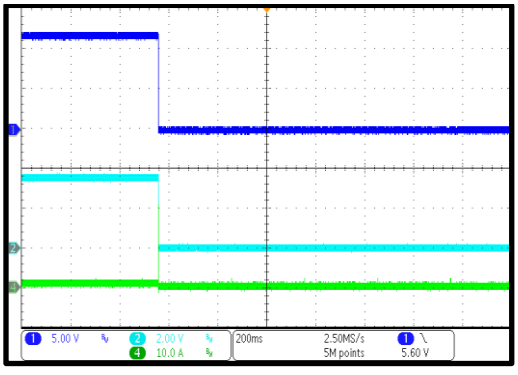
SCP Entry

All I_{OUT} = 0.8A, OUT_A1 SCP in auto-recovery mode



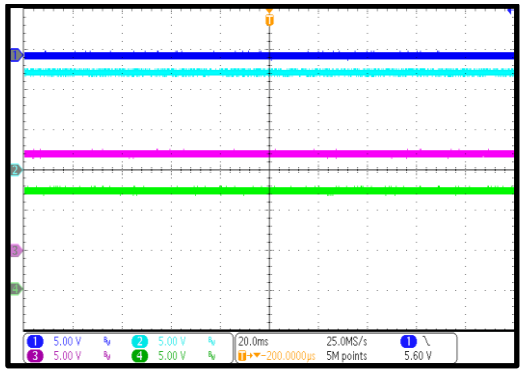
SCP Entry

All I_{OUT} = 0.8A, OUT_A1 SCP in auto-recovery mode



SCP Steady State

All I_{OUT} = 0.8A, OUT_A1 SCP in auto-recovery mode

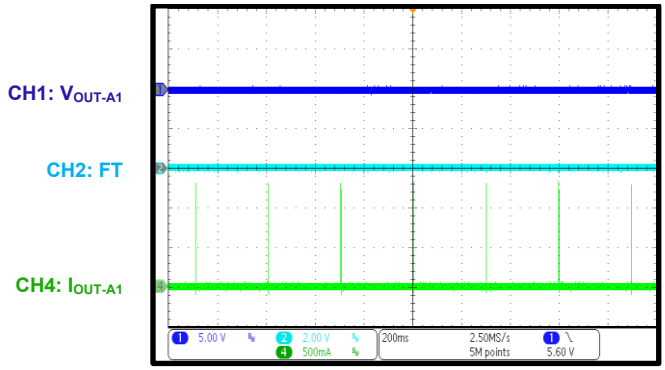


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{INA} = V_{INB} = 12V, V_{DD} = 3.3V, t_{SS} = 1ms, T_A = 25°C, unless otherwise noted.

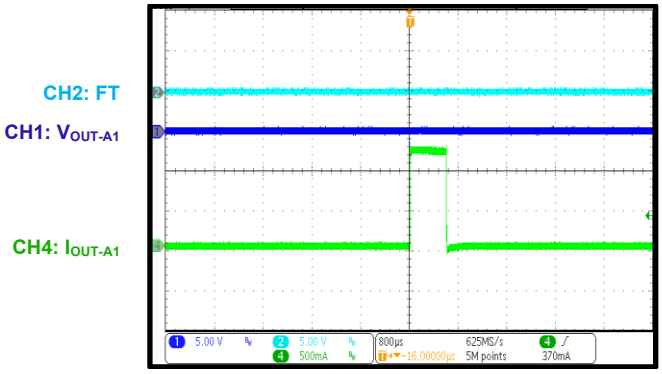
SCP Steady State

All I_{OUT} = 0.8A, OUT_A1 SCP in auto-recovery mode



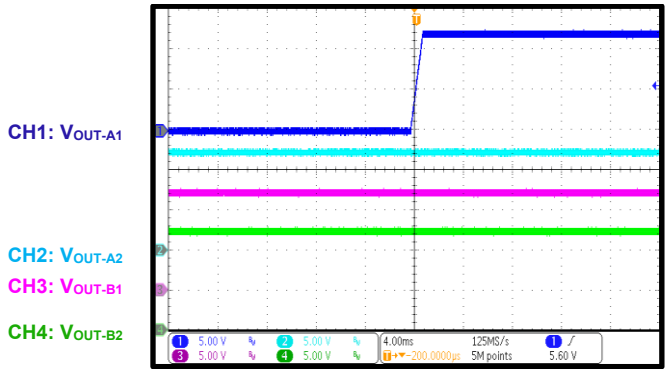
SCP Steady State

All I_{OUT} = 0.8A, OUT_A1 SCP in auto-recovery mode



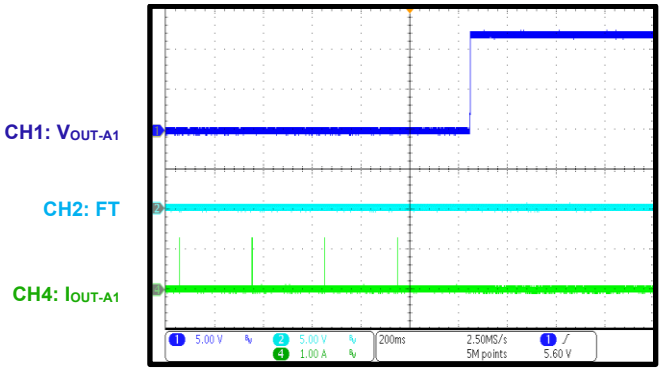
SCP Recovery

All I_{OUT} = 0A, OUT_A1 SCP in auto-recovery mode



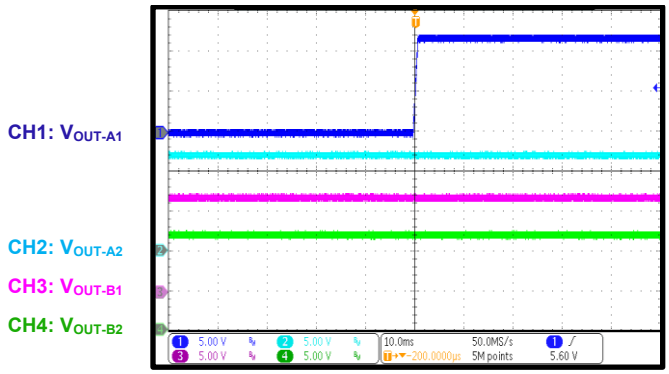
SCP Recovery

All I_{OUT} = 0A, OUT_A1 SCP in auto-recovery mode



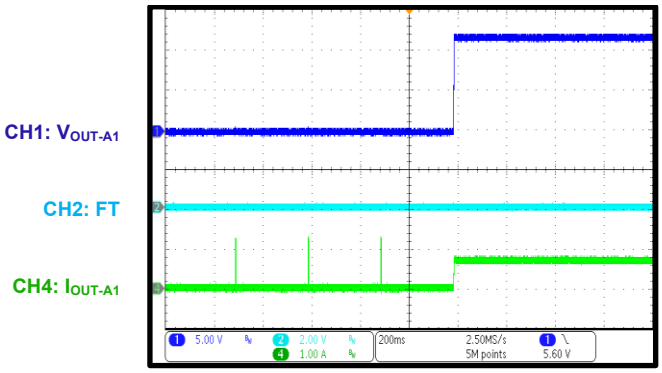
SCP Recovery

All I_{OUT} = 0.8A, OUT_A1 SCP in auto-recovery mode



SCP Recovery

All I_{OUT} = 0.8A, OUT_A1 SCP in auto-recovery mode

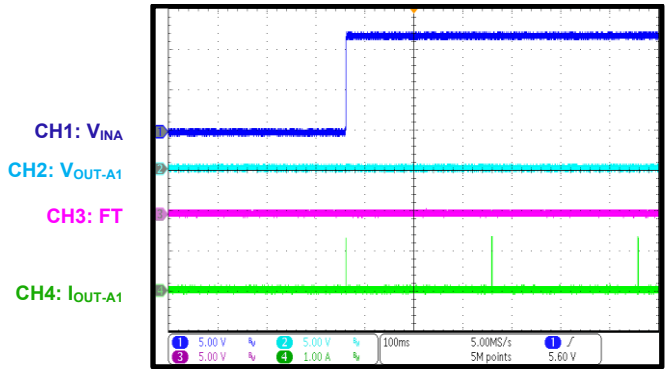


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{INA} = V_{INB} = 12V, V_{DD} = 3.3V, t_{SS} = 1ms, T_A = 25°C, unless otherwise noted.

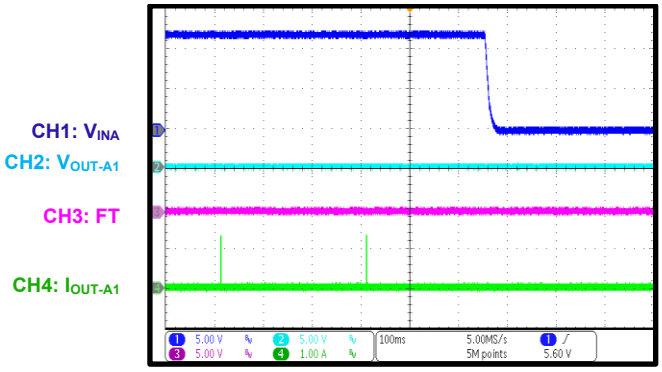
SCP Start-Up

All I_{OUT} = 0.8A, OUT_A1 SCP in auto-recovery mode



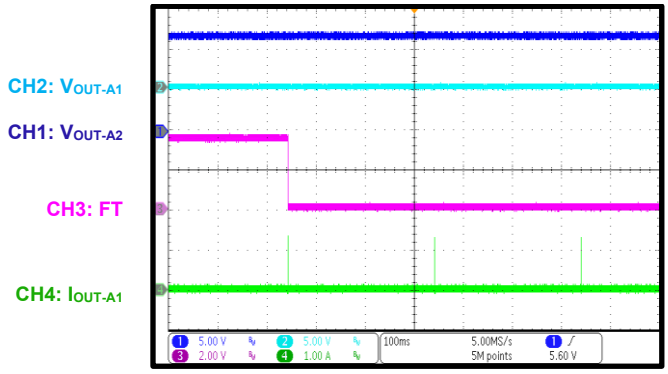
SCP Shutdown

All I_{OUT} = 0.8A, OUT_A1 SCP in auto-recovery mode



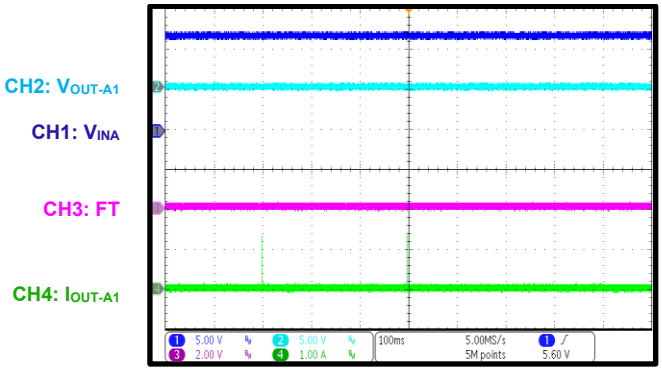
SCP EN Channel On

All I_{OUT} = 0.8A, OUT_A1 SCP in auto-recovery mode



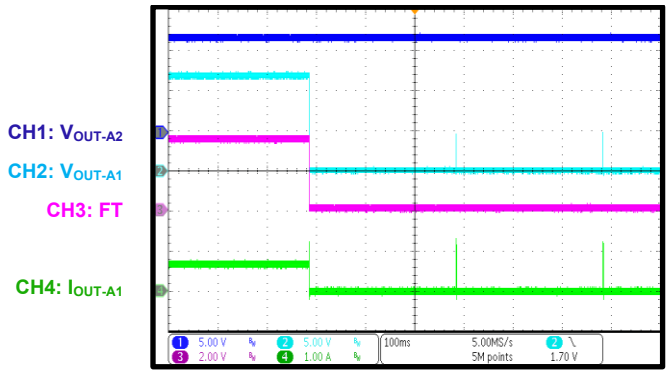
SCP EN Channel Off

All I_{OUT} = 0.8A, OUT_A1 SCP in auto-recovery mode



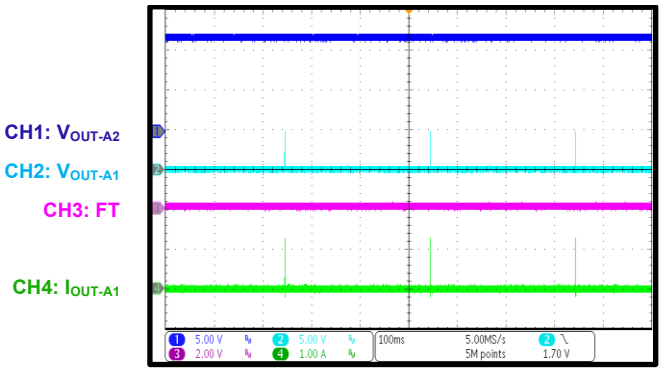
OCP Entry

All I_{OUT} = 0.8A, OUT_A1 OCP in auto-recovery mode



OCP Steady State

All I_{OUT} = 0.8A, OUT_A1 OCP in auto-recovery mode

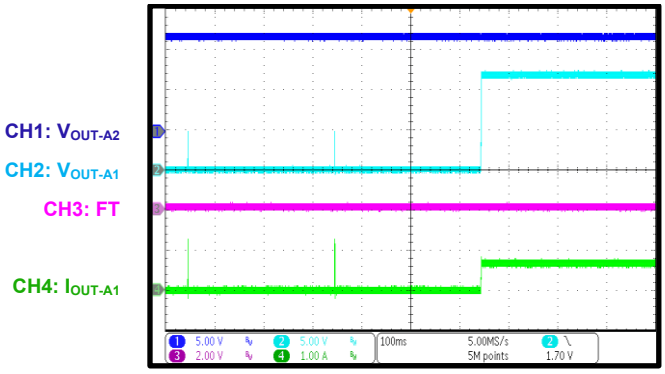


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{INA} = V_{INB} = 12V, V_{DD} = 3.3V, t_{SS} = 1ms, T_A = 25°C, unless otherwise noted.

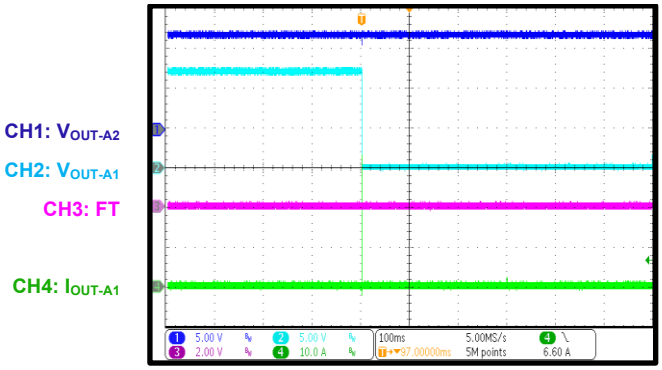
OCP Recovery

All I_{OUT} = 0.8A, OUT_A1 OCP in auto-recovery mode



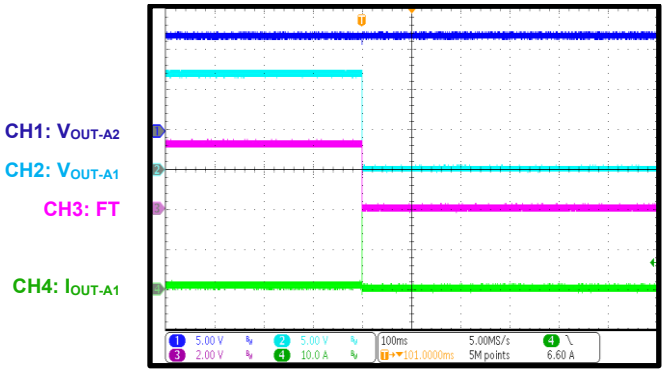
SCP Entry

All I_{OUT} = 0A, OUT_A1 SCP in latch mode



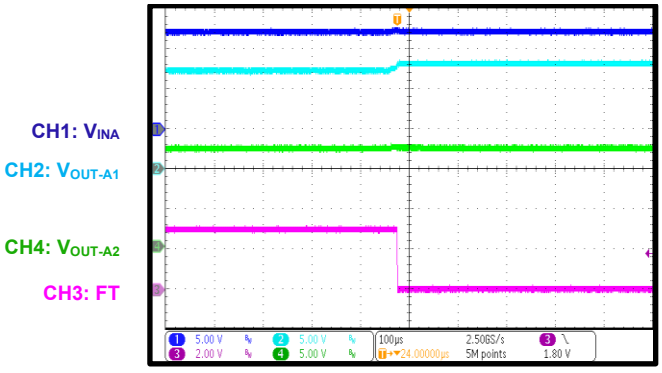
SCP Entry

All I_{OUT} = 0.8A, OUT_A1 SCP in latch mode



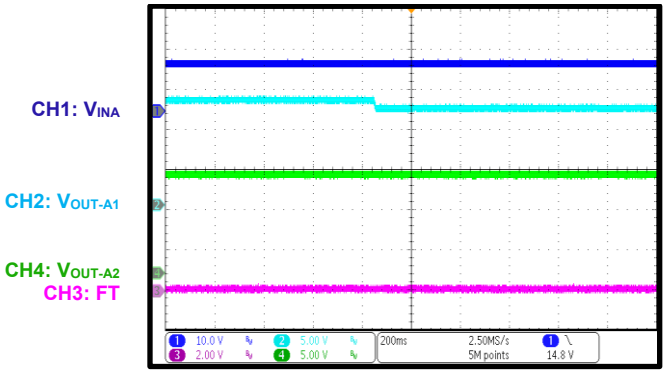
OUT OV Entry

All I_{OUT} = 0A, OUT_A1 OV to 13V



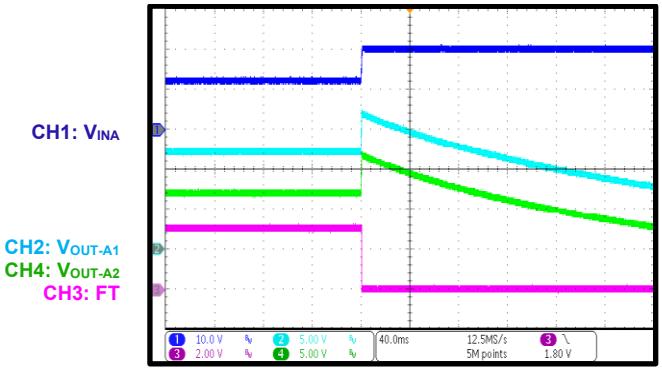
OUT OV Recovery

All I_{OUT} = 0A, OUT_A1 OV to 13V



V_{INA} OVP Entry

All I_{OUT} = 0A, V_{INA} OV to 20V

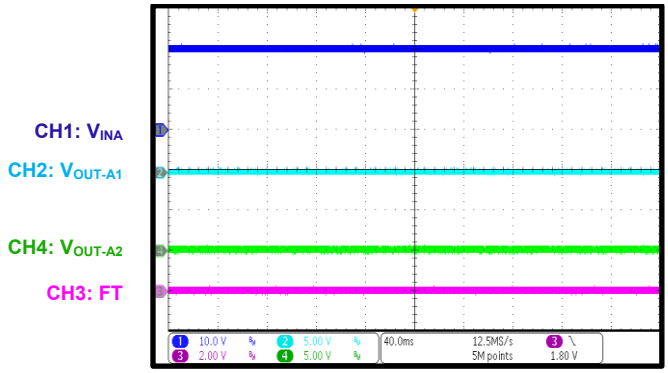


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{INA} = V_{INB} = 12V, V_{DD} = 3.3V, t_{SS} = 1ms, T_A = 25°C, unless otherwise noted.

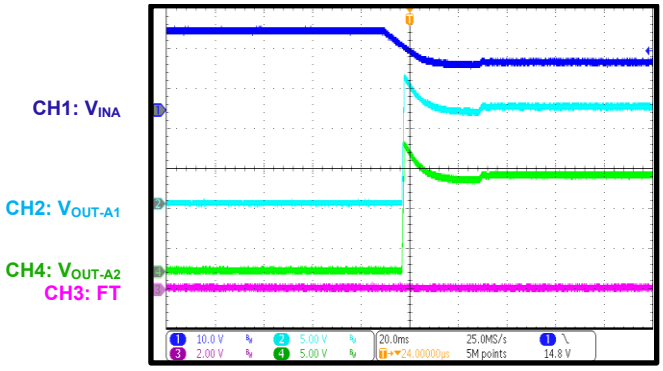
V_{INA} OVP Steady state

All I_{OUT} = 0A, V_{INA} OV to 20V



V_{INA} OVP Recovery

All I_{OUT} = 0A, V_{INA} OV to 20V



FUNCTIONAL BLOCK DIAGRAM

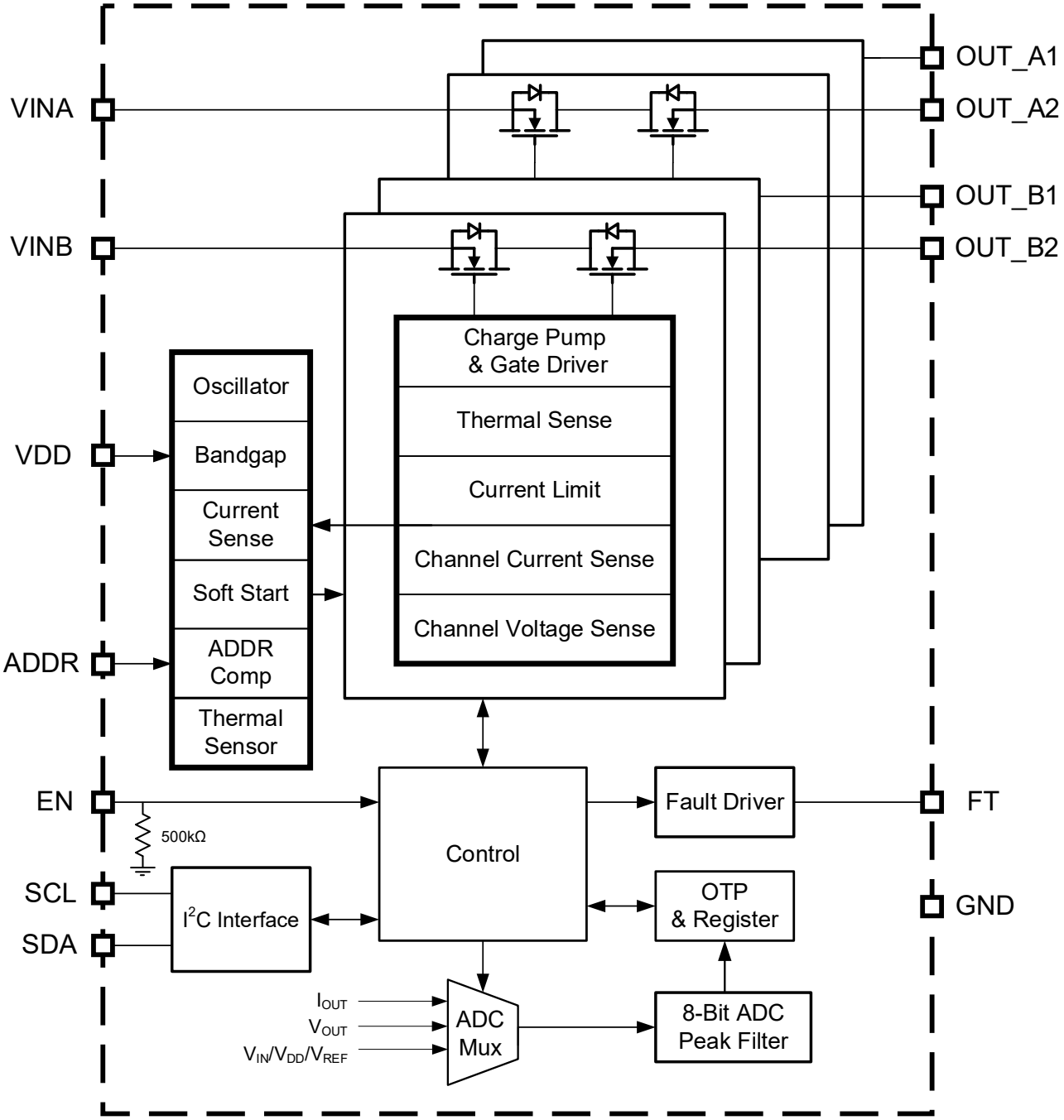


Figure 2: Functional Block Diagram

OPERATION

Separate Power Supplies

With a separate power supply design, the MPQ77240FS supports two different power rails. OUT_A1 and OUT_A2 are supplied power by the VINA pins, while OUT_B1 and OUT_B2 are supplied power by the VINB pins.

When there is only one power rail, it is recommended to connect the VINA pins to the VINB pins.

Parallel Output Connection

The OUT_A1 and OUT_A2 pins can be connected together to achieve up to 1.6A of output current (I_{OUT}). Similarly, OUT_B1 and OUT_B2 can be connected together. In this scenario, set the current limit between the two rails so that they are identical. The current limit during start-up or while recovering from over-current protection (OCP) is half of the total current limit.

When VINA is connected to VINB, all the outputs can be connected together. The current limit of all channels must be set to the same level. During start-up or recovery from over-current (OC) conditions, the current limit is 0.25 x total current limit.

Configurable Current Limit

The device has a configurable current limit. The default channel current limit is 1.2A, but the current limit options for the four channels (A1, A2, B1, and B2) are 1.2A, 0.9A, 0.55A, and 0.25A. A high-accuracy current limit can be configured via the I²C to improve the device's reliability and provide protection from short-circuit or start-up conditions. In addition, this function allows the part to be used in low-current applications.

When the load current reaches the set current limit, I_{OUT} is regulated at the set limit. If this condition lasts for longer than 0.5ms, the channel shuts down to protect the load, and the device reports the fault via the I²C and FT pin. If I_{OUT} increases sharply, the channel shuts down immediately (within 1µs) to protect the device.

Adjustable Start-Up Slew Rate

The start-up time can be set via the I²C to reduce the inrush current during start-up. The options for the start-up time are 0.5ms, 1ms, 4ms, and 8ms. The default time is 1ms.

Internal 8-Bit Analog-to-Digital Converter (ADC)

An integrated, 8-bit analog-to-digital converter (ADC) provides thorough voltage and current information relevant to the device. This information includes the channel currents, input voltages (V_{INx}), reference voltage (V_{REF}), and output voltages.

The ADC's operation mode can be set to continuously sense and update the registers. When the I²C is triggered to save the quiescent current (I_Q), the operation mode can be set to only sense and update the registers once.

The MPQ77240FS can also detect the peak channel current to provide a flexible diagnostic function for applications such as a driver monitoring systems (DMS) (see Figure 3).

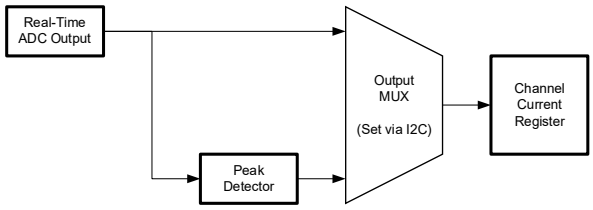


Figure 3: Options for Current Information

Protections and Diagnostic Functions

The MPQ77240FS provides comprehensive and flexible protection and diagnostic functions. The fault status can be reported via both the FT pin and I²C interface. The fault reporting function can be partially masked via the register setting (see Register Map section starting on page 26 for more information).

The various protections and diagnostics are described below.

V_{INx} Over-Voltage Protection (OVP)

The device monitors the input voltages (V_{INx} referring to both V_{INA} and V_{INB}) to protect the load and the device when V_{INx} exceeds V_{INOV_R} (typically 17V). If an over-voltage (OV) condition is detected while in the on state ($V_{INx} > V_{INOV\_R}$), the corresponding output channel (OUT_A1, OUT_A2, OUT_B1, or OUT_B2) shuts down and FT asserts. The corresponding channel turns back on when V_{INx} falls below V_{INOV_RST} (typically 16.5V).

The FT pin's reporting feature can be masked via FT_PIN_MASK_CONTROL (00h), bit[5]. When all the channels are off, V_{INx} OVP can be enabled via FT_PIN_MASK_CONTROL (00h), bit[7].

While in an off state (EN pin is low), the device can still report V_{INx}, and whether there is an OV condition; if there is an OV condition, the corresponding channel(s) cannot turn on.

If the fault status has been removed, write 1 to FT_PIN_MASK_CONTROL (00h), bit[0]. This clears the fault register and de-asserts the FT pin.

V_{INx} Under-Voltage Protection (UVP)

While in the on state, if V_{INx} falls below the under-voltage threshold (V_{INUV_F}), the corresponding output channel(s) turn off, and the status can be detected via the I²C or FT pin. The FT pin's reporting feature can be masked via FT_PIN_MASK_CONTROL (00h), bit[4].

While in the off state, if V_{INx} falls below V_{INUV_F}, the corresponding channel(s) cannot turn on.

If the fault status has been removed, write 1 to FT_PIN_MASK_CONTROL (00h), bit[0]. This clears the fault register and de-asserts the FT pin.

Short-to-GND and Over-Current Protection (OCP)

For short-to-ground protection and OCP, the MPQ77240FS can be configured to auto-retry or latch-off mode for each channel separately via GLOBAL_AND_CHANNEL_CONTROL (01h), bits[7:4]. If auto-retry mode is selected while in the on state, I_{OUT} is regulated to the limited value. If I_{OUT} exceeds the current limit for longer than 0.5ms, the channel shuts down to protect the load, and the device reports the fault via the I²C and FT pin.

If I_{OUT} increases sharply, the channel shuts down immediately (within 1µs). The part automatically tries to recover after 300ms. If the fault status has been removed, write 1 to FT_PIN_MASK_CONTROL (00h), bit[0]. This clears the fault register and de-asserts the FT pin.

If latch-off mode is selected, the part latches off if short-to-GND or current-limit protection occurs. To recover from this state, the device can clear the fault register and the FT pin by cycling the power on VINA or VINB, or by reasserting the EN pin.

Another method to recover from the latch status is to write 0 to disable the corresponding channel via GLOBAL_AND_CHANNEL_CONTROL (01h), bits[3:0], then writing 1 to FT_PIN_MASK_CONTROL (00h), bit[0] to clear the fault register, and lastly, writing 1 to enable the corresponding channel via GLOBAL_AND_CHANNEL_CONTROL (01h), bits[3:0].

If the current limit is set high and a long coaxial cable is used in the application, it is recommended to add an external diode from the GND to OUT pins (OUT_A1, OUT_A2, OUT_B1, and OUT_B2) to prevent the OUT pins from falling below -0.3V when the device is off. A 1N4148 diode is recommended.

Open-Load Detection

While in the on state, the microcontroller (MCU) detects open loads by reading the channel currents reported via the I²C interface.

Short-to-Battery Detection (OUT OVP)

The device monitors the output voltage on each channel (V_{OA1}, V_{OA2}, V_{OB1}, and V_{OB2}). If the output voltage exceeds the corresponding input voltage by about 0.15V (typically), the device turns off the channel and a fault is reported via the FT pin and I²C register. If the output voltage returns to the normal range, the device turns on the channel automatically. The FT report feature can be masked via FT_PIN_MASK_CONTROL (00h), bit[3]. If the fault status has been removed, write 1 to FT_PIN_MASK_CONTROL (00h), bit[0]. This clears the fault register and de-asserts the FT pin.

Thermal Protection

Thermal shutdown is implemented to prevent the chip from thermal runaway. The MPQ77240FS has separate thermal protection for each channel. When the junction temperature (T_J) of one channel rises up to the thermal shutdown threshold (T_{SD}, typically 175°C), the part shuts down and the FT pin pulls down to report the fault. Once T_J falls to its lower threshold (typically 150°C), the device recovers automatically.

If the fault status has been removed, write 1 to FT_PIN_MASK_CONTROL (00h), bit[0]. This

clears the fault register and de-asserts the FT pin.

Other channels are not impacted when a different channel experiences thermal protection. If a channel's temperature exceeds its lower threshold while in the off state, the corresponding channel(s) cannot turn on.

If T_J of one channel exceeds the warning threshold (T_{WR}, typically 140°C), the device reports the thermal warning status via the I²C until T_J falls to its lower threshold (typically 115°C). Meanwhile, the FT pin does not assert, and the other channels are not impacted.

Clock Fault

During operation, the MPQ77240FS monitors its internal clock. If a deviation of 10% is detected, the device enters failsafe mode and the part shuts down. At the same time, the FT pin asserts and FT status is reported in register GLOBAL_STATE_REPORT (05h), bit[1]. Cycle the power on the EN pin to clear the fault.

Reference Voltage Fault

During operation, the MPQ77240FS monitors its internal V_{REF}. If a deviation of 10% is detected, the device enters failsafe mode and the part shuts down. At the same time, the FT pin asserts and FT status is reported in register GLOBAL_STATE_REPORT (05h), bit[2]. Cycle the power on the EN pin to clear the fault.

Analog Built-In Self-Testing (ABIST) Fault

During operation, the MPQ77240FS conducts analog built-in self-testing (ABIST). During ABIST, the following are tested: V_{INx} UVP, V_{INx} OV monitoring, output voltage OV monitoring, and clock monitoring. If an error is detected, the device enters failsafe mode, the FT pin asserts, and the error is reported in register GLOBAL_STATE_REPORT (05h), bit[0]. Cycle the power on the EN pin to clear the fault.

One-Time Programmable (OTP) Memory Cyclic Redundancy Check (CRC) Fault

While loading the configuration from the ome-time programmable (OTP) memory, the end of the OTP page is attached with a cyclic redundancy check (CRC) packet. If an OTP CRC fault is detected, the device enters failsafe mode and the part shuts down. At the same time, the FT pin asserts and FT status is reported in register GLOBAL_STATE_REPORT (05h), bit[0]. Cycle the power on the EN pin to clear the fault.

Start-Up Sequence

Figure 4 shows the start-up sequence.

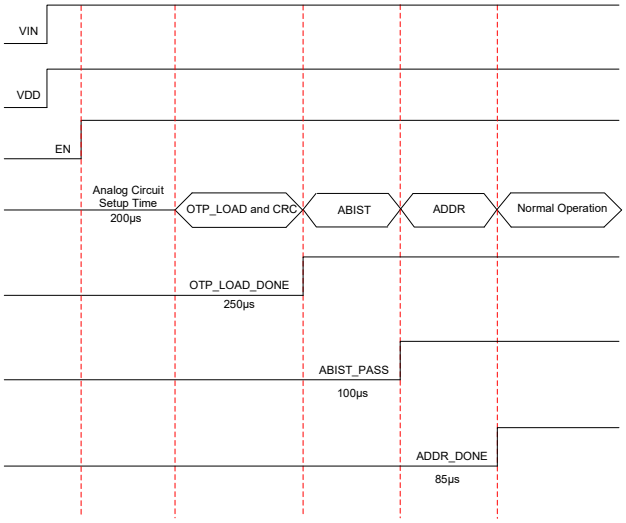


Figure 4: Start-Up Sequence

It is recommended to reserve longer than 700µs to perform the register configuration via the I²C after EN is pulled high, which covers the range of values across different parts.

- VIN, VDD, and EN pull high
- The analog circuit is active
- Check OTP and CRC
- Check ABIST and ADDR
- The MPQ77240FS enters normal operation

To prevent FT from being asserted during start-up, it is required to first apply VIN and VDD. Once both power rails are ready, pull up the EN signal to initiate IC start-up.

AEC Q100-012 Test Grade A Certification

Short-circuit reliability is critical for smart high-side power switch devices. The AEC-Q100-012 standard is used to determine the reliability of the devices when operating under a continuous short-circuit condition. Different grade levels are specified according to the pass cycles. This device is qualified with the highest level (Grade A), which indicates 1 million times short-to-GND certification. The applicable test modes are:

1. Cold repetitive short-circuit test – long pulse
2. Cold repetitive short-circuit test – short pulse
3. Hot repetitive short-circuit test (continuous)

I²C INTERFACE

I²C Serial Interface

The I²C bus is a two-wire, bidirectional serial interface, consisting of a serial data line (SDA) and a serial clock line (SCL). The lines are externally pulled to V_{BUS} when they are idle. When connected to the line, a master device generates the SCL signal and device address, and arranges the communication sequence. The MPQ77240FS works as a slave-only device, which supports up to 1Mbps of bidirectional data transfer in fast-mode, adding flexibility to the power supply solution. V_{OUT}, the transition slew rate, and other converter parameters can be instantaneously controlled via I²C interface.

Data Validity

One clock pulse is generated for each data bit transferred. The data on SDA must be stable during the clock's high period. The SDA line's high or low state can only change when the clock signal on the SCL line is low (see Figure 5).

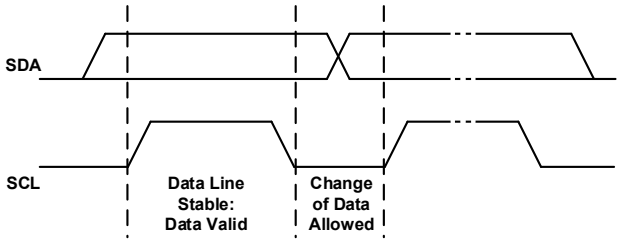


Figure 5: Bit Transfer on the I²C Bus

Start and Stop Commands

Start (S) and stop (P) commands are signaled by the master device, which signifies the beginning and the end of the I²C transfer. A start command is defined as the SDA signal transitioning from high to low while SCL is high. A stop command is defined as the SDA signal transitioning from low to high while SCL is high (see Figure 6).

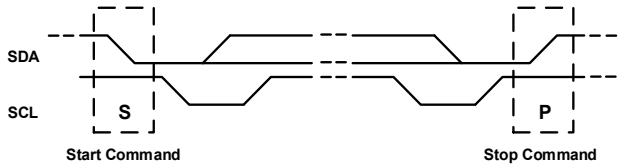


Figure 6: Start and Stop Commands

Data Transfer

Every byte put on SDA must be 8 bits long. Each byte must be followed by an acknowledge (ACK) bit. The acknowledge-related clock pulse is generated by the master. The transmitter releases the SDA line (high) during the acknowledge clock pulse. The receiver must pull down the SDA line during the acknowledge clock pulse, so that it remains stable (low) during the high period of the clock pulse.

Figure 7 shows the data transfer format. After the start command, a slave address is sent. This address is 7 bits long, followed by an 8th data direction bit. The data direction bit determines whether the transmission is a read (R) or write (W). A 0 indicates a write transmission, and a 1 indicates a read (a request for data). A data transfer is always terminated by a stop command, which is generated by the master device. However, if the master device still wishes to communicate on the bus, it can generate a repeated start command and address another slave device without first generating a stop command.

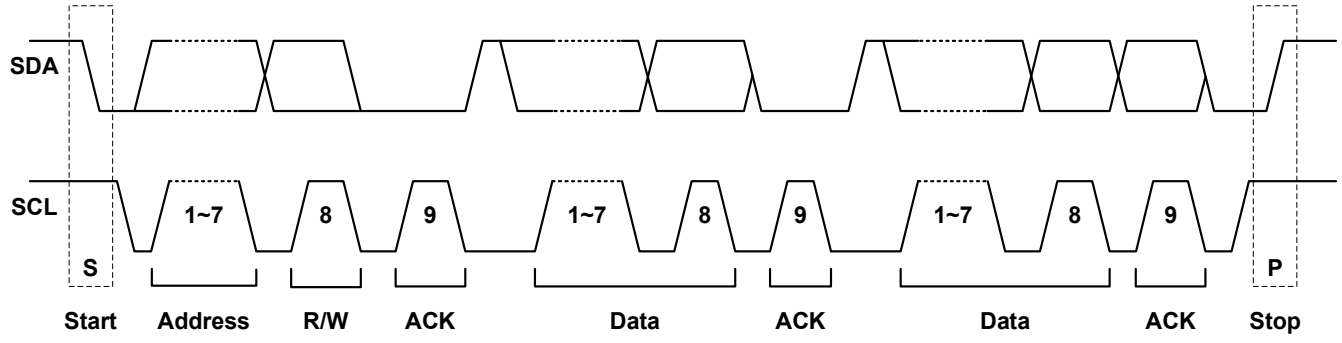


Figure 7: A Complete Data Transfer

Write Sequence

A typical MPQ77240FS write sequence requires a start command from the master device, a valid slave address, a register index byte, and a corresponding data byte (see Figure 8).

After receiving each byte, the MPQ77240FS acknowledges by pulling SDA low during the high period of a single clock pulse.

Read Sequence

The typical MPQ77240FS read sequence requires a start command from the master device, followed by a valid slave address and a register index byte. Unlike with a write sequence, a start command from the master comes again (see Figure 9). The bus direction then turns around with the rebroadcast of the slave address, with bit 1 indicating a read cycle. The following 4th byte contains the data being returned by the MPQ77240FS. The value in this data byte reflects the value of the register index being queried before.

Device Address

The MPQ77240FS's 7-bit address is set via a resistor connected between ADDR and GND. In this scenario, the I²C address is based on the ADDR pin's voltage.

To ensure the resistance is effective within its lifetime, it is required to use a 1% accuracy resistor. The MPQ77240FS checks the I²C address during start-up. Once the I²C address is determined, the address cannot be changed during operation unless the IC's power is reset.

Table 1 shows the recommended resistances, associated effective voltage range, and I²C addresses.

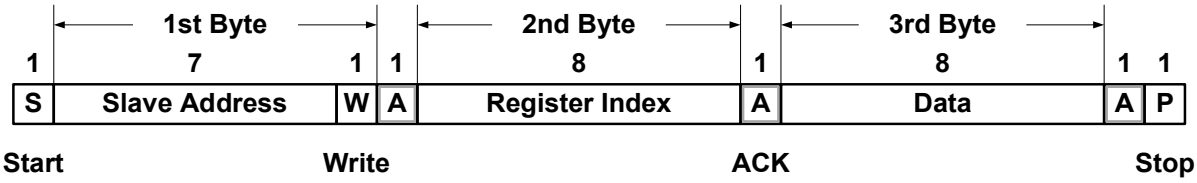


Figure 8: Write Sequence

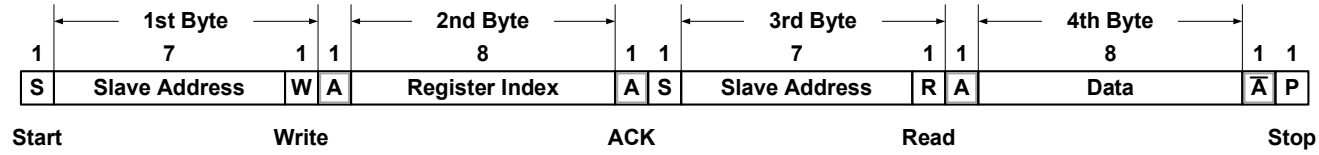


Figure 9: Read Sequence

Table 1: I²C Address Setting

Recommended R_{ADDR}	I²C R/W
Tie to GND	0x70
3.65kΩ	0x73
5.62kΩ	0x74
8.06kΩ	0x75
11.0kΩ	0x76
Float	0x77

REGISTER MAP

The register description and register mapping of MPQ77240FS is shown in Table 2 and Table 3.

Table 2: Register Description

Address	Register Description	Type	Power on Reset
0x00	FT_PIN_MASK_CONTROL	R/W	0x82
0x01	GLOBAL_AND_CHANNEL_CONTROL	R/W	0x00
0x02	CHANNEL_CURRENT_LIMIT_SETUP	R/W	0x00
0x03	CHANNEL_SOFT_ START_SETUP	R/W	0x55
0x04	ADC_CONTROL	R/W	0x00
0x05	GLOBAL_STATE_REPORT	R	0x00
0x06	CHANNEL_STATE_REPROT I	R	0x00
0x07	CHANNEL_STATE_REPROT II	R	0x00
0x08-0x15	ADC1~ADC14	R	0x00

Table 3: Register Mapping

Address	D7	D6	D5	D4	D3	D2	D1	D0
0x00	VINOVEN	REVERSED	VINOVM	VINUVM	OUTOVM	RESERVED	RESERVED	FTCLR
0x01	B2LO	B1LO	A2LO	A1LO	B2EN	B1EN	A2EN	A1EN
0x02	B2CL		B1CL		A2CL		A1CL	
0x03	B2SS		B1SS		A2SS		A1SS	
0x04	ADCCOV	ADCMD	PAPK	PBPK	A1PK	A2PK	B1PK	B2PK
0x05	VINAOV	VINAUV	VINBOV	VINBUV	RESERVED	ADCFT	CLKFT	FSFT
0x06	A1SC	A2SC	B1SC	B2SC	A1OT	A2OT	B1OT	B2OT
0x07	A1OV	A2OV	B1OV	B2OV	A1TW	A2TW	B1TW	B2TW
0x08	ADC1							
0x09	ADC2							
0x0A	ADC3							
0x0B	ADC4							
0x0C	ADC5							
0x0D	ADC6							
0x0E	ADC7							
0x0F	ADC8							
0x10	ADC9							
0x11	ADC10							
0x12	ADC11							
0x13	ADC12							
0x14	ADC13							
0x15	ADC14							

FT_PIN_MASK_CONTROL (00h)

The FT_PIN_MASK_CONTROL command enables $V_{INA/B}$ over-voltage (OV) detection and masks the FT pin's reporting feature.

Bits	Access	Bit Name	Reset	Description
7	R/W	VINOVEN	1	This bit can only be set when all channels are off. 0: V_{INA} or V_{INB} OV detection is disabled 1: V_{INA} or V_{INB} OV detection is enabled; the part shuts down if $V_{INA/B}$ exceeds the threshold
6	R/W	RESERVED	0	Reserved.
5	R/W	VINOVM	0	0: The FT pin reports a V_{INA} or V_{INB} OV condition 1: The FT pin does not report a V_{INA} or V_{INB} OV condition
4	R/W	VINUVM	0	0: The FT pin reports a V_{INA} or V_{INB} under-voltage (UV) condition 1: The FT pin does not report a V_{INA} or V_{INB} UV condition
3	R/W	OUTOVM	0	0: The FT pin reports an OUT OV condition 1: The FT pin does not report an OUT OV condition
2	R/W	RESERVED	0	Reserved.
1	R/W	RESERVED	1	Reserved.
0	R/W	FTCLR	0	0: Normal operation 1: Write to clear the fault in the registers

GLOBAL_AND_CHANNEL_CONTROL (01h)

The GLOBAL_AND_CHANNEL_CONTROL command controls the mode when a short-to-GND or over-current protection (OCP) fault occurs. It also enables the channels.

Bits	Access	Bit Name	Reset	Description
7	R/W	B2LO	0000	Sets whether each channel (A1, A2, B1, or B2) goes into auto-recovery mode or latch-off mode if a short-to-ground or OCP fault occurs. 0: Auto-recovery mode 1: Latch-off mode. For the device to recover, clear the fault register, then cycle the power on VINx or reassert the EN pin
6		B1LO		
5		A2LO		
4		A1LO		
3	R/W	B2EN	0000	Enables each individual channel (A1, A2, B1, or B2). Both the device EN and the channel's EN signal must be high to enable the channel. 0: Disabled 1: Enabled
2		B1EN		
1		A2EN		
0		A1EN		

CHANNEL_CURRENT_LIMIT_SETUP (02h)

The CHANNEL_CURRENT_LIMIT_SETUP command sets the current-limit value for each channel (A1, A2, B1, and B2).

Bits	Access	Bit Name	Reset	Description
7:6	R/W	B2CL	00	00: Current limit: 1.2A 01: Current limit: 0.9A 10: Current limit: 0.55A 11: Current limit: 0.25A
5:4	R/W	B1CL	00	
3:2	R/W	A2CL	00	
1:0	R/W	A1CL	00	

CHANNEL_SOFT_START_SETUP (03h)

The CHANNEL_SOFT_START_SETUP command sets the soft-start time (t_{SS}) for each channel (A1, A2, B1, and B2).

Bits	Access	Bit Name	Reset	Description
7:6	R/W	B2SS	01	00: t_{SS} = 0.5ms 01: t_{SS} = 1ms 10: t_{SS} = 4ms 11: t_{SS} = 8ms
5:4	R/W	B1SS	01	
3:2	R/W	A2SS	01	
1:0	R/W	A1SS	01	

ADC_CONTROL (04h)

The ADC_CONTROL command controls the operation mode of the analog-to-digital converter (ADC); it can be set to continuously sense and update the registers, or to sense and update only once when the I^2C is triggered. This command can also control whether to detect the peak current in the past 1s or the real-time current for each channel (A1, A2, B1, and B2).

Bits	Access	Bit Name	Reset	Description
7	R/W	ADCCOV	0	If ADCMD is set to 1, the user can set this pin to let the ADC convert for one cycle. Once the conversion is finished, this bit is set to 0 automatically and the data in the I^2C registers (ADC1~ADC14) are valid for reading. 0: ADC conversion is complete; ready for I^2C reading 1: Start ADC conversion
6	R/W	ADCMD	0	0: Continuously update ADC1~ADC14 if VDD and EN are ready 1: The ADC starts conversion only when the I^2C sets ADCCOV to 1
5	R/W	PAPK	0	Selects whether the ADC reads the currents in parallel. 0: The ADC reads the channel's real-time current (OUT_A1 + OUT_A2 or OUT_B1 + OUT_B2) 1: The ADC reads the channel's peak channel (OUT_A1 + OUT_A2 or OUT_B1 + OUT_B2) in the past 1s (the data is valid only when ADCCOV is set to 0)
4	R/W	PBPK	0	
3	R/W	A1PK	0000	Selects how to read each channel's current. 0: The ADC reads the channel's real-time current 1: The ADC reads the channel's peak current in the past 1s (the data is valid only when ADCCOV is set to 0)
2		A2PK		
1		B1PK		
0		B2PK		

GLOBAL_STATE_REPORT (05h)

The GLOBAL_STATE_REPORT command reports the global state for over-voltage (OV) and under-voltage (UV) conditions; if the FT pin asserts, the relevant bit is read as 1.

Bits	Access	Bit Name	Reset	Description
7	R	VINAOV	0	0: No V_{INA} OV condition has been detected 1: A V_{INA} OV condition has been detected
6	R	VINAUV	0	0: No V_{INA} UV condition has been detected 1: A V_{INA} UV condition has been detected
5	R	VINBOV	0	0: No V_{INB} OV condition has been detected 1: A V_{INB} OV condition has been detected
4	R	VINBUV	0	0: No V_{INB} UV condition has been detected 1: A V_{INB} UV condition has been detected
3	R	RESERVED	0	Reserved.

2	**R**	**ADCFT**	**0**	**0: No ADC reference voltage error has been detected** **1: An ADC reference voltage error has been detected**
1	R	CLKFT	0	0: No internal CLK error has been detected 1: An internal CLK error has been detected
0	R	FSFT	0	0: No ABIST or OTP CRC error has been detected 1: An ABIST or OTP CRC error has been detected

CHANNEL_STATE_REPROT_I (06h)

The CHANNEL_STATE_REPROT_I command reports the short-to-GND, OCP, and over-temperature (OT) status for each channel (A1, A2, B1, and B2).

Bits	Access	Bit Name	Reset	Description
7	R	A1SC	0000	Reports whether the channel output is experiencing a short-to-GND or OCP fault. 0: No output short-to-GND or OCP fault has been detected 1: An output short-to-GND or OCP fault has been detected
6		A2SC		
5		B1SC		
4		B2SC		
3	R	A1OT	0000	0: No OT condition has been detected on the channel 1: An OT condition has been detected on the channel
2		A2OT		
1		B1OT		
0		B2OT		

CHANNEL_STATE_REPROT_II (07h)

The CHANNEL_STATE_REPROT_II command reports whether an output over-voltage (OV) condition or thermal warning has occurred for each channel (A1, A2, B1, and B2).

Bits	Access	Bit Name	Reset	Description
7	R	A1OV	0000	Indicates whether an output OV condition has been detected on the channel. 0: No output OV condition has been detected on the channel 1: An output OV condition has been detected on the channel
6		A2OV		
5		B1OV		
4		B2OV		
3	R	A1TW	0000	Indicates whether a thermal warning has been detected on the channel. 0: No thermal warning has been detected 1: Thermal warning has been detected on the channel.
2		A2TW		
1		B1TW		
0		B2TW		

ADC1~ADC14 (08h~15h)

The ADC1~ADC14 reads the following for all four channels (A1, A2, B1, and B2): V_{INx}, V_{REF}, and output voltages.

Bits	Access	Bit Name	Reset	Description
7:0	R	ADC1~ADC14	0000 0000	V_{INA}, V_{INB}, and OUT voltages (OUT_A1, OUT_A2, OUT_B1, and OUT_B2): 75mV/LSB. VDD: 20.8mV/LSB. V_{REF}: 5mV/LSB. OUT currents (OUT_A1, OUT_A2, OUT_B1, and OUT_B2): 5mA/LSB. Parallel OUT currents (OUT_A1 + OUT_A2, and OUT_B1 + OUT_B2): 10mA/LSB. ADC1~ADC4: Returns the value for V_{INA}, V_{INB}, V_{DD}, and V_{REF}, respectively ADC5~ADC8: Returns the OUT_A1, OUT_A2, OUT_B1, and OUT_B2 voltage, respectively ADC9~ADC12: Returns the OUT_A1, OUT_A2, OUT_B1, and OUT_B2 current (real-time or peak), respectively ADC13: Returns the OUT_A1 + OUT_A2 current (real-time or peak) ADC14: Returns the OUT_B1 + OUT_B2 current (real-time or peak)

APPLICATION INFORMATION

Functional Safety Compliant

As a functional safety compliant device, the MPQ77240FS can achieve ASIL-B levels without additional diagnostics. The device can achieve ASIL-D compliance by reading input/output voltages and channel currents via the ADC. The MPQ77240FS also provides related safety documentation to aid functional safety design. A multiple-pin design is applied for several pins (VINA, VINB, and GND); this means that a single-point failure does not impact the device's operation, which improves the device's reliability.

Power-over-Coaxial Cable

One of the key applications for the MPQ77240FS is intended to be protecting power lines that supply remote cameras across a coaxial cable with concurrent data transmission. Figure 10 shows a system architecture diagram example.

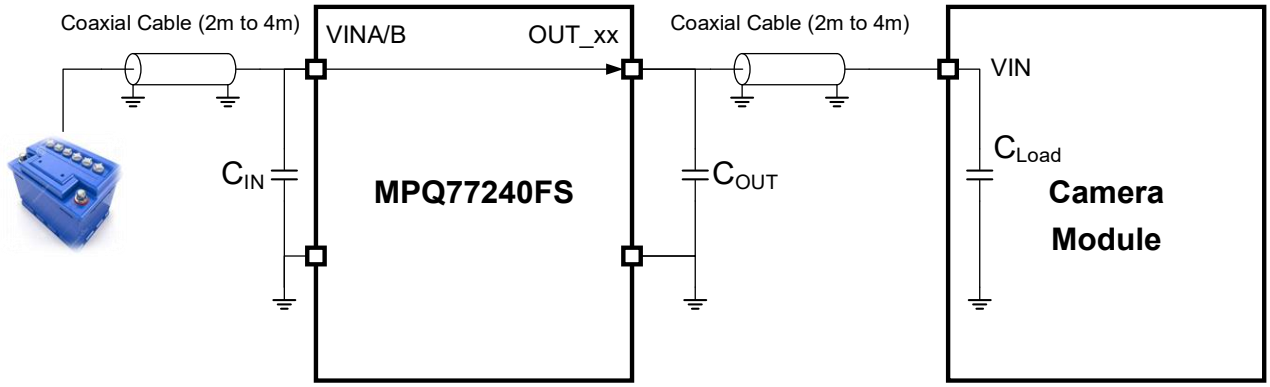


Figure 10: System Architecture Diagram Example

Figure 11 shows a typical application circuit for the MPQ77240FS.

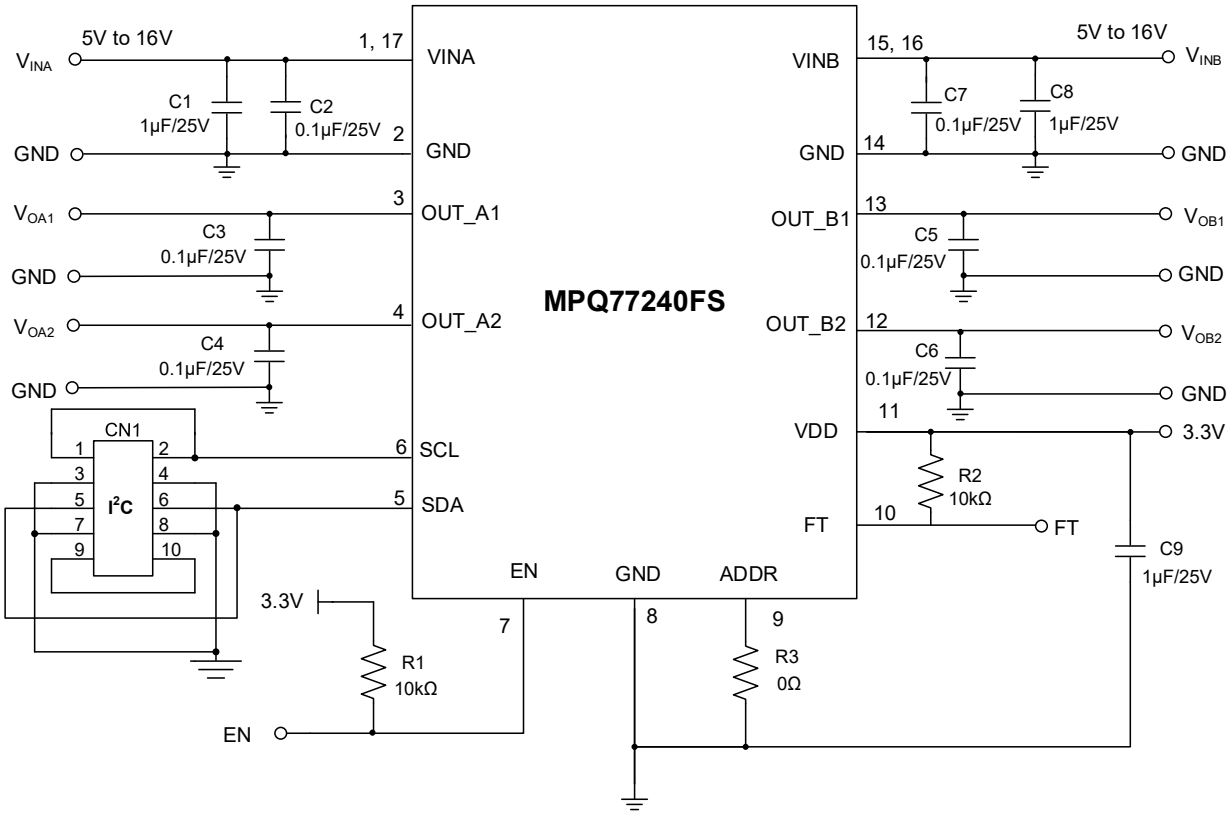


Figure 11: MPQ77240FS Typical Application Circuit

Table 4 shows the design guide index.

Table 4: Design Guide Index

Pin #	Pin Name	Component	Design Guide Index
1, 17	VINA	C1, C2	Selecting the Input Capacitor (VINA, Pins 1 and 17; VINB, Pins 15 and 16)
15, 16	VINB	C7, C8	Selecting the Input Capacitor (VINA, Pins 1 and 17; VINB, Pins 15 and 16)
3	OUT_A1	C3	Selecting the Output Capacitor (OUT_A1, Pin 3; OUT_A2, Pin 4; OUT_B1, Pin 13; OUT_B2, Pin 12)
4	OUT_A2	C4	Selecting the Output Capacitor (OUT_A1, Pin 3; OUT_A2, Pin 4; OUT_B1, Pin 13; OUT_B2, Pin 12)
12	OUT_B2	C6	Selecting the Output Capacitor (OUT_A1, Pin 3; OUT_A2, Pin 4; OUT_B1, Pin 13; OUT_B2, Pin 12)
13	OUT_B1	C5	Selecting the Output Capacitor (OUT_A1, Pin 3; OUT_A2, Pin 4; OUT_B1, Pin 13; OUT_B2, Pin 12)
2, 8, 14	GND	-	Ground Connection (GND, Pins 2, 8, and 14)
5	SDA	-	Digital Interface (SDA, Pin 5; SCL, Pin 6)
6	SCL	-	Digital Interface (SDA, Pin 5; SCL, Pin 6)
7	EN	R1	Enable (EN, Pin 7)
9	ADDR	R3	Setting the I²C Address (ADDR, Pin 9)
10	FT	R2	Fault Indicator (FT, Pin 10)
11	VDD	C9	Analog Supply Bypass (VDD, Pin 11)

Selecting the Input Capacitor (VINA, Pins 1 and 17; VINB, Pins 15 and 16)

For the best performance, it is recommended to use 1µF (or greater) ceramic capacitors with X5R or X7R dielectrics due to their low ESR and small temperature coefficients.

It is recommended to use another lower-value capacitor (e.g. 0.1µF) with a small package size (e.g. 0603) to absorb high-frequency switching noise. Place the lower-value capacitor as close to VINA, VINB, and GND as possible.

Selecting the Output Capacitor (OUT_A1, Pin 3; OUT_A2, Pin 4; OUT_B1, Pin 13; OUT_B2, Pin 12)

For the best performance, it is recommended to use a 0.1µF capacitor with a small package size (e.g. 0603) to absorb high-frequency switching noise. Place the capacitor as close to OUT_A1, OUT_A2, OUT_B1, OUT_B2, and GND as possible.

Ground Connection (GND, Pins 2, 8 and 14)

See the PCB Layout Guidelines section on page 31 for more details.

Digital Interface (SDA, Pin 5; SCL, Pin 6)

The MPQ77240FS works as a slave-only device that supports standard mode (100kbps), fast mode (400kbps), and fast-plus mode (1Mbps) bidirectional data transfers, adding flexibility to the power supply solution. The SCL and SDA lines are externally pulled to a bus voltage via a resistor (e.g. 1kΩ).

Enable (EN, Pin 7)

EN is a digital control pin that turns the device on and off. When the EN pin voltage exceeds 1.2V, the MPQ77240FS turns on. To turn on the device, connect EN to a power supply via a pull-up resistor (R1, which is recommended to be about 10kΩ).

Setting the I²C Address (ADDR, Pin 9)

See Table 1 on page 25 for more details to set R3.

Fault Indicator (FT, Pin 10)

The FT pin is an open-drain output. If using the FT pin, connect it to a power supply via a pull-up resistor (R2, which is recommended to be about 10kΩ). FT asserts low if a fault occurs.

Analog Supply Bypass (VDD, Pin 11)

Connect the VDD pin to a 3.3V power rail to supply the internal ADC and logic circuit. Connect this pin to GND with a 1µF bypass capacitor (C9).

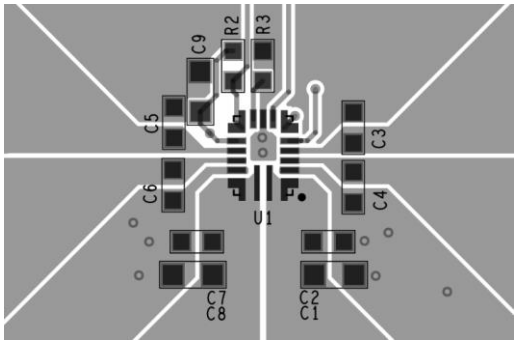
PCB Layout Guidelines (10)

Efficient PCB layout, especially input capacitor placement, is critical for stable operation. A 4-layer layout is strongly recommended to improve thermal performance. For the best results, refer to Figure 12 and follow the guidelines below:

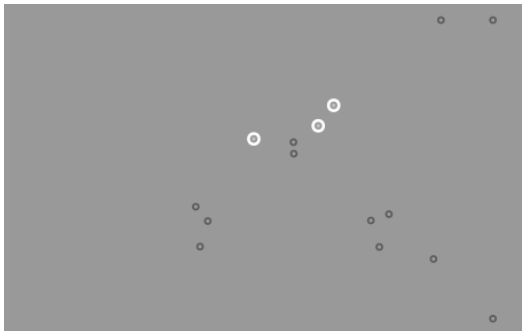
1. Connect a large ground plane directly to the GND pin.
2. Place the ceramic input capacitor, especially the small package size (0603) input and output bypass capacitors, as close to VINA, VINB, OUT_A1, OUT_A2, OUT_B1, OUT_B2, and GND as possible to minimize noise.
3. Place the VDD capacitor as close to the VDD and GND pins as possible.
4. Use multiple vias to connect the power planes to the internal layers.

Note:

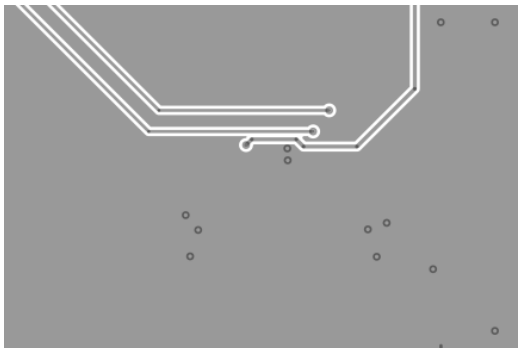
10) The recommended PCB layout is based on Figure 13 on page 34.



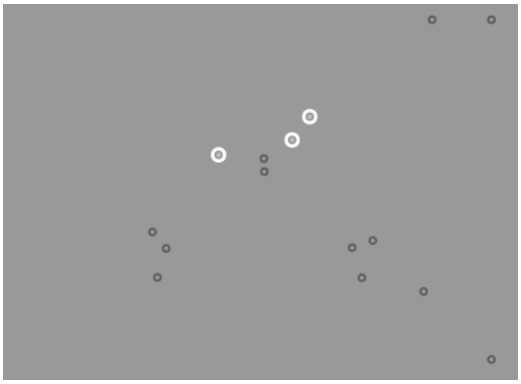
Top Layer



Mid-Layer 1



Mid-Layer 2



Bottom Layer

Figure 12: Recommended PCB Layout

TYPICAL APPLICATION CIRCUIT

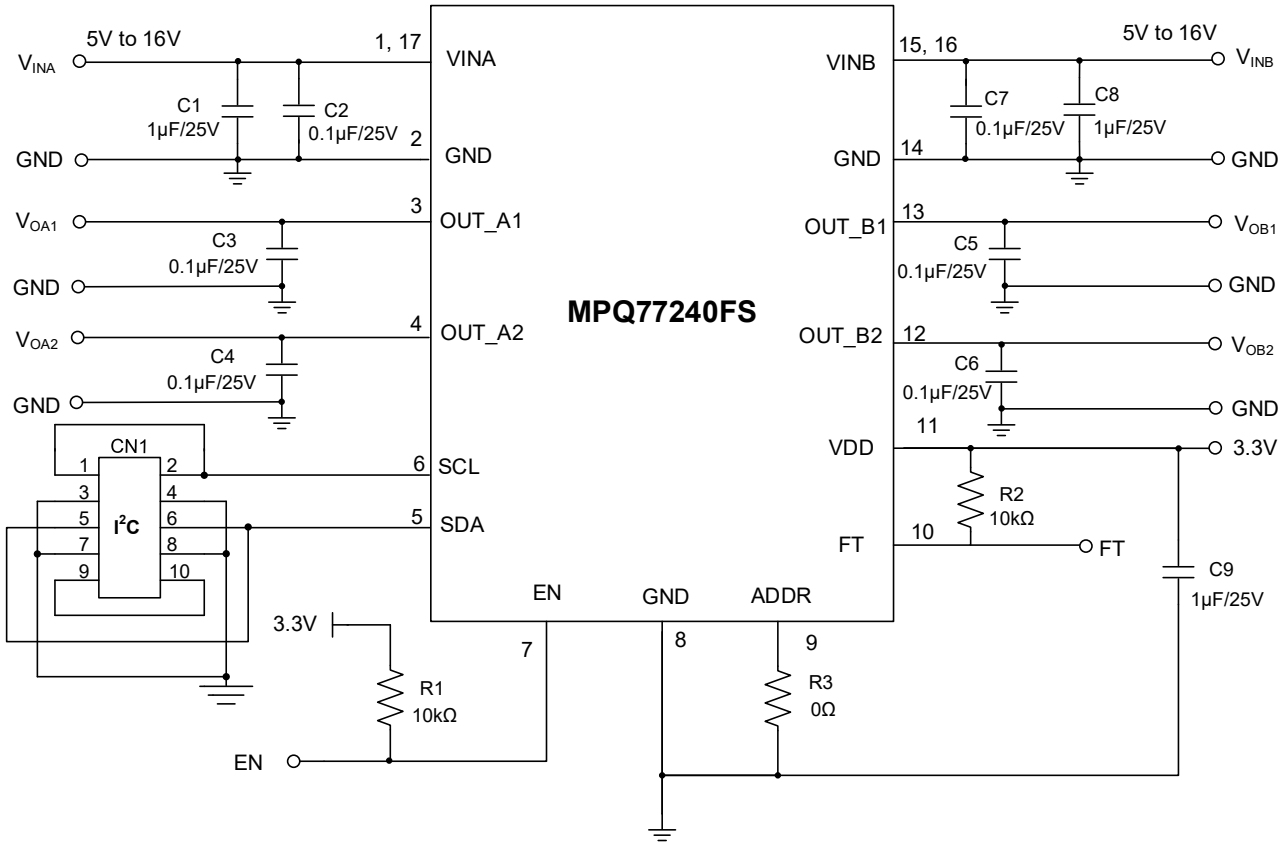
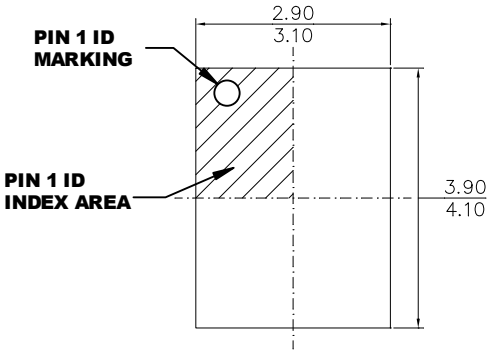


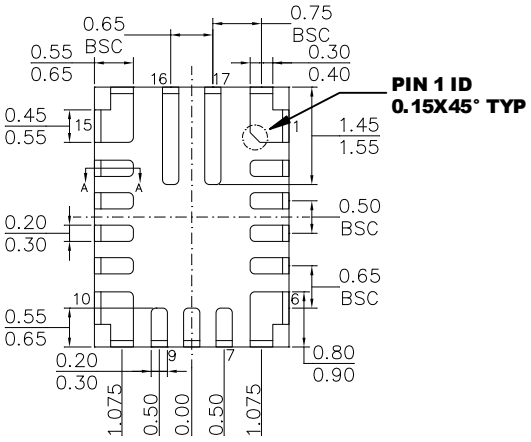
Figure 13: Application Circuit

PACKAGE INFORMATION

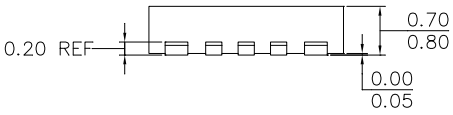
TQFN-17 (3mmx4mm)
Wettable Flank



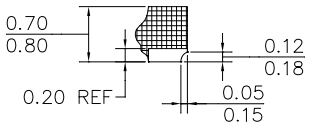
TOP VIEW



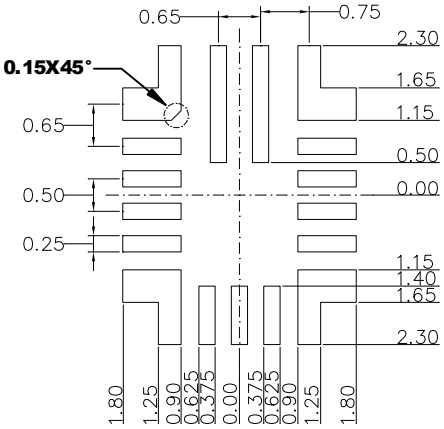
BOTTOM VIEW



SIDE VIEW



SECTION A-A

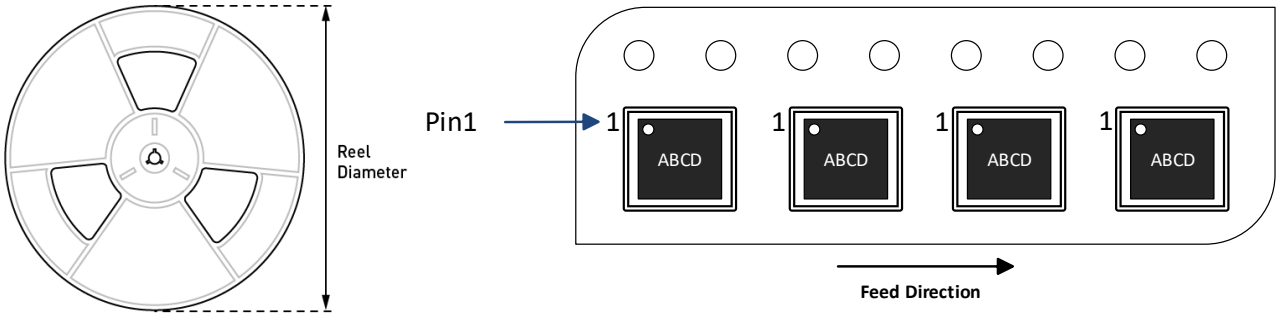


RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ77240FSGLTE-xxxxAEC1-Z	TQFN-17 (3mmx4mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	7/24/2024	Initial Release	-
1.1	9/25/2025	Updated from ASIL-B to ASIL-B/D compliant in the header	All pages
		Updated the following in the Description section: • Added description about the MPQ77240FS being ASIL-B and ASIL-D compliant and made formatting edits Updated the following in the Features section: • Updated “Integrated 8-Bit ADC to Report Channel Voltage and Current” to “Integrated 8-Bit ADC to Enhance Diagnostic Coverage” • Removed “Built-In Self-Testing (BIST)” • Updated “ASIL-B Compliant” to “ASIL-B/D Compliant”	1
		Updated the Table 1 page reference from page 24 to page 25 in the Pin Functions and Setting the I^2C Address (ADDR, Pin 9) sections.	5, 32
		Updated the following in the Pin Functions section: • Removed “3.3V or 5V” from the FT pin’s external power source description • Removed 5V from the VDD pin’s power rail description	5
		Updated the following in the Electrical Characteristics section: • Input logic high: Changed the max value (1.3V) to be the min value • Input logic low: Removed the min value (0.4V), and added the max value (0.5V)	8
		Added description to the Parallel Output Connection section regarding the current limit of all channels when VINA is connected to VINB, and all the outputs can be connected together; updated the page reference to the Register Map section from page 25 to page 26 in the Protections and Diagnostic Functions section.	21
		Corrected the part number from MPQ5864 to MPQ77240FS in the Internal 8-Bit Analog-to-Digital Converter (ADC) and Enable (EN, Pin 7) sections.	21, 32
		Made a minor copyedit and added description regarding another method to recover from the latch status in the Short-to-GND and Over-Current Protection (OCP) section.	22
		Added the Start-Up Sequence section (including Figure 4).	23
		Updated bits[2:0] of the 0x05 address (previously reserved) in Table 3 of the Register Map section.	26
		Updated bits[2:0] (previously reserved) and the bit[3] reset value in the GLOBAL_STATE_REPORT (05h) section; updated the bits[3:0] description in the CHANNEL_STATE_REPROT_I (06h) section.	29
		Updated the functional safety compliant device description to specify ASIL-B/D compliance and made minor copyedits in the Functional Safety Compliant section.	31

REVISION HISTORY *(continued)*

Revision #	Revision Date	Description	Pages Updated
1.2	01/23/2026	• Updated Figure 4 by adding the VIN sequence. • Updated to “VIN, VDD, and EN pull high” from “VDD and EN pull high” in the Start-Up Sequence section. • Added “To prevent FT from being asserted during start-up, it is required to first apply VIN and VDD. Once both power rails are ready, pull up the EN signal to initiate IC start-up.” in the Start-Up Sequence section. • Minor formatting updates.	23