MPQ6539-AEC1

80V, Three-Phase, BLDC Motor Pre-Driver with HS and LS Inputs, AEC-Q100 Qualified

DESCRIPTION

The MPQ6539-AEC1 is a gate driver IC that is designed for three-phase, brushless DC (BLDC) motor driver applications. The MPQ6539-AEC1 can drive three half-bridges consisting of six N-channel power MOSFETs up to 80V.

The MPQ6539-AEC1 uses a bootstrap (BST) capacitor (C_{BST}) to generate a supply voltage for the high-side MOSFET (HS-FET) driver. If the output is held high for an extended period, an internal charge pump maintains the high-side (HS) gate driver.

Full protection features include configurable over-current protection (OCP), adjustable dead-time (DT) control, under-voltage lockout (UVLO), and thermal shutdown.

The MPQ6539-AEC1 is available in a QFN-28 (4mmx5mm) package with an exposed thermal pad and wettable flanks, and is available in AEC-Q100 Grade 1.

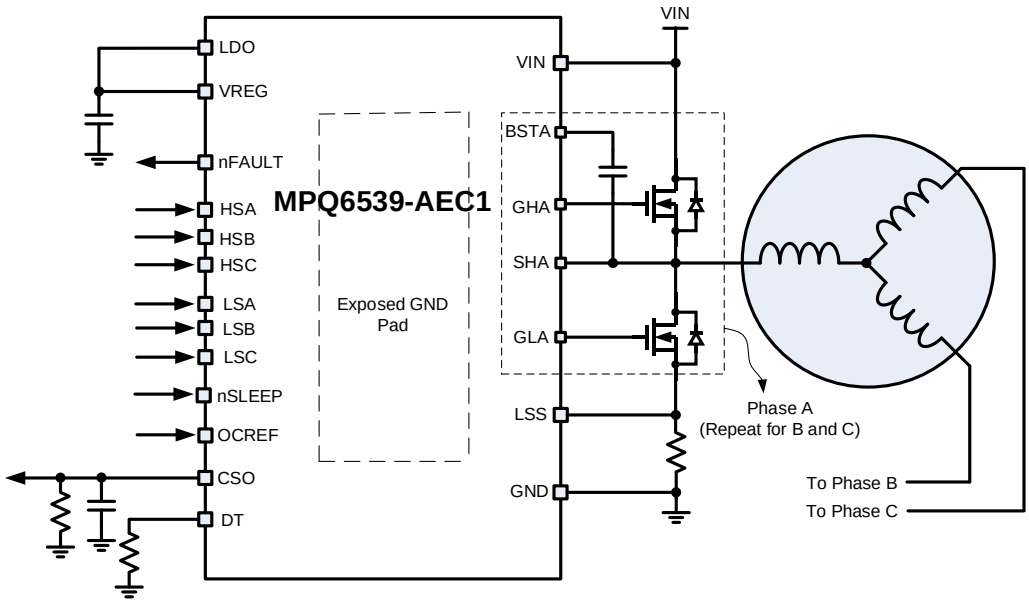
FEATURES

- Supports 80V Operation
- 100V Maximum Bootstrap (BST) Voltage (V_{BST})
- Internal Low-Dropout (LDO) Supports External NPN for High-Current Driver Requirements
- Integrated Current-Sense (CS) Amplifier
- Low-Power Sleep Mode for Battery-Powered Applications
- Configurable Over-Current Protection (OCP) for External MOSFETs
- Adjustable Dead-Time (DT) Control to Prevent Shoot-Through
- Thermal Shutdown and Under-Voltage Lockout (UVLO) Protection
- Fault Indication Output
- Available in a Thermally Enhanced, Surface-Mount QFN-28 (4mmx5mm) Package with Exposed Pad and Wettable Flanks
- Available in AEC-Q100 Grade 1

APPLICATIONS

- Three-Phase Brushless DC (BLDC) Motors and Permanent Magnet Synchronous Motors (PMSMs)
- Power Drills
- E-Bikes

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number	Package	Top Marking	MSL Rating
MPQ6539GVE-AEC1*	QFN-28 (4mmx5mm)	*See Below*	2

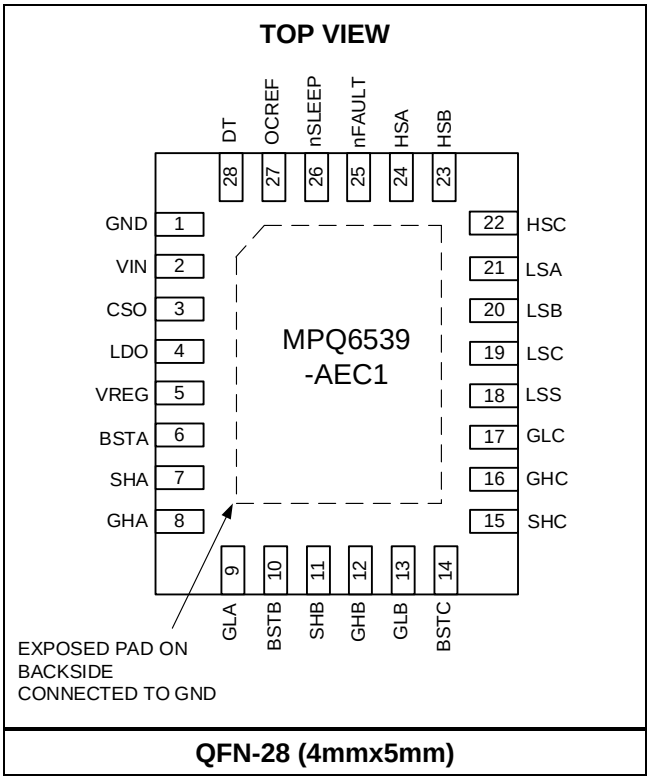
* For Tape & Reel, add suffix -Z (e.g. MPQ6539GVE-AEC1-Z).

TOP MARKING

MPSYWW
MP6539
LLLLLL
E

MPS: MPS prefix
Y: Year code
WW: Week code
MP6539: Part number
LLLLLL: Lot number
E: Wettable lead flank

PACKAGE REFERENCE



QFN-28 (4mmx5mm)

PIN FUNCTIONS

Pin #	Name	Description
1	GND	**Ground.**
2	VIN	**Input supply voltage.**
3	CSO	**Current-sense (CS) output and over-current protection (OCP) off-time adjustment.**
4	LDO	**Gate driver low-dropout (LDO) output and base driver for external NPN transistor.**
5	VREG	**Gate driver supply voltage.**
6	BSTA	**Phase A bootstrap (BST) output.**
7	SHA	**Phase A high-side (HS) source connection.**
8	GHA	**Phase A HS gate driver.**
9	GLA	**Phase A Low-side (LS) gate driver.**
10	BSTB	**Phase B BST output.**
11	SHB	**Phase B HS source connection.**
12	GHB	**Phase B HS gate driver.**
13	GLB	**Phase B LS gate driver.**
14	BSTC	**Phase C BST output.**
15	SHC	**Phase C HS source connection.**
16	GHC	**Phase C HS gate driver.**
17	GLC	**Phase C LS gate driver.**
18	LSS	**LS source connection.**
19	LSC	**Phase C LS input pin.**
20	LSB	**Phase B LS input pin.**
21	LSA	**Phase A LS input pin.**
22	HSC	**Phase C HS input pin.**
23	HSB	**Phase B HS input pin.**
24	HSA	**Phase A HS input pin.**
25	nFAULT	**Fault indication.** The nFAULT pin is an open-drain output, and is pulled low if a fault condition is detected.
26	nSLEEP	**Sleep mode input.** Pull the nSLEEP pin low to enter low-power sleep mode; pull nSLEEP high to enable the part. nSLEEP is pulled down via an internal resistor.
27	OCREF	**OCP reference input.**
28	DT	**Dead time (DT) setting.**

ABSOLUTE MAXIMUM RATINGS (1)

Input voltage (V_{IN}) .....-0.3V to +90V
Input voltage (V_{REG}), GLA/B/C ...-0.3V to +14.3V
LDO .....-0.3V to +14.3V
BSTA/B/C .....-0.3V to +100V
GHA/B/C .....-0.3V to (BST-SH) + 0.3V
GHA/B/C (transient, 2µs) .....
.....-8V to (BST-SH) + 0.3V
LSS .....-0.3V to +4V
LSS (transient, 2µs).....-1V to +4V
SHA/B/C .....-5V to +90V
SHA/B/C (transient, 2µs) .....-8V to +90V
All other pins to GND .....-0.3V to +6.5V
Continuous power dissipation (T_A = 25°C) (2)
QFN-28 (4mmx5mm)..... 3.1W
Storage temperature..... -55°C to +150°C
Junction temperature (T_J) .....150°C
Lead temperature (solder) .....260°C

ESD Ratings

Human body model (HBM) ..... ±2000V
Charged-device model (CDM) ..... ±2000V

Recommended Operating Conditions (3)

Input voltage (V_{IN}) .....8V to 80V
Input voltage (V_{REG}).....8.5V to 14V
OCREF voltage (V_{OC}) .....0.125V to 2.4V
Operating junction temp (T_J).... -40°C to +150°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-28 (4mmx5mm)..... 40..... 9.... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on a JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 48V, V_{REG} = 12V, T_J = -40°C to 150°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
Input supply voltage	V_{IN}		8		80	V
Low-dropout (LDO) output voltage (V_{OUT})	V_{LDO}	I_{LDO} ≤ 5mA, V_{IN} > 15V	10.8	12	13.2	V
Gate driver supply voltage	V_{REG} (5)		8.5		14	V
Quiescent current	I_Q	nSLEEP = 1, not switching		0.7		mA
	I_{Q_SLEEP}	nSLEEP = 0			10	µA
Control Logic						
Input low logic threshold	V_{IL}				0.8	V
Input high logic threshold	V_{IH}		2.1			V
Logic input current	$I_{IN(H)}$	V_{IH} = 0.8V	-2.5		+2.5	µA
	$I_{IN(L)}$	V_{IL} = 5V	-15		+15	µA
nSLEEP pull-down resistance	$R_{SLEEP-PD}$			450		kΩ
Internal pull-down resistance	R_{PD}			450		kΩ
Fault Outputs (Open-Drain Output)						
Output low voltage	V_{OL}	I_{OUT} = 5mA			0.2	V
Output high leakage current	I_{OH}	V_{OUT} = 3.3V			2	µA
Protection Circuits						
V_{REG} under-voltage lockout (UVLO) rising threshold	V_{REG_RUVLO}		6.5	7.5	8.5	V
V_{REG} UVLO falling threshold	V_{REG_FUVLO}		6	6.8	7.6	V
V_{REG} UVLO hysteresis	V_{REG_HYS}			670		mV
V_{IN} UVLO rising threshold	V_{VIN_RUVLO}		3.6	4	4.7	V
V_{IN} UVLO falling threshold	V_{VIN_FUVLO}		3.3	3.8	4.6	V
V_{IN} UVLO hysteresis	V_{VIN_HYS}			100		mV
V_{BST} UVLO threshold	V_{BST_UVLO}	Voltage between SHx and BSTx		6.3		V
OCREF threshold	V_{OC}	V_{OC} = 1V	0.8	1	1.2	V
		V_{OC} = 2.4V	2.18	2.4	2.62	V
Over-current protection (OCP) deglitch time	t_{OC}			2.7		µs
Sleep wake-up time	t_{SLEEP}			2		ms
Thermal shutdown	T_{TSD} (5)			175		°C
Thermal shutdown hysteresis	T_{TSD_HYS} (5)			20		°C
Gate Drivers						
Bootstrap (BST) diode forward voltage	V_{FBOOT}	I_D = 10mA			1.2	V
		I_D = 50mA			2.9	V
Maximum source current	DS_O (5)			0.8		A
Maximum sink current	DS_I (5)			1		A
Gate driver pull-up resistance	R_{UP}	V_{DS} = 1V		7		Ω
High-side (HS) gate driver pull-down resistance	R_{HS-DN}	V_{DS} = 1V	0.6		4.5	Ω
Low-side (LS) gate driver pull-down resistance	R_{LS-DN}	V_{DS} = 1V	0.6		4.5	Ω
LS automatic turn-on time	t_{LS}			4.6		µs
Dead time (DT)	t_{DEAD}	R_{DT} = 10kΩ		560		ns
		R_{DT} = 100kΩ		4.5		µs
		DT tied to GND		77		ns

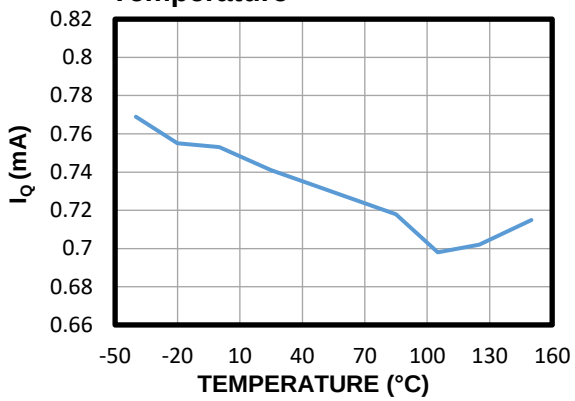
Note:

5) Guaranteed by design.

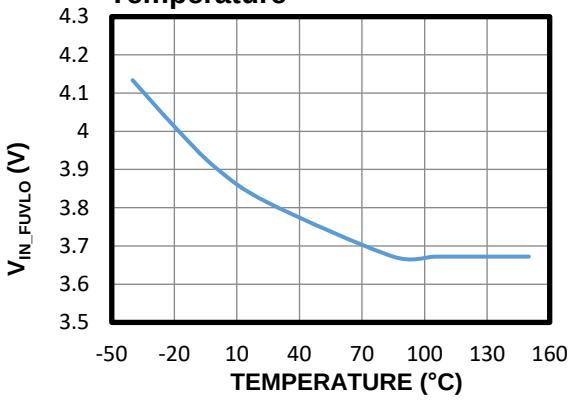
TYPICAL CHARACTERISTICS

V_{IN} = 48V, unless otherwise noted.

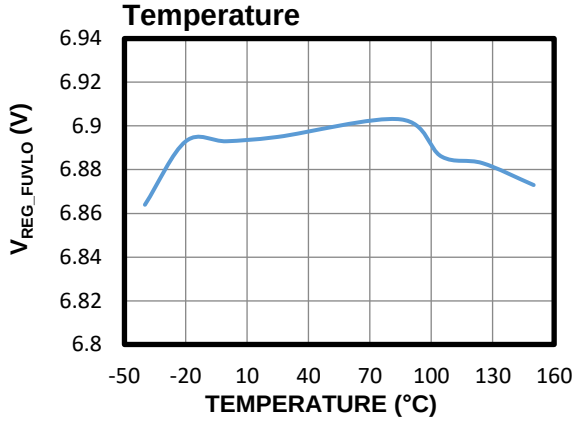
Quiescent Current vs. Temperature



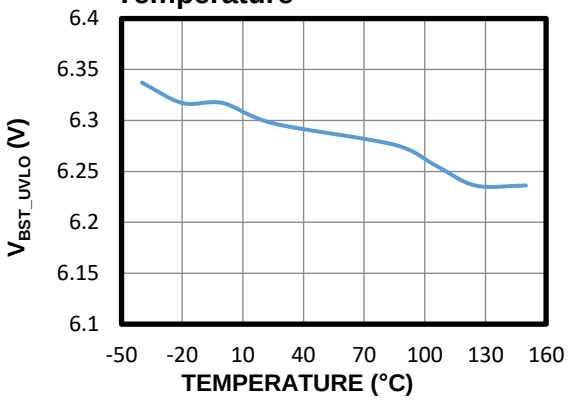
V_{IN} UVLO Falling Threshold vs. Temperature



V_{REG} UVLO Falling Threshold vs. Temperature

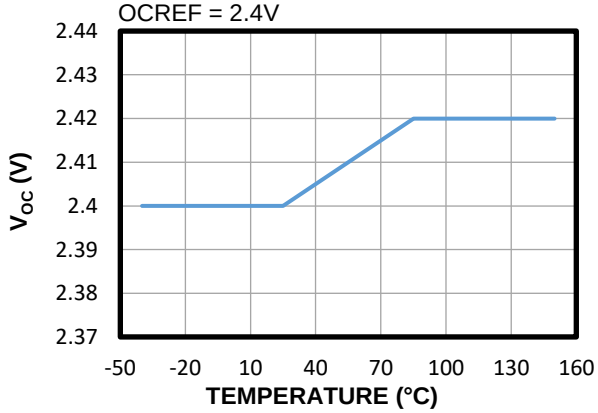


V_{BST} UVLO Threshold vs. Temperature

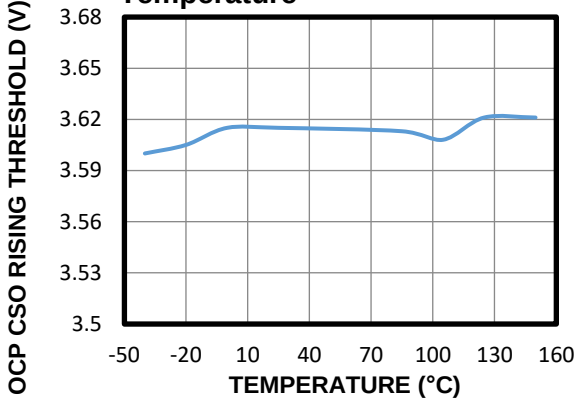


OCREF Threshold vs. Temperature

OCREF = 2.4V

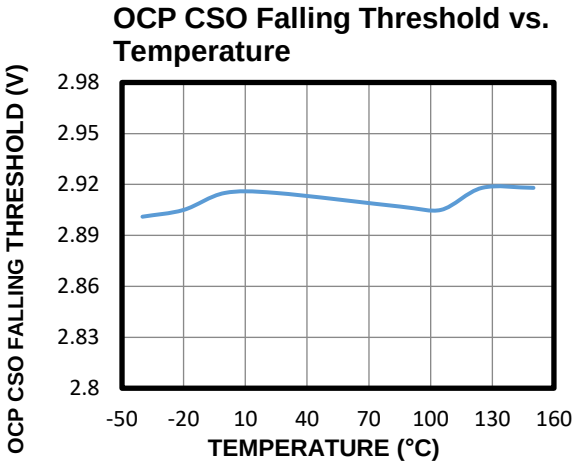


OCP CSO Rising Threshold vs. Temperature



TYPICAL CHARACTERISTICS *(continued)*

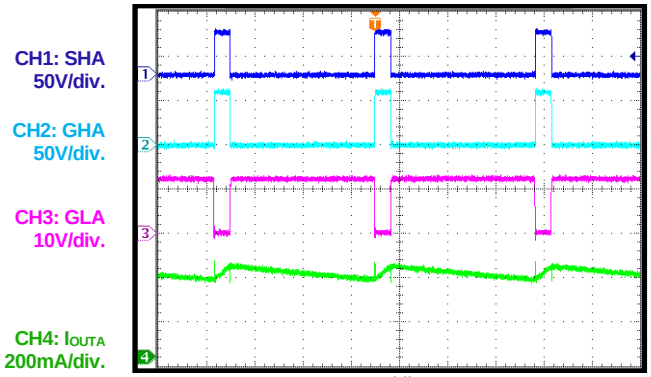
V_{IN} = 48V, unless otherwise noted.



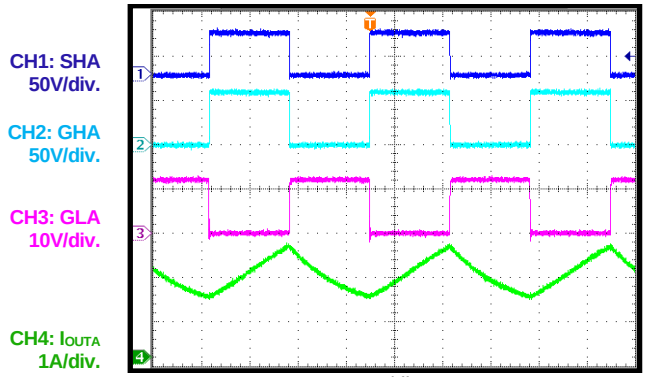
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 48V, OCREF = 0.5V, R_{DT} = 1kΩ, phase A switching, phase B low-side (LS) enabled, f_{PWMA} = 30kHz, T_A = 25°C, resistor + inductor load = 5Ω + 1mH/phase with star connection, unless otherwise noted.

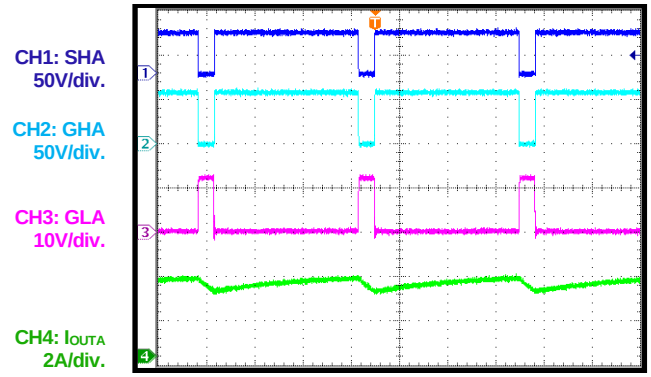
Steady State
Duty cycle = 10%



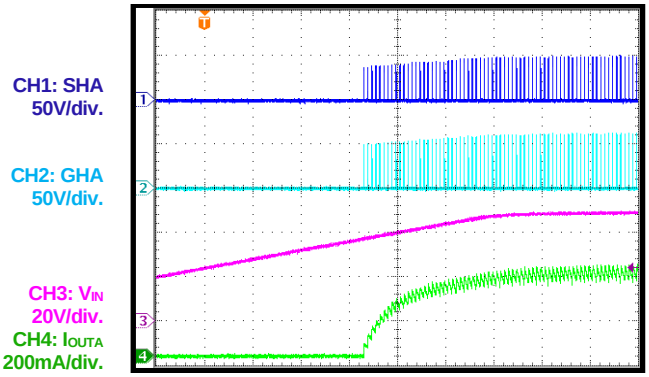
Steady State
Duty cycle = 50%



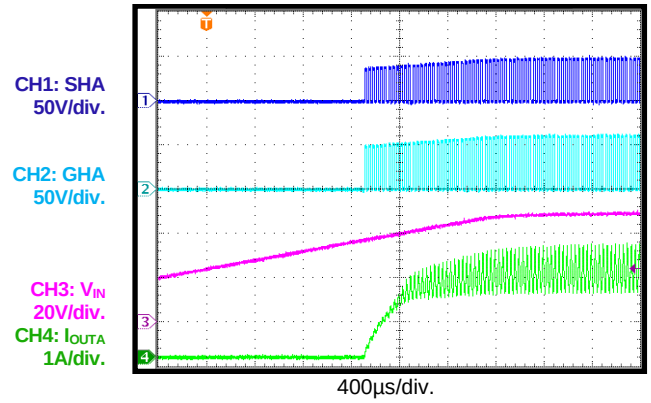
Steady State
Duty cycle = 90%



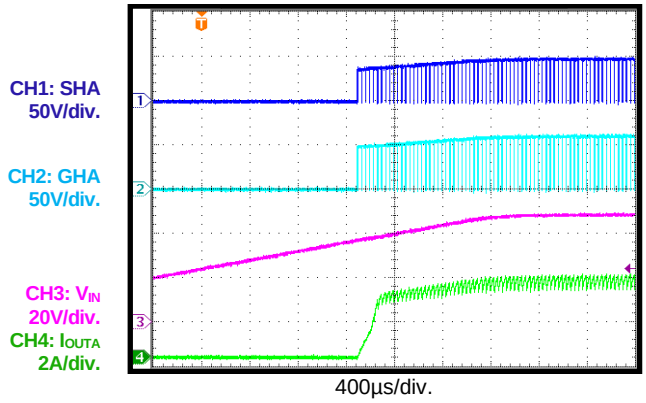
Power Ramping Up
Duty cycle = 10%



Power Ramping Up
Duty cycle = 50%



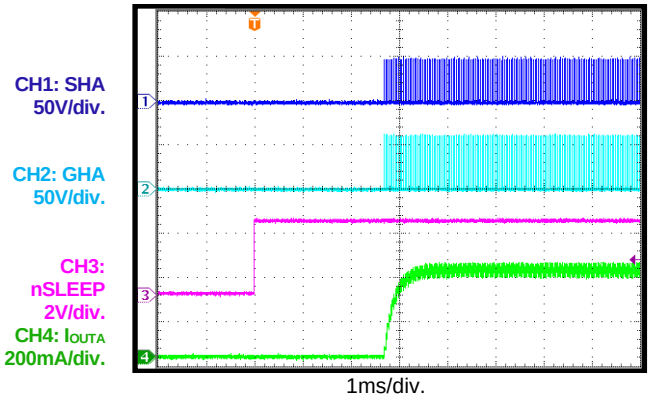
Power Ramping Up
Duty cycle = 90%



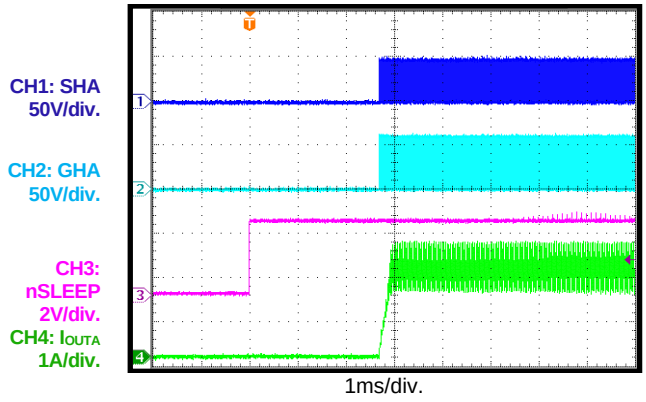
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 48V, OCREF = 0.5V, R_{DT} = 1kΩ, phase A switching, phase B LS enabled, f_{PWMA} = 30kHz, T_A = 25°C, resistor + inductor load = 5Ω + 1mH/phase with star connection, unless otherwise noted.

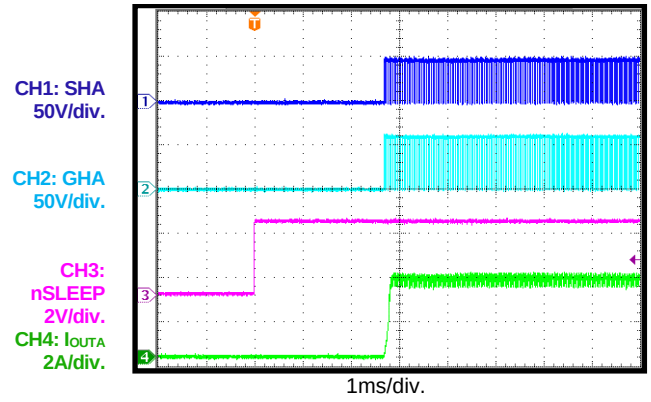
Sleep Recovery
Duty cycle = 10%



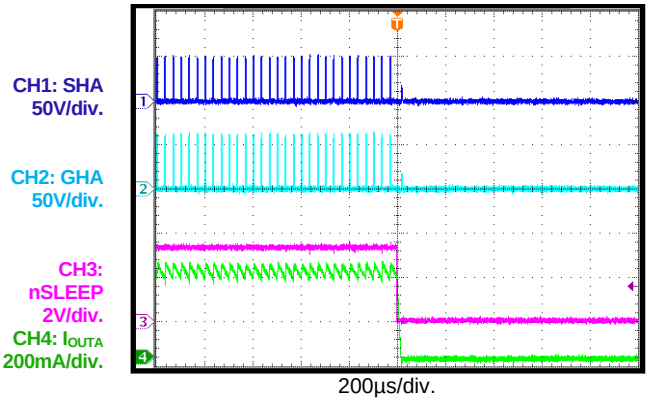
Sleep Recovery
Duty cycle = 50%



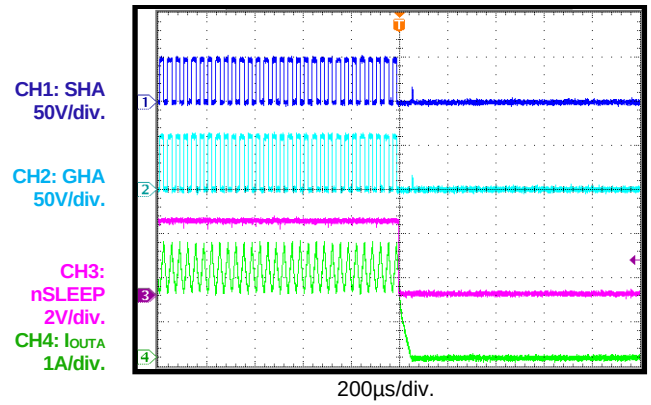
Sleep Recovery
Duty cycle = 90%



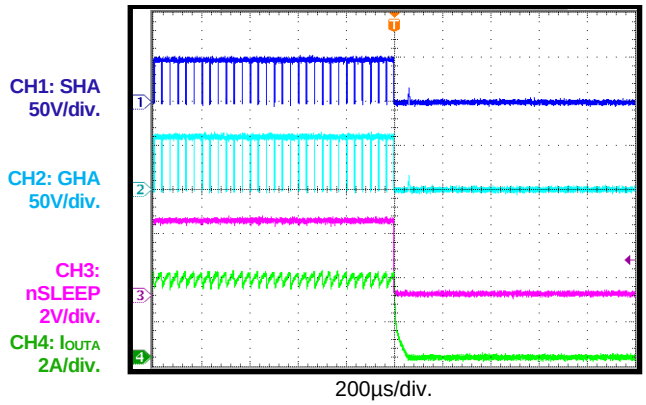
Sleep Entry
Duty cycle = 10%



Sleep Entry
Duty cycle = 50%



Sleep Entry
Duty cycle = 90%



FUNCTIONAL BLOCK DIAGRAM

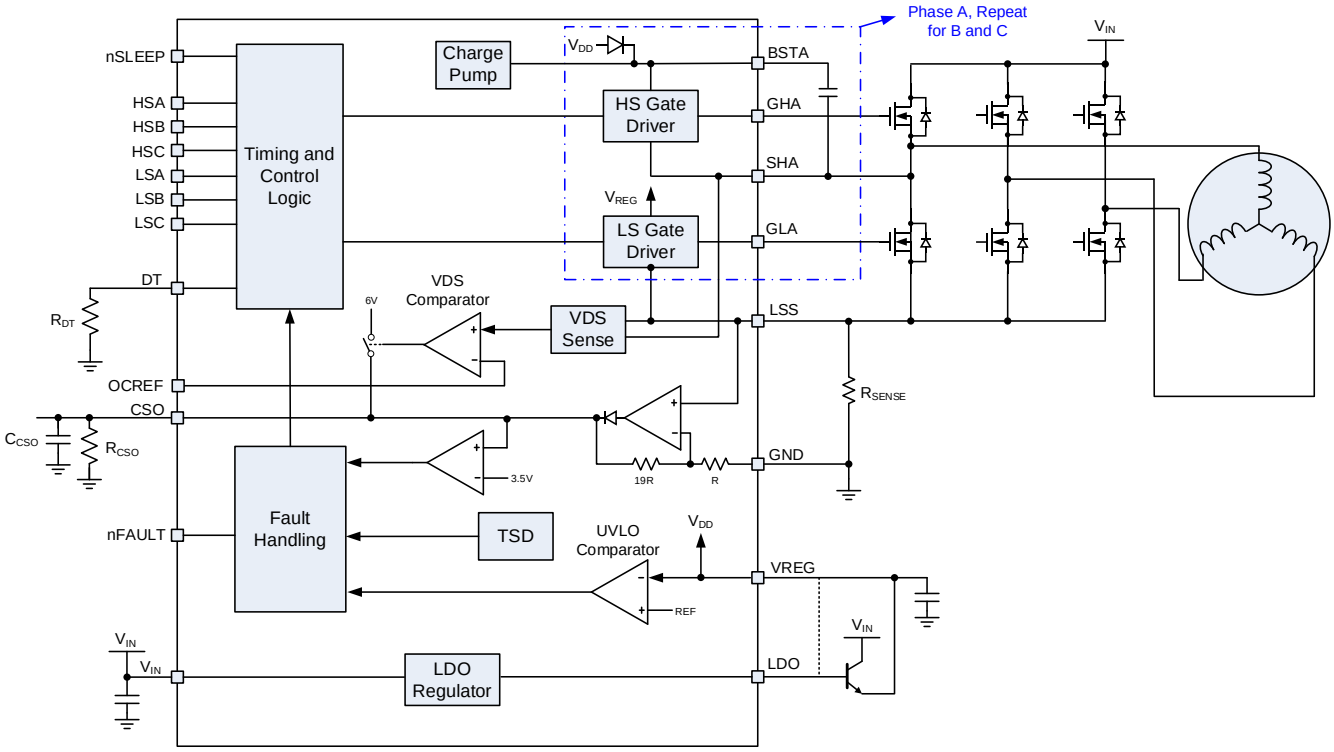


Figure 1: Functional Block Diagram

OPERATION

The MPQ6539-AEC1 is a three-phase, brushless DC (BLDC) motor pre-driver that can drive three half-bridges with a 0.8A source and 1A sink current capability. The device supports operation of up to 80V and features a low-power sleep mode, which disables the device and draws a very low supply current.

The MPQ6539-AEC1 offers several flexible features, such as adjustable dead-time (DT) control and over-current protection (OCP), allowing the device to support a wide range of applications.

Start-Up Sequence

The start-up sequence begins when a voltage is applied to the VIN pin and the voltage is present on the VREG pin. The VREG pin is typically supplied via an internal low-dropout (LDO) regulator connected to VIN, but other power sources can be used.

To initiate a start-up, the input voltage (V_{IN}) must be above 4.5V and the gate driver supply voltage (V_{REG}) must be above its under-voltage lockout (UVLO) threshold (7.5V). If VREG is supplied via the internal LDO regulator, V_{IN} must be at 8V before the part starts up. Once V_{REG} exceeds its UVLO threshold, the MPQ6539-AEC1 sequentially turns on each low-side MOSFET (LS-FET) in succession to charge the bootstrap (BST) capacitors.

The start-up process takes between 1ms and 2ms, then the device starts responding to logic inputs and drives the outputs.

Input Logic

The device can enter a low-power state by pulling the nSLEEP pin low. In this state, all internal circuits are disabled. All inputs are ignored when nSLEEP is active low. To exit sleep mode, pull nSLEEP high and wait about 2ms, then issue a pulse-width modulation (PWM) command to provide the internal circuitry time to stabilize.

The HSx pins control the high-side MOSFET (HS-FET) gate drivers for each phase. The LSx pins control the LS-FET gate drivers. The device enforces a positive DT. If both the HSx and LSx pins are driven high, neither MOSFET is driven (see Table 1).

Table 1: Input Logic Truth Table

LSx	HSx	SHx
H	H	High impedance (Hi-Z)
H	L	GND
L	H	VIN
L	L	Hi-Z

nFAULT

The nFAULT pin reports to the system if a fault condition occurs, such as OCP or over-temperature protection (OTP). The nFAULT pin is an open-drain output, and is pulled low if a fault condition occurs. Once the fault condition is removed, nFAULT is pulled high via an external pull-up resistor.

Current-Sense (CS) Amplifier

An integrated current-sense (CS) amplifier amplifies the LSS voltage (V_{LSS}), relative to GND, by a factor of 20. The CSO pin is the output of the CS amplifier.

The CS amplifier only sources current. A minimum 1nF external capacitor must be connected between CSO and GND for stability.

During the PWM on time, the current flowing through the output MOSFETs also flows through the shared low-side (LS) CS resistor (R_{SENSE}). The current generates a voltage that is amplified via the CS amplifier, and charges the external capacitor on CSO. During the PWM off time, the current recirculates through the LS-FETs and does not pass through R_{SENSE}, so there is zero voltage across it. During this time, the capacitor on CSO discharges through the internal feedback (FB) resistor (R_{FB}, typically 450kΩ) and any external resistor connected to ground. Select an external resistor and capacitor to provide a filter to hold the current value through the PWM off time. A 1kΩ or greater external resistor is recommended.

Over-Current Protection (OCP) and Current Regulation

The voltage across each LS-FET (V_{DS}) is monitored via an internal comparator. If an over-current (OC) condition occurs, then all the output MOSFETs turn off. The OC shutdown voltage threshold is configured via the OCREF pin when an external reference voltage (V_{REF}) is applied with a DAC or resistor divider.

When the MOSFET's V_{DS} exceeds OCREF, CSO is pulled internally to 6V. If CSO exceeds 3.5V, an OCP event is detected, all output MOSFETs turn off, and nFAULT is pulled active low.

Once the current flowing through the LS-FETs and sense resistors (R_{SENSE}) stop, the CSO voltage (V_{CSO}) starts to fall at a rate determined via the external capacitor and resistor. Once V_{CSO} falls below 2.9V, the output MOSFETs are reenabled and nFAULT is inactive.

The resulting off time is set via the external capacitor and internal R_{FB} in parallel with the external resistor (if used).

The off time (t_{OFF}) generated when CSO reaches 3.5V can be calculated with Equation (1):

$$t_{OFF}\,(\mu s) = 0.2 \times R(k\Omega) \times C(nF) \quad (1)$$

A longer off time is generated when V_{DS} exceeds OCREF. To reenable the outputs, pull CSO to 6V and let CSO decay to 2.9V. This off time (t_{OFF}) can be calculated with Equation (2):

$$t_{OFF}\,(\mu s) = 0.6 \times R(k\Omega) \times C(nF) \quad (2)$$

Where C is the capacitance between CSO and ground, and R is the total resistance between CSO and ground, comprised of the internal R_{FB} (450kΩ) in parallel with any external resistor to GND.

During current regulation, this feature limits the stall and start-up current of the motor by using an external CS resistor or the $R_{DS(ON)}$ LS-FET ($R_{DS(ON)\_LS}$). Using the $R_{DS(ON)\_LS}$ leads to lower accuracy.

In addition to LS current monitoring, a circuit monitors the output. If the output is driven high but does not exceed 4.5V, the circuit triggers a fault condition. This provides protection against a short to ground event, which would not be detected by LS current-sensing. If this occurs, the MPQ6539-AEC1 enters a latched fault state and disables all outputs. The MPQ6539-AEC1 remains latched off until it is reset via nSLEEP or UVLO.

Gate-Driver Voltage Regulator

To generate the voltage that drives the external MOSFET gates, a linear regulator is integrated into the MPQ6539-AEC1.

If a current exceeding 5mA is required to drive the high gate charge MOSFETs at a high switching frequency (f_{SW}), then an external NPN transistor (and optionally also a resistor) must be used to remove power dissipation from the IC.

For low-current applications, LDO is connected directly to VREG. For higher current requirements, an NPN transistor is used (see Figure 2).

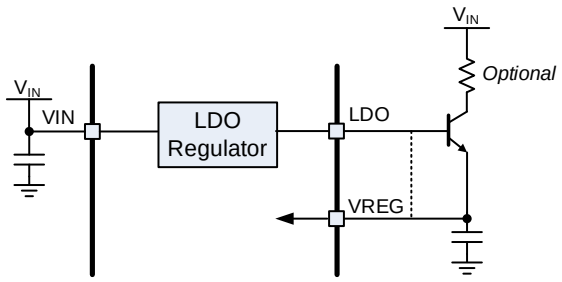


Figure 2: High-Current LDO Configuration

If necessary, an appropriate gate driver supply voltage can also be supplied directly to VREG via an external supply. In this case, connect only the capacitor to LDO. VIN must still be connected to the input supply voltage (V_{IN}).

Over-Current Protection (OCP) Deglitch Time

Due to the body diode's reverse-recovery current or the distributed inductance or capacitance, there is typically a current spike during the switching transition. Filtering is required to prevent the current spike from erroneously triggering OCP and shutting down the external MOSFET. An internal, fixed deglitch time (t_{OC}), which is also the minimum on time for the MOSFET, blanks the VDS monitor output when the outputs are switched.

Charge Pump and Bootstrap (BST)

The high-side (HS) gate driver voltage is generated via bootstrap (BST) capacitors connected between the SHx and BSTx pins. The bootstrap (BST) capacitor (C_{BST}) charges when the LS-FET turns on.

If the output is held high for a long period of time, C_{BST} discharges slowly and eventually leads to HS-FET gate driver loss. To prevent gate driver loss, an internal charge pump generates a voltage to maintain the C_{BST} charge.

The BST voltage (V_{BST}) is monitored via an under-voltage (UV) detection circuit. If V_{BST} falls below the VBST UVLO threshold, the part initiates a new start-up sequence.

Dead-Time (DT) Adjustment

To prevent shoot-through at any phase of the bridge, it is recommended to insert a dead time (t_{DEAD}) between a HS or LS shutdown and the next complementary turn-on event. t_{DEAD} for all three phases is set via a single dead-time (DT) resistor (R_{DT}) between the DT pin and ground. t_{DEAD} can be calculated with Equation (3):

$$t_{DEAD}\ (\mu s) = 0.044 \times R(k\Omega) + 0.1 \quad (3)$$

If DT is tied directly to GND, an internal minimum 77ns DT is applied. The 100kΩ maximum allowed resistance to GND generates a 4.5µs t_{DEAD}.

V_{REG} and V_{IN} Under-Voltage Lockout Protection

If V_{REG} falls below the V_{REG} UVLO threshold, the outputs are disabled and the nFAULT signal is asserted. Once V_{REG} exceeds the UVLO threshold, the device restarts and resumes normal operation with a BST refresh.

If V_{IN} falls below the V_{IN} UVLO threshold, all device circuitries disable and the internal logic is reset. The nFAULT pin is not asserted. Once V_{IN} and V_{REG} exceed their respective UVLO thresholds, the device restarts and resumes normal operation.

Thermal Shutdown

The device employs thermal monitoring. If the die temperature exceeds safe limits (175°C), all output MOSFETs turn off and the nFAULT pin is pulled low. Once the die temperature drops to a safe temperature (155°C), the IC restarts and resumes normal operation.

APPLICATION INFORMATION

Bootstrap (BST) Components

The primary source of charge to enable the HS-FETs is provided by the bootstrap capacitors. There are several considerations to be made when selecting the capacitance.

When the output is driven low, the bootstrap capacitor (C_{BST}) is charged from VREG through an internal diode. To turn on the HS-FET, the C_{BST} charge transfers to the HS-FET gate. If C_{BST} is too low, it will not contain enough charge to fully enhance the MOSFET.

C_{BST} is selected depending on the MOSFET total gate charge (Q_G). When the HS-FET is on, the charge stored in C_{BST} transfers to the HS-FET gate. For simplification, the minimum C_{BST} (C_{BOOT}) can be estimated with Equation (4):

$$C_{BOOT} > 8 \times Q_G \quad (4)$$

Where Q_G is the total gate charge of the MOSFET (in nC), and C_{BOOT} is in nF.

At the other extreme, if C_{BST} is too high, it takes a very long time to charge when the output is low due to the limited current-sourcing capability through the BST diode. The total power dissipated in the BST diode can also be a concern.

PCB Layout Guidelines

Efficient PCB layout is critical for optimizing the performance of the MOSFET gate drivers. The pre-driver is designed to accommodate a negative undershoot, but excessive negative undershoot can result in unstable operation or damage to the IC. For the best results, refer to Figure 3 and follow the guidelines below:

1. Make the connection between the HS source and LS drain as direct as possible to avoid a negative undershoot on the phase node due to parasitic inductance.
2. Use surface-mount N-channel MOSFETs that have a very short connection between the HS-FET and LS-FET.
3. Use wide copper areas for all of the high-current paths.
4. Place the supply bypass capacitors as close to the IC as possible.
5. Place multiple thermal vias under the exposed pad to improve thermal dissipation. This allows heat to move between the IC and a plane located on the backside of the PCB.

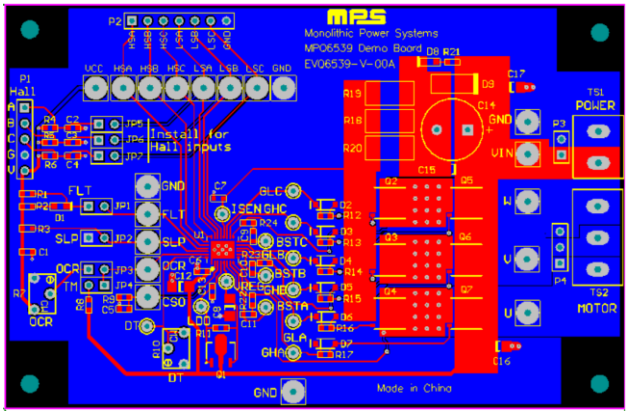


Figure 3: Recommended PCB Layout

TYPICAL APPLICATION CIRCUIT

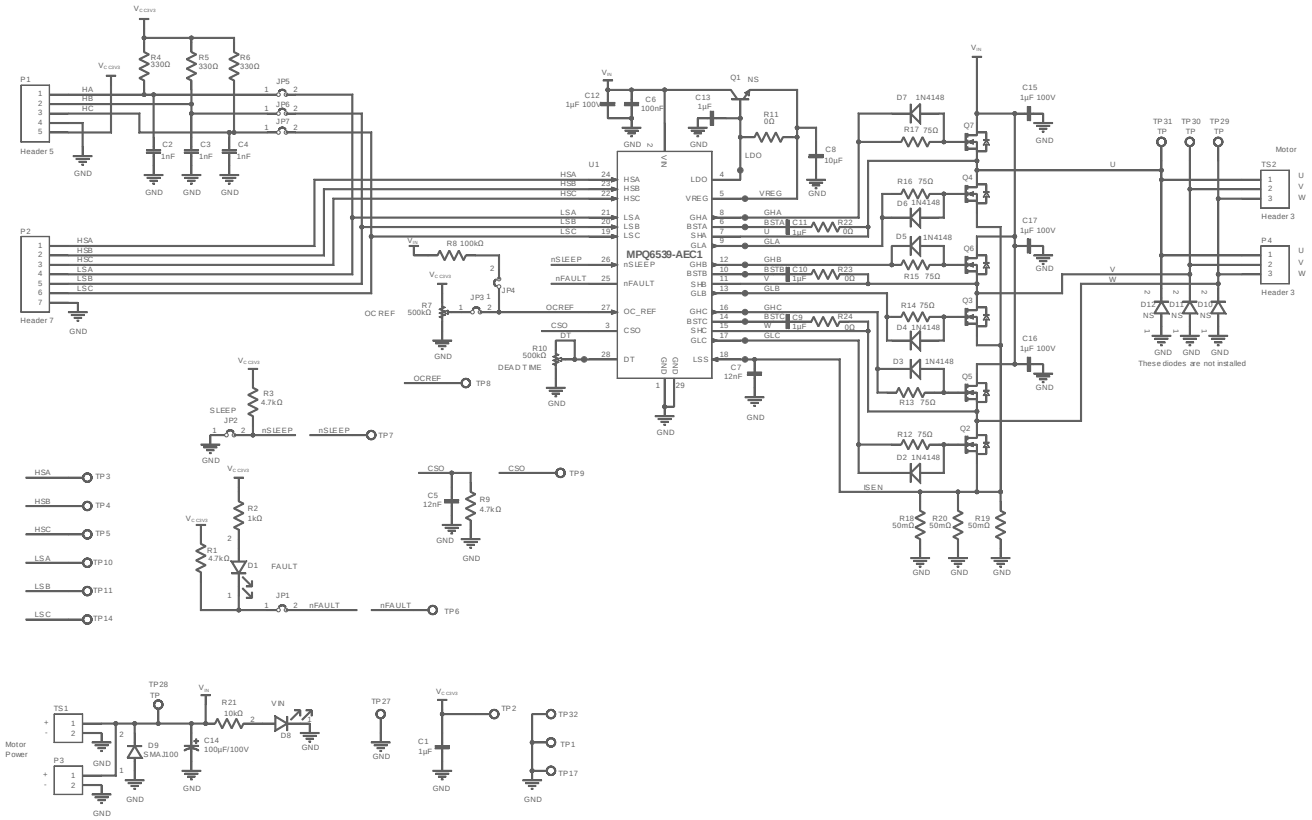
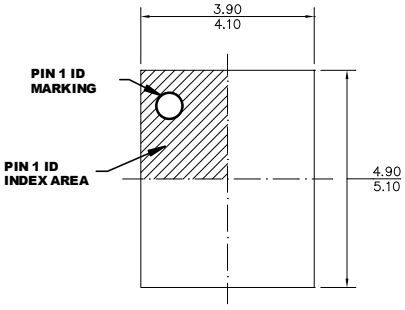


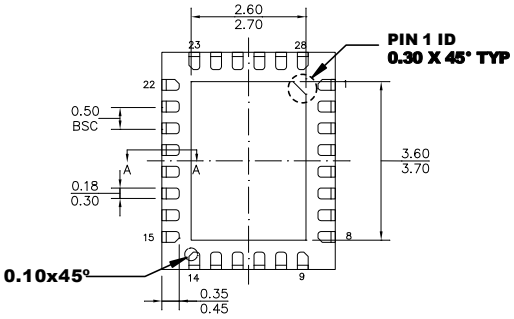
Figure 4: Typical Application Circuit

PACKAGE INFORMATION

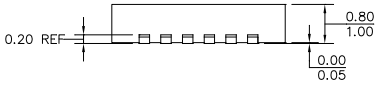
QFN-28 (4mmx5mm)
Wettable Flank



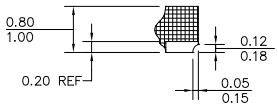
TOP VIEW



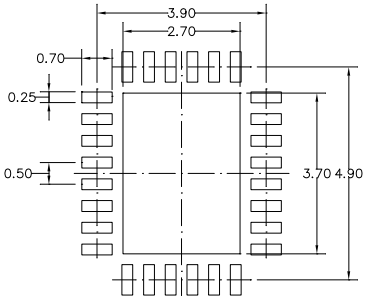
BOTTOM VIEW



SIDE VIEW



SECTION A-A

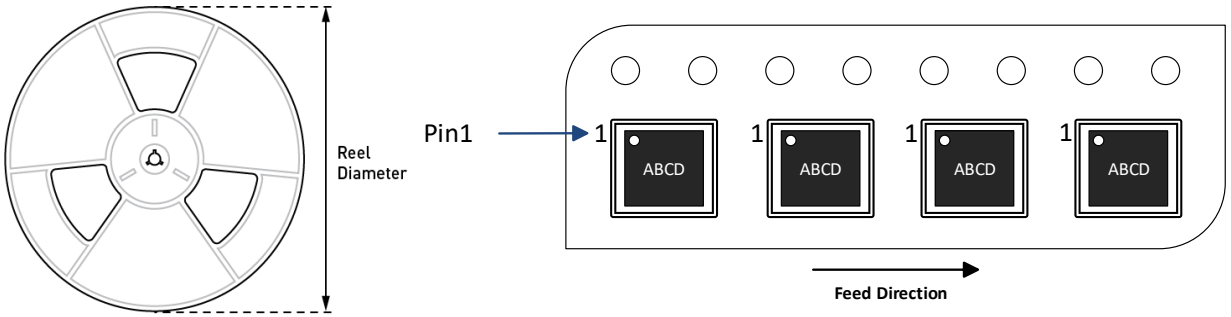


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) DRAWING CONFIRMS TO JEDEC MO-220, VARIATION VGHD-3.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tary	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ6539GVE-AEC1-Z	QFN-28 (4mmx5mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	12/16/2024	Initial Release	-