MPM54524

Fully Integrated, 16V, Quad 5A Output Power Module with I²C Interface

DESCRIPTION

The MPM54524 is an integrated, quad 5A power module with an I²C interface. The device offers a complete power solution with built-in turn-on/-off sequencing control, configurable soft start (SS), compensation, and various protection thresholds.

Constant-on-time (COT) control provides ultra-fast transient response. The output voltage (V_{OUTx}) (where x = A, B, C, or D) is adjustable via the I²C bus or preset via the multiple-time programmable (MTP) memory. The power-on/-off sequence is also configurable via the MTP or can be controlled via the I²C.

The MPM54524 offers configurable active voltage positioning (AVP), which generates a droop voltage (V_{DROOP}). This allows four channels in parallel with passive current balancing. In addition, buck regulator A (buck A) and buck regulator B (buck B) can operate in parallel for up to 10A in interleaving mode, which enables active current balancing. Full protection features include under-voltage lockout (UVLO), over-current protection (OCP), over-voltage protection (OVP), under-voltage protection (UVP), and thermal shutdown.

The MPM54524 requires a minimal number of external components and is available in a compact ECLGA (8mmx8mmx2.9mm) package.

FEATURES

- Wide 4V to 16V Input Voltage (V_{INy}) Range (where y = 1 or 2)
- Adaptive Constant-On-Time (COT) for Ultra-Fast Transient Response
- Parallel Operation with Passive or Active Current Balancing
- I²C-Configurable Output Voltage (V_{OUTx})
- Configurable f_{SW}: 500kHz to 1000kHz
- Differential V_{OUTx} Remote Sense
- Accurate V_{OUTx}, I_{OUTx}, and Junction Temperature (T_J) Monitoring via the I²C
- Open-Drain Power Good (PG) Indication
- Configurable I²C Slave Address
- Selectable Pulse-Frequency Modulation (PFM)/Pulse-Width Modulation (PWM) Mode, Adjustable Frequency, and Current Limit via the I²C
- Pre-Biased Start-Up
- Protections Include OCP, UVP, UVLO, OVP and Thermal Shutdown
- Available in ECLGA (8mmx8mmx2.9mm) Package

APPLICATIONS

- FPGA and ASIC Power Supplies
- Networking and Telecommunications
- Optical Module Power Supplies

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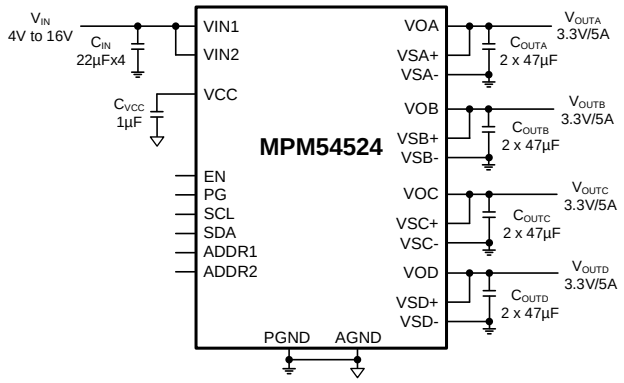
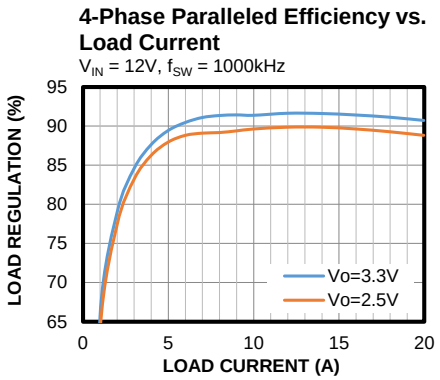
TYPICAL APPLICATION





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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPM54524GCQ-xxxx**	ECLGA-51 (8mmx8mmx2.9mm)	*See Below*	3
MPM54524GCQ-0000**	ECLGA-51 (8mmx8mmx2.9mm)	*See Below*	3

* For Tray, add suffix -T (e.g. MPM54524GCQ-xxxx-T).

* For Tape & Reel, add suffix -Z (e.g. MPM54524GCQ-xxxx-Z).

** "xxxx" is the configuration code identifier for the register setting stored in the multiple-time programmable (MTP) memory. The default code is "0000". Each "x" can be a hexadecimal value between 0 and F. Work with an MPS FAE to create this unique number, even if ordering the "0000" code. See Table 3 on page 51 for the MPM54524GCQ-0000 detailed configuration.

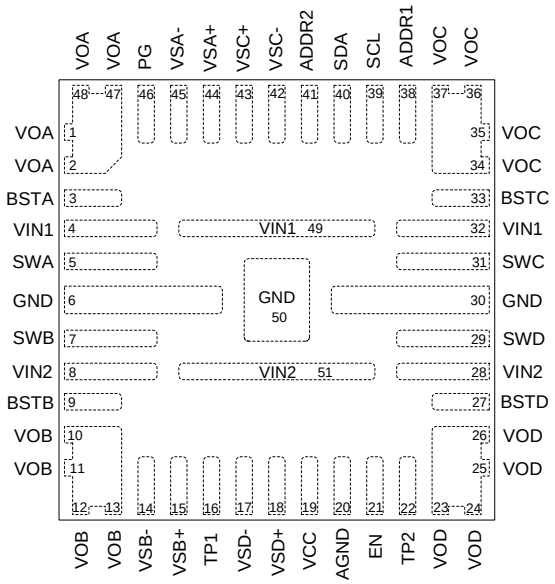
TOP MARKING

MPSYYWW
MP54524
LLLLLLLLL
M

MPS: MPS prefix
YY: Year code
WW: Week code
MP54524: Part number
LLLLLLLLL: Lot number
M: Module

PACKAGE REFERENCE

TOP VIEW



ECLGA-51 (8mmx8mm)

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PIN FUNCTIONS

Pin #	Name	Description
1, 2, 47, 48	VOA	**Buck regulator A (buck A) output.** The VOA pin is the output of buck A.
3	BSTA	**Buck A bootstrap.** Float the BSTA pin.
4, 32, 49	VIN1	**Supply voltage input of buck A and buck regulator C (buck C).** Ceramic capacitors are required to decouple the input rail. Connect the VIN1 and VIN2 pins using a wide PCB trace.
5	SWA	**Buck A switching node.** Float the SWA pin.
6, 30, 50	GND	**Power ground.** The GND pin requires special consideration during PCB layout. Connect GND using copper traces and vias.
7	SWB	**Buck B switching output.** Float the SWB pin.
8, 28, 51	VIN2	**Supply voltage input of buck regulator B (buck B) and buck regulator D (buck D).** Ceramic capacitors are required to decouple the input rail. Connect the VIN1 and VIN2 pins using a wide PCB trace.
9	BSTB	**Buck B bootstrap.** Float the BSTB pin.
10, 11, 12, 13	VOB	**Buck B output.** The VOB pin is the output of buck B.
14	VSB-	**Remote-sense ground of buck B.** Kelvin connect the VSB- pin to the ground node of the output capacitor (C_{OUT}) for buck B.
15	VSB+	**Positive feedback of buck B.** Connect the VSB+ pin to buck B's output.
16	TP1	**Test pin.** Float the TP1 pin.
17	VSD-	**Ground of buck D.** Kelvin connect the VSD- pin to the ground node of C_{OUT} for buck D.
18	VSD+	**Positive feedback of buck D.** Connect the VSD+ pin to buck D's output.
19	VCC	**Internal 3.3V low-dropout (LDO) output.** The driver and control circuits are powered from the VCC pin voltage (V_{CC}). Decouple VCC using a 1μF ceramic capacitor placed as close to VCC as possible.
20	AGND	**Analog ground.** Connect the AGND pin to the power GND pin.
21	EN	**Enable control.** Pull the EN pin high to enable the module; pull EN low to disable the module.
22	TP2	**Test pin.** Float the TP2 pin.
23, 24, 25, 26	VOD	**Buck D output.** The VOD pin is the output of Buck D.
27	BSTD	**Buck D bootstrap.** Float the BSTD pin.
29	SWD	**Buck D switching output.** Float the SWD pin.
31	SWC	**Buck C switching output.** Float the SWC pin.
33	BSTC	**Buck C bootstrap.** Float the BSTC pin.
34, 35, 36, 37	VOC	**Buck C output.** The VOC pin is the output of buck C.
38	ADDR1	**I²C bus address.** There are 9 selectable I²C addresses. To select the I²C address, pull the ADDR1 pin high, low, or float the pin.
39	SCL	**I²C clock.**
40	SDA	**I²C data.**
41	ADDR2	**I²C address.** There are 9 I²C selectable addresses by pulling the ADDR2 pin high, low, or floating the pin.
42	VSC-	**Remote-sense ground of buck C.** Kelvin connect the VSC- pin to the ground node of C_{OUT} for buck C.

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PIN FUNCTIONS *(continued)*

Pin #	Name	Description
43	VSC+	**Positive feedback of buck C.** Connect the VSC+ pin to buck C's output directly.
44	VSA+	**Positive feedback of buck A.** Connect buck A's output to the VSA+ pin directly. In dual-phase interleaving mode, VSA+ must be connected to VSB+.
45	VSA-	**Remote-sense ground of buck A.** Kelvin connect the VSA- pin to the ground node of C_{OUT} for buck A.
46	PG	**Open-drain power good output.** Pull the PG pin low when any enabled regulator drops below the under-voltage (UV) threshold. Pull PG low when all the regulators are disabled.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{INy}) 18V
V_{SWx_DC} .....-0.3V to V_{IN} + 0.3V
V_{BSTx} ..... V_{SW} + 4V
VOA, VOB, VOC, VOD 6V
V_{CC} 4.5V
V_{CC}, ADDR1, ADDR2, PG (1s) (2)……..
……6V
All other pins .....-0.3V to +4.3V
Continuous power dissipation (T_A = 25°C) (6)
..... 7.8W
Junction temperature (T_J) .....150°C
Storage temperature ..... -65°C to +150°C

ESD Ratings

Human body model (HBM) ..... ±2kV
Charged-device model (CDM) ..... ±2kV

Recommended Operating Conditions (3)

Supply voltage (V_{INy}) .....4V to 16V
Output voltage (V_{OUTx}).....0.4V to 5.5V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance (4) (5) (6) (7) (8)

θ_{JA}.....16°C/W
θ_{JC_TOP}.....0.3°C/W
θ_{JB}.....4.4°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) Voltage rating during multiple-time programmable (MTP) memory configuring.
3) The device is not guaranteed to function outside of its operating conditions.
4) θ_{JA} is the junction-to-ambient thermal resistance, θ_{JC_TOP} is the junction-to-case top thermal characterization parameter, and θ_{JB} is the junction-to-board thermal characterization parameter.
5) The thermal parameter is based on testing on the MPS evaluation board, EVM54524-CQ-00A, under no airflow cooling conditions in a standard enclosure. The EVM54524-CQ-00A is a 4-layer, 2oz board (8.1cmx8.1cm).
6) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature.
7) The junction-to-case top thermal characterization parameter, θ_{JC_TOP}, estimates the junction temperature in the real system, based on the equation, $T_J = \theta_{JC_TOP} \times P_{LOSS} + T_{CASE_TOP}$, where P_{LOSS} is the entire loss of the module in real application, and T_{CASE_TOP} is the case top temperature.
8) The junction-to-board thermal characterization parameter, θ_{JB}, estimates the junction temperature in the real system, based on the equation, $T_J = \theta_{JB} \times P_{LOSS} + T_{BOARD}$, where P_{LOSS} is the entire loss of the module in real application, and T_{BOARD} is the the board temperature.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C (9), typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (no switching)	I_{IN}	No switching, FB high, pulse-frequency modulation (PFM), no I²C communication		7.24		mA
Default switching frequency	f_{SW}	0Fh = 0xAA		1000		kHz
VIN1 or VIN2						
V_{INy} over-voltage (OV) rising threshold (where y = 1 or 2)	$V_{INy_OV_R}$	90h, bit[0] = 1'b1		15		V
V_{INy} OV hysteresis	$V_{INy_OV_HYS}$			0.25		V
V_{INy} under-voltage lockout (UVLO) rising threshold	$V_{INy_UVLO_R}$	90h, bit[1] = 1'b1, AFh, bits[1:0] = 2'b00	2.85	3.05	3.25	V
V_{INy} UVLO hysteresis	$V_{INy_UVLO_HYS}$			0.25		V
Enable (EN)						
EN logic high voltage	V_{EN_H}		1.2			V
EN logic low voltage	V_{EN_L}				0.35	V
EN internal pull-down resistance	R_{EN_DOWN}			2.7		MΩ
ADDR1 or ADDR2						
ADDR1 or ADDR2 logic high voltage	V_{ADDRx_H}		1.2			V
ADDR1 or ADDR2 logic low voltage	V_{ADDRx_L}				0.35	V
Buck Regulators (Buck A, Buck B, Buck C, or Buck D)						
Feedback (FB) voltage accuracy	V_{FBA}	25h, bit[3] = 1'b1, 15h = 0x90	3.31	3.36	3.41	V
	V_{FBB}	25h, bit[2] = 1'b1, 16h = 0x90	3.31	3.36	3.41	V
	V_{FBC}	25h, bit[1] = 1'b1, 17h = 0x90	3.31	3.36	3.41	V
	V_{FBD}	25h, bit[0] = 1'b1, 18h = 0x90	3.31	3.36	3.41	V
Output voltage (V_{OUTx}) (where X = A, B, C, or D) under-voltage (UV) rising threshold	$V_{OUTx_UV_R}$			85		% of V_{OUT}
V_{OUTx} UV falling threshold	$V_{OUTx_UV_F}$			80		% of V_{OUT}
Low-side (LS) current limit (source)	$I_{LS_VALLEY1}$	26h = 0xAA		5.5		A
Minimum on time (10)	t_{ON_MIN1}			30		ns
Minimum off time (10)	t_{OFF_MIN1}			120		ns
Output over-voltage protection (OVP) rising threshold	V_{OVP1_H}			112		% of V_{REF}
Output OVP recovery threshold	V_{OVP1_L}			109		% of V_{REF}

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C (9), typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Soft-start (SS) time of buck regulator A (buck A)	t_{SS_A}	12h, bits[7:6] = 2b'10, V_{OUT} = 10% to 90%		2		ms
SS time of buck regulator B (buck B)	t_{SS_B}	12h, bits[5:4] = 2b'10, V_{OUT} = 10% to 90%		2		ms
SS time of buck regulator C (buck C)	t_{SS_C}	12h, bits[3:2] = 2b'10, V_{OUT} = 10% to 90%		2		ms
SS time of buck regulator D (buck D)	t_{SS_D}	12h, bits[1:0] = 2b'10, V_{OUT} = 10% to 90%		2		ms
Discharge resistance	R_{DIS}	0Eh, bits[3:1] = 3b'000/111	-40%	10/2	+40%	Ω
Analog-to-Digital Converter (ADC)						
V_{OUTx} readback accuracy		V_{OUTx} = 3.3V	217	220	223	LSB
Output current readback accuracy		I_{OUT} = 4A		32		LSB
Power Good (PG)						
PG UV rising threshold	$V_{PG_UV_R}$	0Dh, bits[3:0] = 0000		98		% of V_{REF}
PG UV falling threshold	$V_{PG_UV_F}$			95		% of V_{REF}
PG OV rising threshold	$V_{PG_OV_R}$			105		% of V_{REF}
PG OV falling threshold	$V_{PG_OV_F}$			102		% of V_{REF}
PG output port sink current capability	V_{PG_SINK}	Sink 1mA			0.4	V
VCC Regulator						
V_{CC} UVLO rising threshold	V_{CC_R}		2.5	2.7	2.9	V
V_{CC} UVLO hysteresis	V_{CC_HYS}			300		mV
VCC voltage	V_{CC}	I_{CC} = 25mA		3.3		V
V_{CC} regulation	V_{CC_RG}	I_{CC} = 0mA to 25mA		1		%
Temperature Protections						
Thermal shutdown (10)	T_{OTP_R}			145		°C
Thermal hysteresis (10)	T_{HYS}			20		°C

Notes:

9) Not tested in production. Guaranteed by over-temperature correlation.
10) Not tested in production. Guaranteed by engineering sample characterization.

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I²C PORT SIGNAL CHARACTERISTICS (11)

V_{IN} = 12V, T_J = -40°C to +125°C (9), typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	C_B = 100pF		C_B = 400pF		Units
			Min	Max	Min	Max	
SCL clock frequency	f_{SCHL}		0	3.4	0	0.4	MHz
Set-up time for a repeated start command	t_{SU_STA}		160		600		ns
Hold time (repeated) for a start command	t_{HD_STA}		160		600		ns
SCL clock low period	t_{LOW}		160		1300		ns
SCL clock high period	t_{HIGH}		60		600		ns
Data set-up time	t_{SU_DAT}		10		100		ns
Data hold time	t_{HD_DAT}		0	70	0		ns
SCL signal rising time	t_{R_CL}		10	40	20 x 0.1C_B	300	ns
Rising time of the SCL signal after a repeated start command and an acknowledge bit	t_{F_CL1}		10	80	20 x 0.1C_B	300	ns
SCL signal falling time	t_{F_CL}		10	40	20 x 0.1Cb	300	ns
SDA signal rising time	t_{fDA}		10	80	20 x 0.1C_B	300	ns
SDA signal falling time	t_{F_DA}		10	80	20 x 0.1C_B	300	ns
Set-up time for stop command	t_{SU_STO}		160		600		ns
Bus free time between a stop and start condition	t_{BUF}		160		1300		ns
Data valid time	t_{VD_DAT}			16		90	ns
Data valid acknowledge time	t_{VD_ACK}			160		900	ns
Capacitive load for each bus line	C_B	SDA and SCL line		100		400	pF
		SDAH + SDA line, SCLH + SCL line		400		400	pF
Low-level noise margin	C_I	For each connected device		0.1V_{CC}	0.1V_{CC}		V
High-level noise margin	V_{NH}	For each connected device		0.2V_{CC}	0.2V_{CC}		V

Note:

11) The maximum I²C bus voltage must be below 4V. A 1.8V or 3.3V typical bus voltage is recommended.

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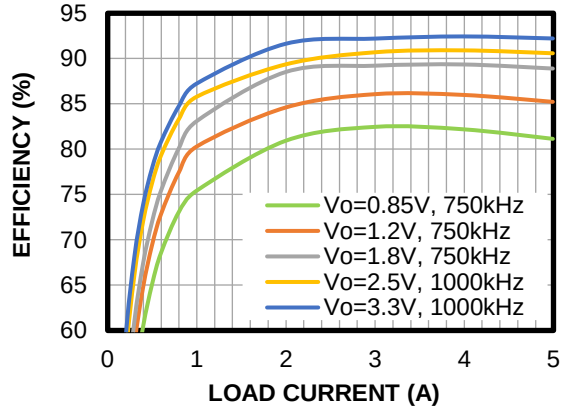
TYPICAL PERFORMANCE CHARACTERISTICS

Performance curves are tested on the evaluation board. V_{IN} = 12V, T_A = 25°C, unless otherwise noted.

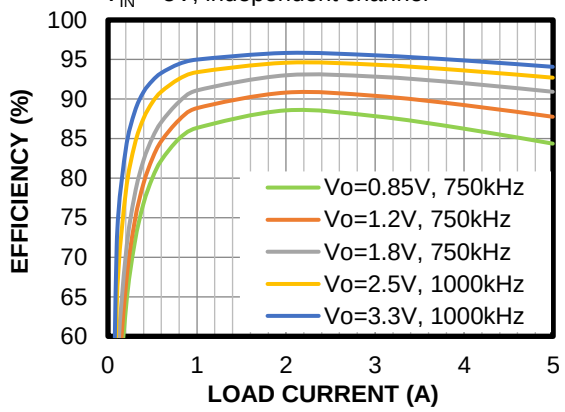
Efficiency vs. Load Current

V_{IN} = 12V, independent channel



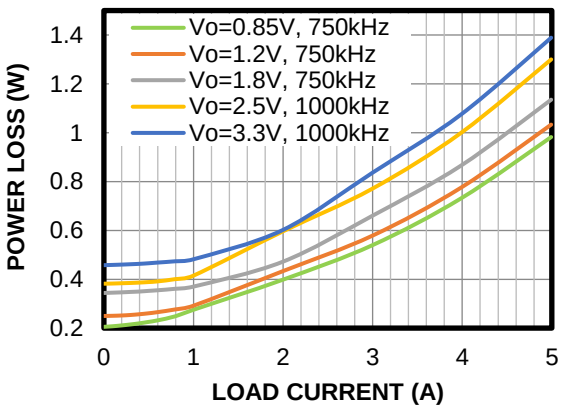
Efficiency vs. Load Current

V_{IN} = 5V, independent channel



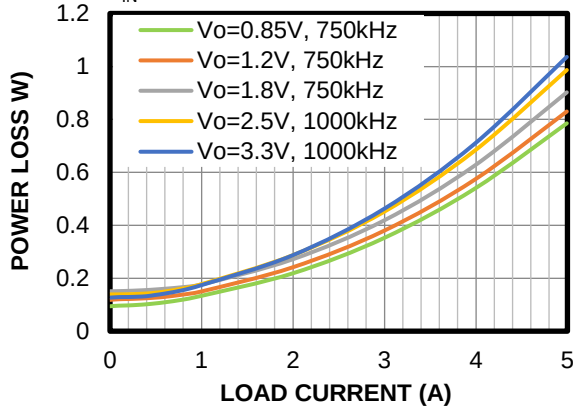
Power Loss vs. Load Current

V_{IN} = 12V



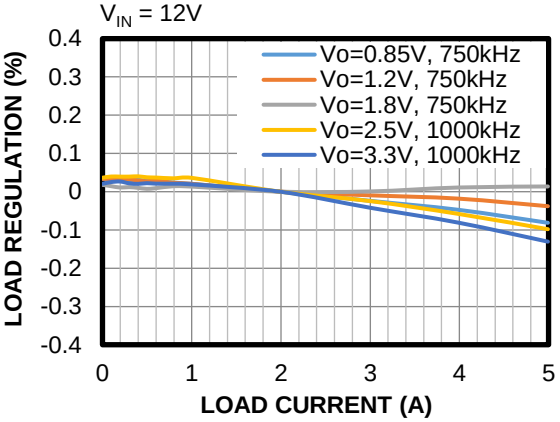
Power Loss vs. Load Current

V_{IN} = 5V



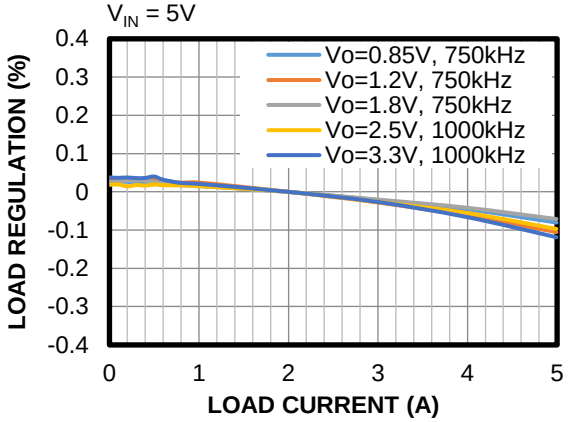
Load Regulation

V_{IN} = 12V



Load Regulation

V_{IN} = 5V



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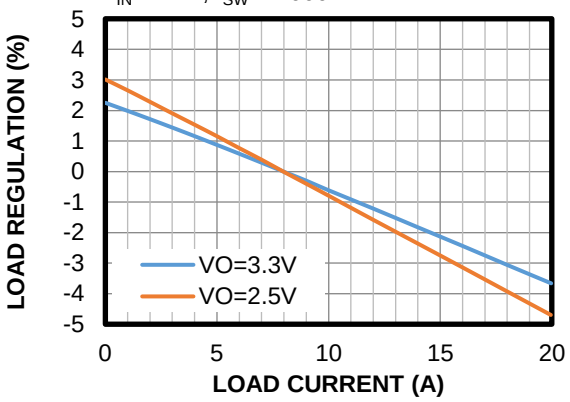
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance curves are tested on the evaluation board. V_{IN} = 12V, T_A = 25°C, unless otherwise noted.

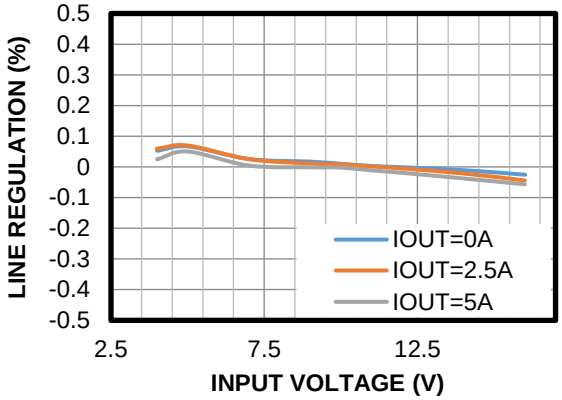
4-Phase Paralleled Load Regulation

V_{IN} = 12V, f_{SW} = 1000kHz



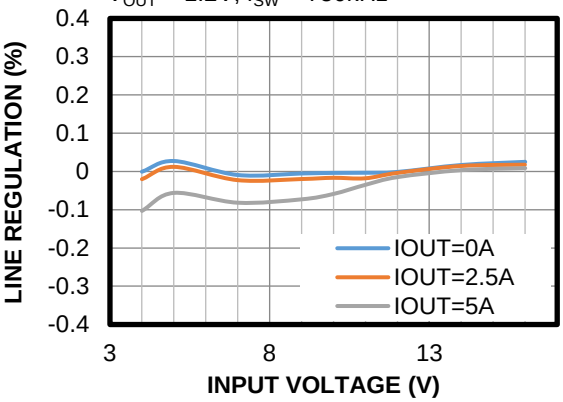
Line Regulation

V_{OUT} = 0.85V, f_{SW} = 750kHz



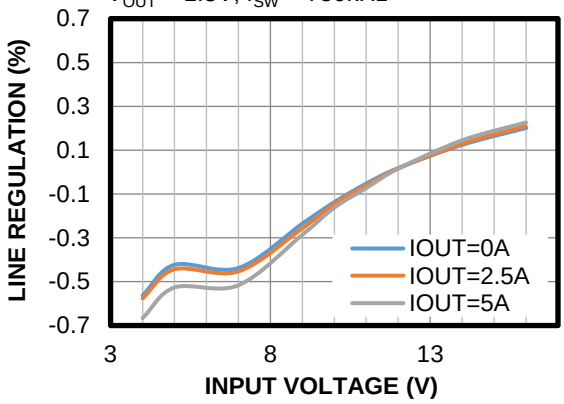
Line Regulation

V_{OUT} = 1.2V, f_{SW} = 750kHz



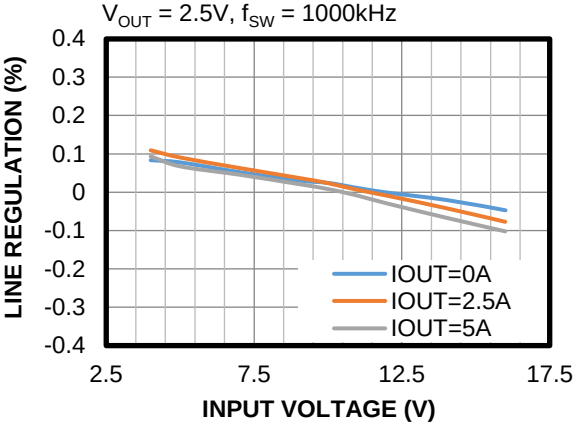
Line Regulation

V_{OUT} = 1.8V, f_{SW} = 750kHz



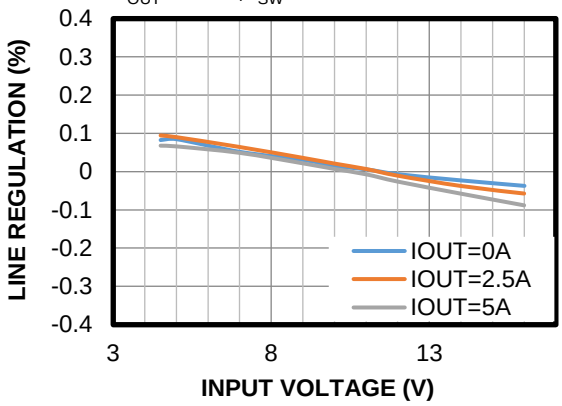
Line Regulation

V_{OUT} = 2.5V, f_{SW} = 1000kHz



Line Regulation

V_{OUT} = 3.3V, f_{SW} = 1000kHz



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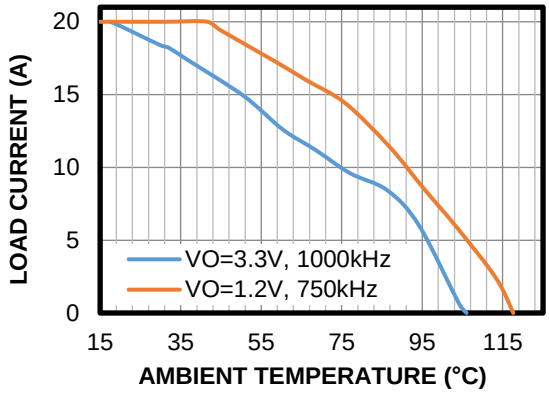
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance curves are tested on the evaluation board. V_{IN} = 12V, T_A = 25°C, unless otherwise noted.

Thermal Derating

V_{IN} = 12V, no airflow



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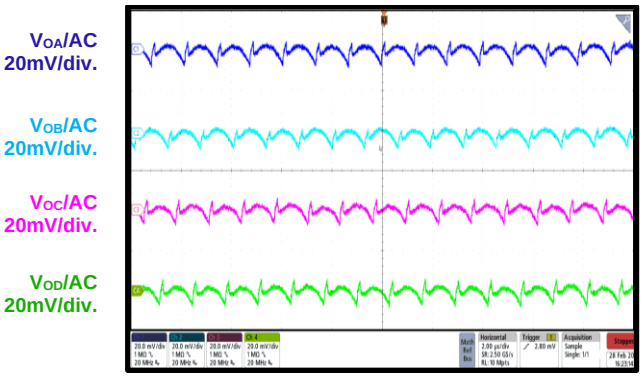
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance curves are tested on the evaluation board. V_{IN} = 12V, T_A = 25°C, unless otherwise noted.

Steady State

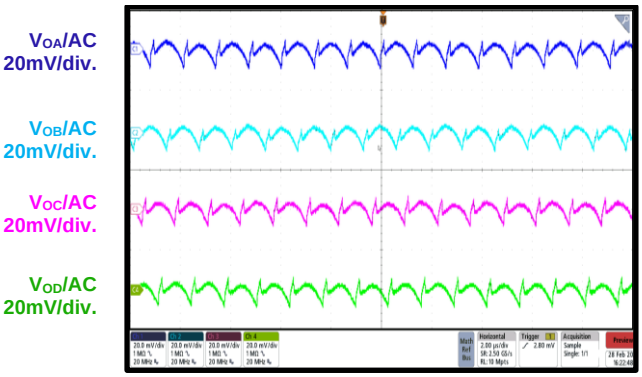
V_{IN} = 12V, V_{OUT} = 1.2V, f_{SW} = 750kHz,
I_{OUT} = 0A, single channel



2μs/div.

Steady State

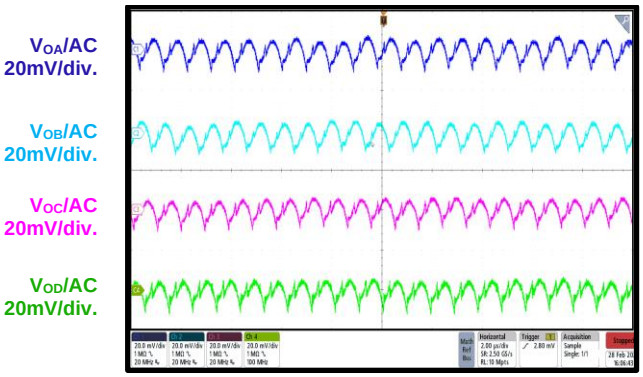
V_{IN} = 12V, V_{OUT} = 1.2V, f_{SW} = 750kHz,
I_{OUT} = 5A, single channel



2μs/div.

Steady State

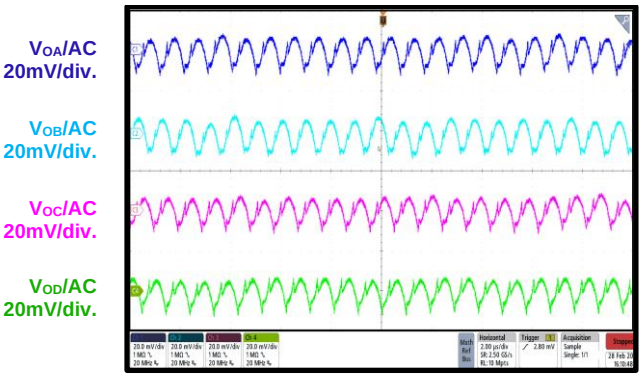
V_{IN} = 12V, V_{OUT} = 3.3V, f_{SW} = 1000kHz,
I_{OUT} = 0A, single channel



2μs/div.

Steady State

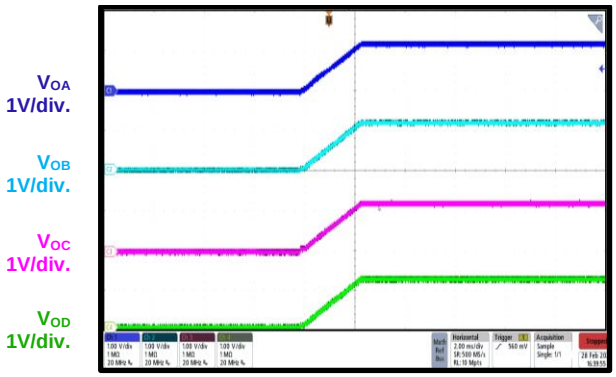
V_{IN} = 12V, V_{OUT} = 3.3V, f_{SW} = 1000kHz,
I_{OUT} = 5A, single channel



2μs/div.

Start-Up through EN

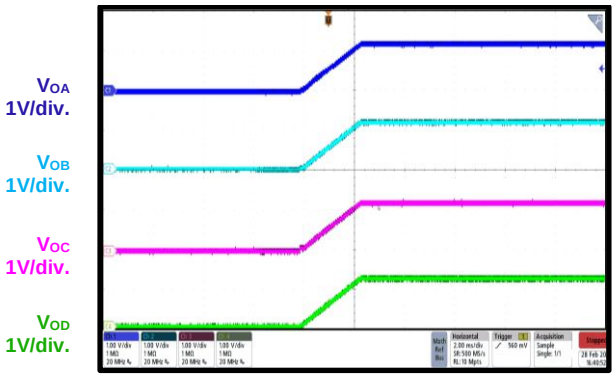
V_{IN} = 12V, V_{OUT} = 1.2V, f_{SW} = 750kHz,
I_{OUT} = 0A, single channel



2ms/div.

Start-Up through EN

V_{IN} = 12V, V_{OUT} = 1.2V, f_{SW} = 750kHz,
I_{OUT} = 5A, single channel



2ms/div.

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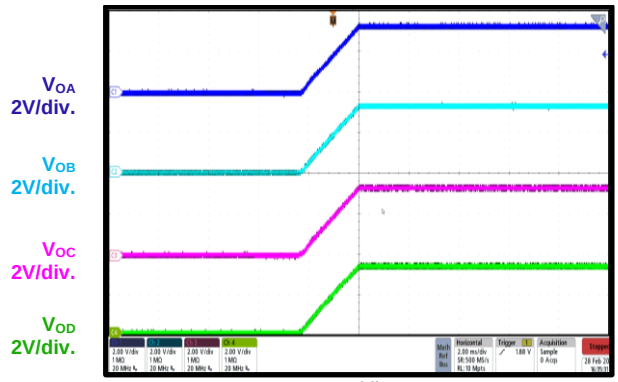
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance curves are tested on the evaluation board. V_{IN} = 12V, T_A = 25°C, unless otherwise noted.

Start-Up through EN

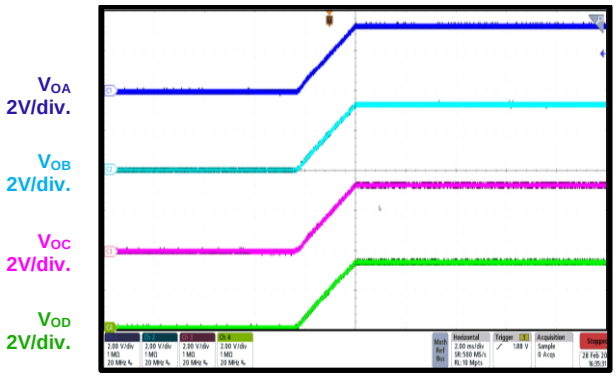
V_{IN} = 12V, V_{OUT} = 3.3V, f_{SW} = 1000kHz,
I_{OUT} = 0A, single channel



2ms/div.

Start-Up through EN

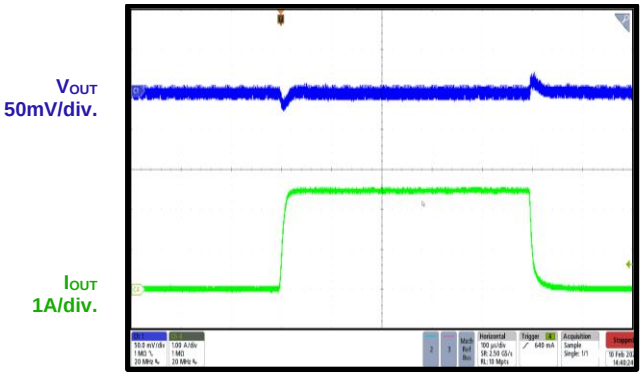
V_{IN} = 12V, V_{OUT} = 3.3V, f_{SW} = 1000kHz,
I_{OUT} = 5A, single channel



2ms/div.

Load Transient

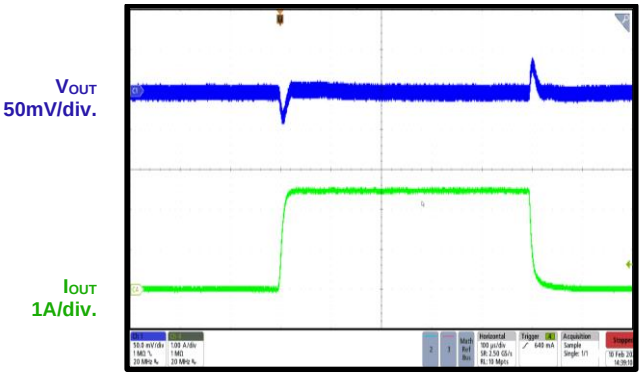
V_{IN} = 12V, V_{OUT} = 1.2V, f_{SW} = 750kHz,
I_{OUT} = 0A to 2.5A, 2.5A/µs e-load, single channel



100µs/div.

Load Transient

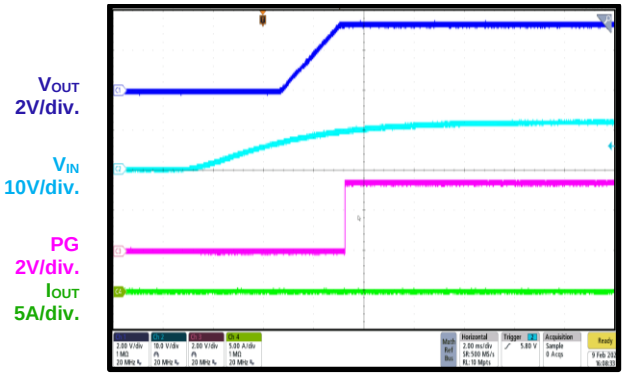
V_{IN} = 12V, V_{OUT} = 3.3V, f_{SW} = 1000kHz,
I_{OUT} = 0A to 2.5A, 2.5A/µs e-load, single channel



100µs/div.

Start-Up through VIN

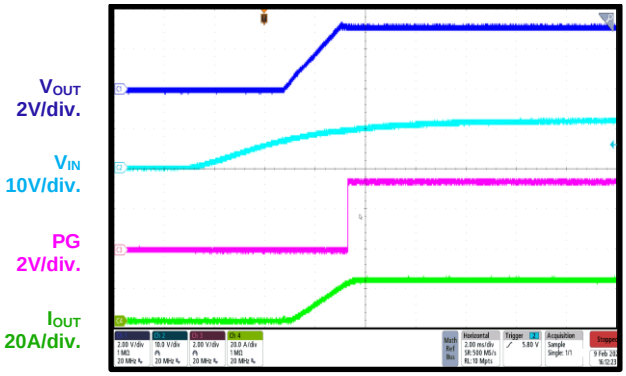
V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0A,
4-phase paralleled



2ms/div.

Start-Up through VIN

V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 20A,
4-phase paralleled



2ms/div.

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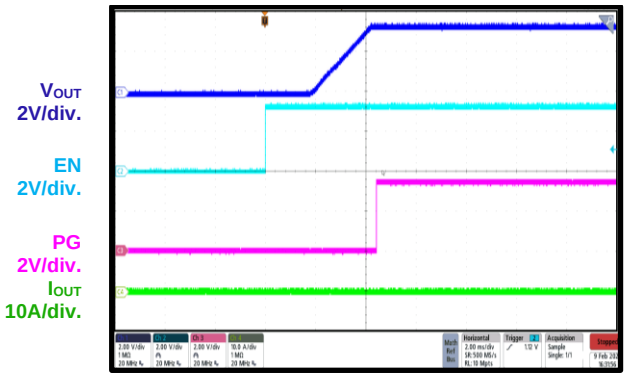
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance curves are tested on the evaluation board. V_{IN} = 12V, T_A = 25°C, unless otherwise noted.

Start-Up through EN

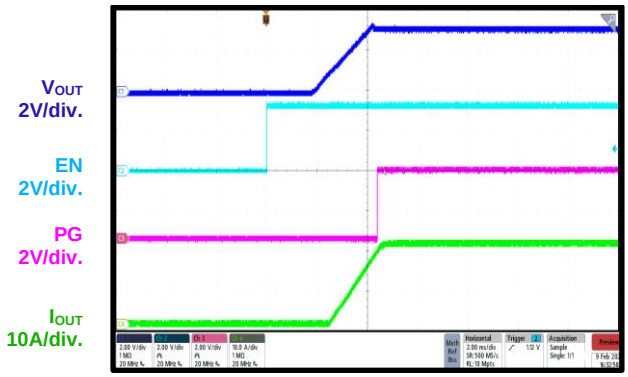
V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0A,
4-phase paralleled



2ms/div.

Start-Up through EN

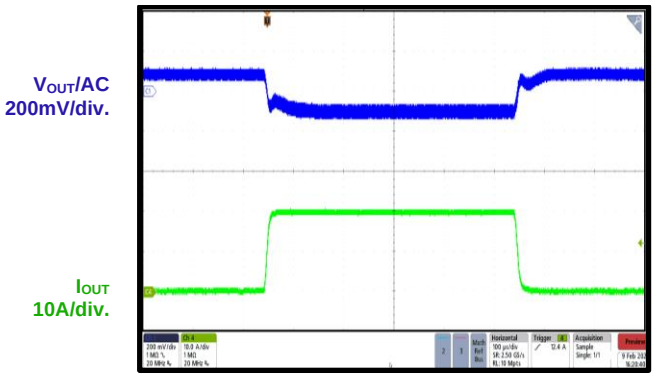
V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 20A,
4-phase paralleled



2ms/div.

Load Transient

V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0A to 20A,
2.5A/µs e-load, 4-phase paralleled



100µs/div.

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FUNCTIONAL BLOCK DIAGRAM

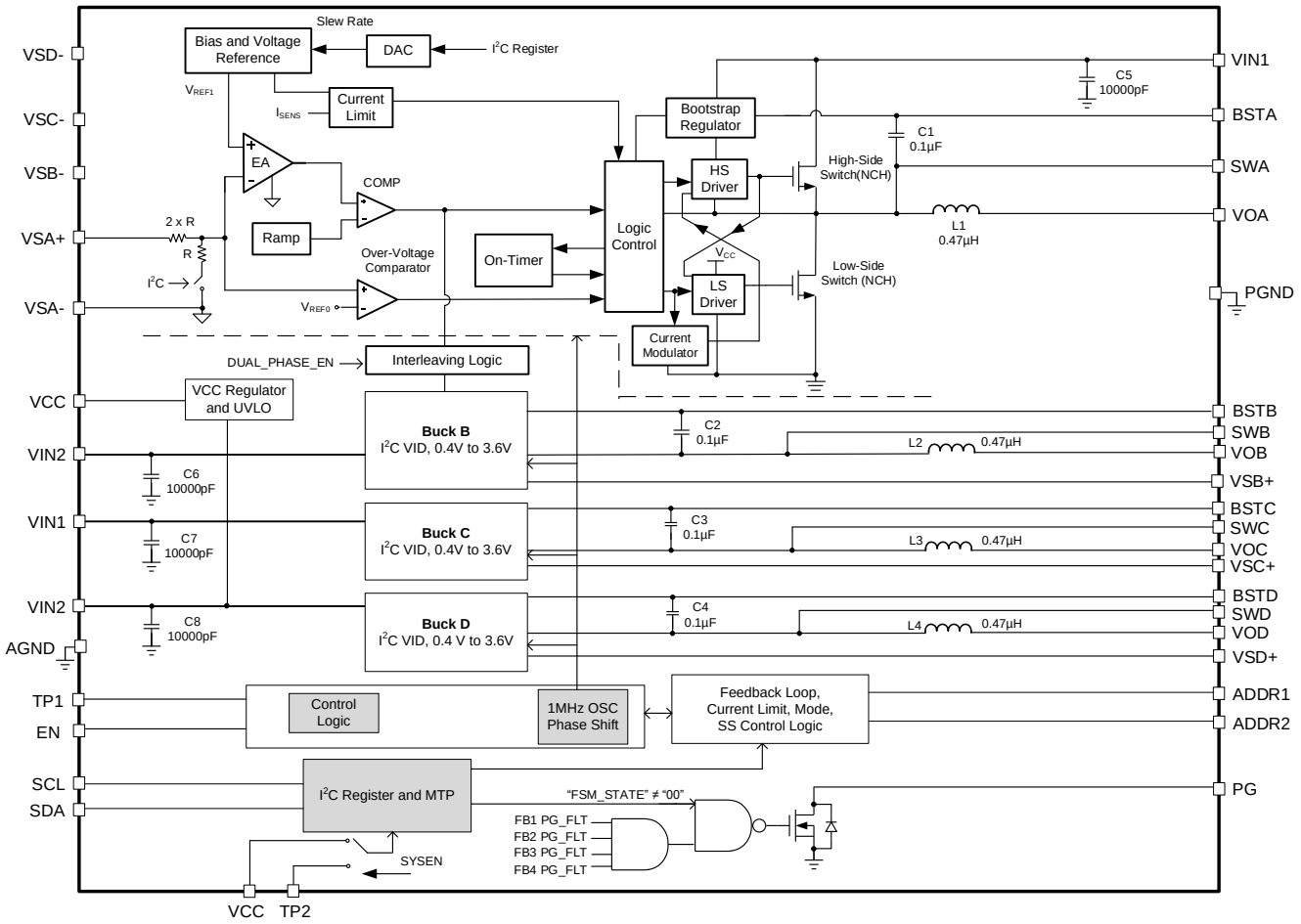

Figure 1: Functional Block Diagram

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OPERATION

The MPM54524 is a quad, synchronous, step-down DC/DC power module that offers built-in soft start (SS), compensation, and protections including over-voltage protection (OVP), under-voltage protection (UVP), and over-current protection (OCP). Fixed-frequency constant-on-time (COT) control provides fast transient response.

Power Supply Input and Under-Voltage Protection (UVP)

The input voltage (V_{INy}) (where y = 1 or 2) is the power module's power supply. If V_{INy} exceeds the UVP rising threshold and all the other start-up conditions are met, then the four-channel buck regulators start up. The bucks shut down once V_{INy} drops below the UVP falling threshold.

Internal VCC Supply

VCC is the internal driver and power supply of the control circuitries. A decoupling capacitor is required to stabilize the regulator and reduce ripple. This regulator takes the V_{INy} input (where y = 1 or 2) and operates across the full V_{INy} range. If V_{INy} exceeds 3.5V, the regulator's output is in full regulation. If V_{INy} drops below 3.5V, the regulator's output decreases according to the changes in V_{INy}.

Enable (EN)

If V_{INy} exceeds the under-voltage lockout (UVLO) threshold, pull the EN pin above 1.2V to enable the MPM54524. Float EN or pull the pin down to ground to disable the MPM54524. There is an internal 2.7MΩ resistor connected between EN and ground.

If EN is pulled high and reaches the V_{IN} UVLO threshold, BUCKX_CTRL_REG (0Ch), bits[7:4] can enable or disable the four channels after the power-on sequence is complete. If the power-on sequence set via 19h to 1Ch, bit[7] = 1'b0, then the outputs of the four channels are disabled by default. Once EN and VIN are ready, 0Ch can enable the four channels.

When the MPM54524 is disabled, the part goes into output discharge or soft shutdown mode if the two functions are enabled.

Power-On Sequence

Once the V_{INy} supply is valid and EN is pulled high, the MPM54524 initiates the power-on sequences of configuration 0, configuration 1, configuration 2, and configuration 3 via 19h to 1Fh to enable the corresponding output regulators in the specified sequence. Figure 2 on page 16 shows the power-on sequence. After V_{IN} reaches the UVLO threshold, EN goes high, and a 2ms system delay, each channel follows the start-up delay time, soft-start time (t_{SS_x}) (where x = A, B, C, or D), and PON_SEQ_DELAY0 time to execute the power-on sequence. Before enabling each channel, the MPM54524 loads the default voltage of each channel from the multiple-time programmable (MTP) memory registers.

t_{SS_x} for each channel can be configured via 13h.

Power-Off Sequence

If the EN pin is logic low or V_{INy} is below its UVLO threshold, the MPM54524 enters the power-off sequence set via 1Dh to 23h. Figure 3 on page 16 shows the power-off sequence. After each channel finishes its off delay, the MPM54524 turns off each channel sequentially with discharge or soft shutdown if the two functions are enabled. The discharge enable/disable function and discharge resistor can be configured via 0Eh. The soft shutdown enable/disable and t_{SS_x} can be configured via 11h, bits[7:4] and 12h, bits[7:0].

During the power-off sequence at falling UVLO, if rising UVLO is detected again, all the channels continue to execute the power-off sequence, then turn on sequentially based on the new power-on sequence.

Pre-Biased Start-Up

The MPM54524 is designed for monotonic start-up into pre-biased loads. If the output is pre-biased to a set voltage during start-up, the internal bootstrap (BST) voltage (V_{BST}) is refreshed and charged, and the voltage on the internal soft-start capacitor (C_{SS}) is charged as well. If V_{BST} exceeds its rising threshold, and the

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C_{SS} voltage exceeds the sensed output voltage (V_{OUTx}) (where x = A, B, C, or D) at the feedback pin (VSA+, VSB+, VSC+, or VSD+), then the part starts to work normally.

Power Good (PG)

The MPM54524 provides a power good (PG) output to indicate whether the enabled buck's V_{OUTx} is ready. The PG pin is an open-drain output. Connect PG to VCC or another voltage source via a pull up resistor (e.g. 10kΩ). PG is pulled high after the PON_SEQ_DELAY_PG bit, and all the channels finish soft start if they are enabled. During normal operation, PG is pulled low if any fault occurs.

Output Over-Voltage Protection (OVP)

The MPM54524 monitors V_{OUTx} and enters OVP latch-off mode once V_{OUTx} exceeds the output OVP rising threshold (V_{OVP1_H}). After triggering output OVP, all the channels turn off and PG is low. The MPM54524 does not automatically start up again until the OV fault is removed and recycling power on EN is initiated.

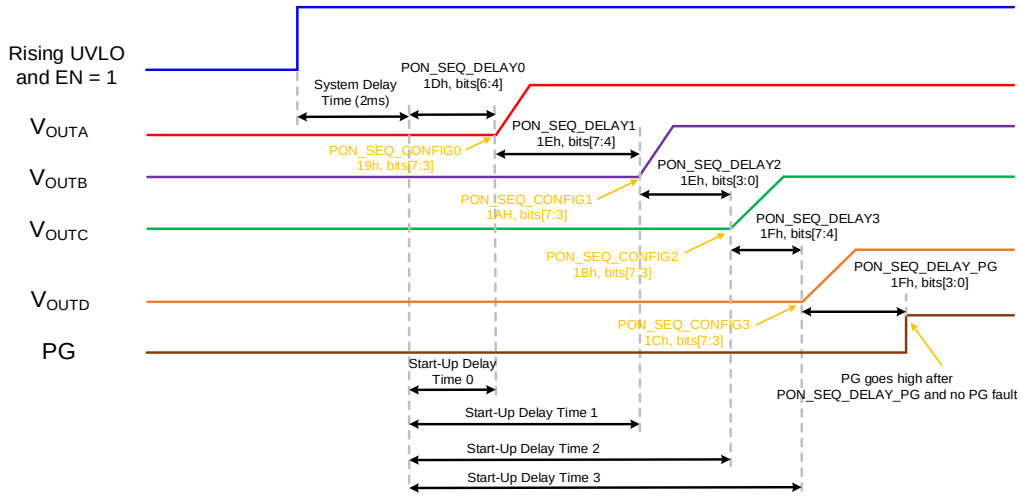

Figure 2: Power-On Sequence

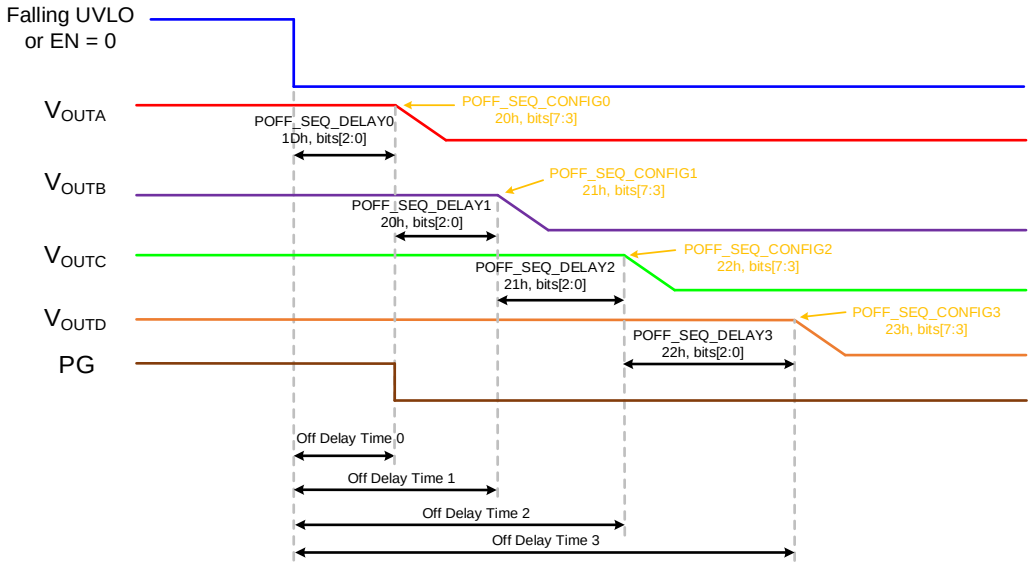

Figure 3: Power-Off Sequence

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V_{INy} Over-Voltage Protection (OVP)

If 90h, bit[0] = 1 and V_{INy} exceeds 15V for longer than 2µs, then the MPM54524 shuts down and VIN_OV_STATUS (00h, bit[1]) is set from 0 to 1. Even when the V_{INy} over-voltage (OV) fault is removed, the MPM54524 does not automatically start up until recycling power on EN is initiated. VIN_OV_STATUS remains set to 1 until power is recycled on EN, or the host clears the fault by writing the clear bit to 1 in 07h, bit[1].

Over-Current Protection (OCP) and Short-Circuit Protection (SCP)

The MPM54524 provides valley current limit control. When the low-side MOSFET (LS-FET) is on, the inductor current (I_L) is monitored. If the sensed I_L exceeds the valley current limit threshold, the device indicates an over-current (OC) fault via 2Ah. The high-side MOSFET (HS-FET) is not allowed to turn on until the valley current drops below the OC threshold. Meanwhile, V_{OUTx} drops until it is below the under-voltage (UV) threshold.

Once the UV and OC conditions are triggered, OCP latches off the device. This means the MPM54524 disables the output power stage and does not automatically turn on again until the UV and OC faults are removed, and recycling power on EN is initiated.

Output Discharge

To discharge the energy of the output capacitor (C_{OUT}) during the power-off sequence, there is a discharge path between the VOx pin and ground (where x = A, B, C, or D). The discharge function can be enabled via the MTP interface. The discharge resistor can also be changed via the MTP interface.

Soft Start (SS) and Soft Shutdown

The MPM54524 employs a soft start and soft shutdown mechanism to ensure smooth output during start-up and shutdown.

When the MPM54524 is enabled and V_{BST} reaches its rising threshold, the internal digital-to-analog converter (DAC) outputs a ramp voltage as the reference voltage (V_{REF}). V_{OUTx} smoothly ramps up with V_{REF}. Once the DAC output reaches the final voltage, it maintains a steady voltage. At this point, soft start finishes and enters steady-state operation.

When the MPM54524 is disabled, the internal DAC ramps down V_{REF}. V_{OUTx} follows the soft shutdown slew rate with V_{REF} until the output drops to 0.15V. Then soft shutdown stops, and the output is discharged via a 30Ω discharge resistor.

The start-up delay, shutdown delay, soft-start and soft shutdown slew rate can be configured via the MTP.

Out-of-Phase Operation

Figure 4 shows that buck regulator A (buck A), buck regulator B (buck B), buck regulator C (buck C), and buck regulator D (buck D) are frequency-locked with a fixed 90° phase shift, except for during interleaving mode.

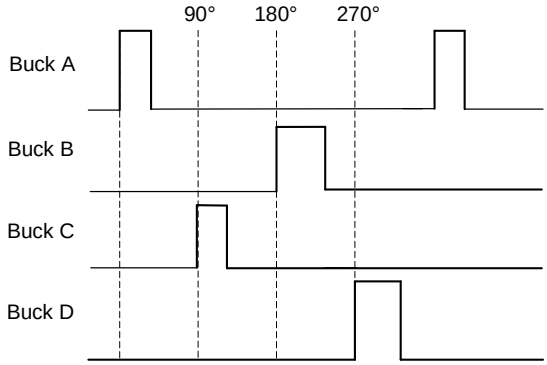

Figure 4: Phase Shift Functional Diagram

When buck A and buck B work in interleaving parallel mode, the phase shift between buck A and buck B changes to 180° (see Figure 5 on page 18). Buck C and buck D cannot work in interleaving mode, with the phase shift remaining at 90°.

Interleaving Mode for Buck A and Buck B

The MPM54524 supports 2-phase interleaving mode for buck A and buck B by setting 14h, bit[5] = 1. VSA+ must be connected to VSB+ in interleaving mode.

Figure 5 on page 18 shows the internal SET signal that is triggered when buck A or buck B's feedback (FB) signal is smaller than the internal REF signal. When the SET signal becomes high, only one phase's pulse-width modulation (PWM) output becomes high; the next time SET goes high, the next phase's PWM output goes high. This achieves automatic interleaving.

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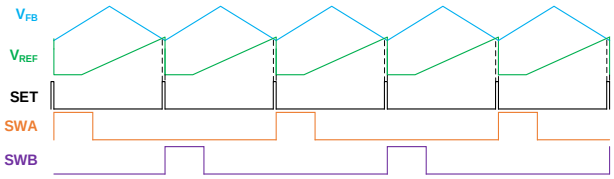

Figure 5: Dual-Phase Interleaving Mode

When buck A and buck B work in dual phase interleaving mode, the MPM54524 senses two-phase current and automatically tunes the buck's on time (t_{ON}) to achieve current balance actively.

Active Voltage Positioning (AVP)

The MPM54524 supports active voltage positioning (AVP) by setting the AVP_EN_X/X bit (where x = A/B or C/D) (71h, bit[7] and 79h, bit[7]) to 1 via the I²C. Once enabled, V_{OUTx} of the corresponding channel drops in proportion with the load current, which is determined using Equation (1) and Equation (2).

The droop voltage (V_{DROOP}) can be calculated with Equation (1):

$$V_{DROOP} = I_{OUT} \times R_{DROOP} \quad (1)$$

Where R_{DROOP} is the droop resistance with a typical value of about 40mΩ.

V_{OUTx} can be calculated with Equation (2):

$$V_{OUTx} = V_{REFx} - V_{DROOP} \quad (2)$$

Where V_{REFx} is the reference voltage of each channel.

The AVP functions enables on-demand parallel operation, where four outputs, three outputs, or two outputs can be connected in parallel in any combination without pre-setting any registers.

The current of the paralleled channels is inherently balanced by V_{DROOP}, which is generated by the AVP function.

Thermal Shutdown

The MPM54524 employs thermal shutdown by internally monitoring the junction temperature (T_J). If T_J exceeds the 145°C threshold, the MPM54524 shuts down based on the soft shutdown ramping down slew rate. This is a non-latch protection. There is a hysteresis of about 20°C. Once T_J drops to about 125°C, the MPM54524 initiates a soft start.

Analog-to-Digital Converter (ADC)

The MPM54524 supports the analog-to-digital converter (ADC) to monitor the regulator's V_{INy}, V_{OUTx}, output current (I_{OUTx}), and output power (P_{OUTx}) (where x = A, B, C, or D).

Multiple-Time Programmable (MTP) Configuration

After the MPM54524's V_{INy} starts up, the system-on-chip (SoC) configures the MPM54524's I²C register and MTP.

See the I²C Interface section on page 19 for more details on identifying a valid slave address. When the SoC writes to the I²C register, the I²C register takes effect immediately; it can also be burned into the MTP. During the buck's normal operation, the I²C master can read and write the register's data online.

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I²C INTERFACE

I²C Serial Interface

The I²C is a 2-wire, bidirectional, serial interface consisting of a data line (SDA) and a clock line (SCL). The lines are pulled to a bus voltage externally when they are idle. When connecting to the line, a master device generates the SCL signal and device address, then arranges the communication sequence. The MPM54524 interface is an I²C slave. The I²C interface adds flexibility to the power supply solution.

I²C Address Selection

Two ADDR pins are available to configure bit[0] to bit[3] of the I²C slave address according to Table 1, where bit[4] to bit[6] can be modified by writing to 73h, bit[1] to bit[3], respectively. Table 1 shows the I²C address setting via the ADDR1 and ADDR2 pins.

Table 1: I²C Address Setting via the ADDR1 and ADDR2 Pins

ADDR1	ADDR2	I²C Address
Low	Low	0XXX 1001 (12)
Low	Float	0XXX 1100 (12)
Low	High	0XXX 1110 (12)
Float	Low	0XXX 1010 (12)
Float	Float	0XXX 1000 (12)
Float	High	0XXX 1111 (12)
High	Low	0XXX 1011 (12)
High	Float	0XXX 1101 (12)
High	High	0XXX 0111 (12)

Note:

12) "XXX" refers to the portion of the address that can be configured by the customer.

Data Validity

One clock pulse is generated for each data bit transferred. The data on the SDA line must be stable during the clock's high period. The high or low state of the data line can only change when the clock signal on the SCL line is low (see Figure 6).

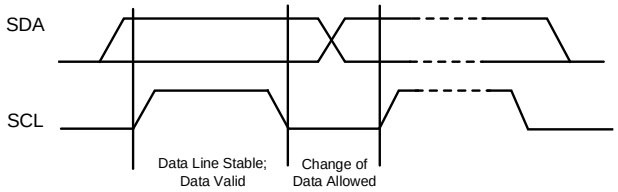

Figure 6: Bit Transfer on the I²C Bus

The start (S) and stop (P) commands are signaled by the master device, which signifies the beginning and the end of the I²C transfer. The start command is defined as the SDA signal transitioning from high to low while SCL is high. The stop command is defined as the SDA signal transitioning from low to high while SCL is high (see Figure 7).

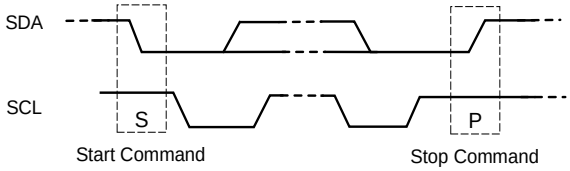

Figure 7: Start and Stop Commands

Start and stop commands are always generated by the master. The bus is busy after the start condition, and it is considered to be free again a minimum of 4.7µs after the stop command. The bus remains busy if a repeated start (Sr) is generated instead of a stop command. The start and repeated start conditions are functionally identical.

Transfer Data

Every byte put on the SDA line must be 8 bits long. Each byte must be followed by an acknowledge (ACK) bit. The acknowledge-related clock pulse is generated by the master. The transmitter releases the SDA line (high) during the acknowledge clock pulse. The receiver must pull down the SDA line during the acknowledge clock pulse so that it remains stable low during the clock pulse's high period.

Figure 8 on page 20 shows the data transfer format. After the start command, a slave address is sent. This address is 7 bits, followed by an 8th data direction bit (R/W). A 0 indicates a transmission (write), and a 1 indicates a request for data (read). A data transfer is always terminated by a stop command, which is generated by the master. If the master still wants to communicate on the bus, it can generate a repeated start command and address another slave without first generating a stop command.

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The MPM54524 requires a start command, a valid I²C address, register address byte, and data byte for a single data update. After receiving each byte, the MPM54524 acknowledges by pulling the SDA line low during a single clock pulse's high period. A valid I²C address selects the MPM54524. The MPM54524 performs an update on the LSB byte's falling edge.

Figure 9 shows an example of writing to a single register. Figure 10 shows an example of reading to a single register.

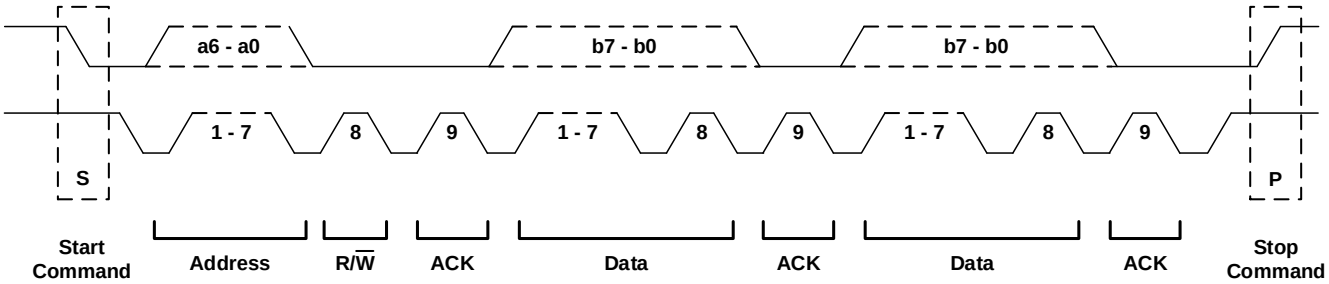

Figure 8: Complete Data Transfer

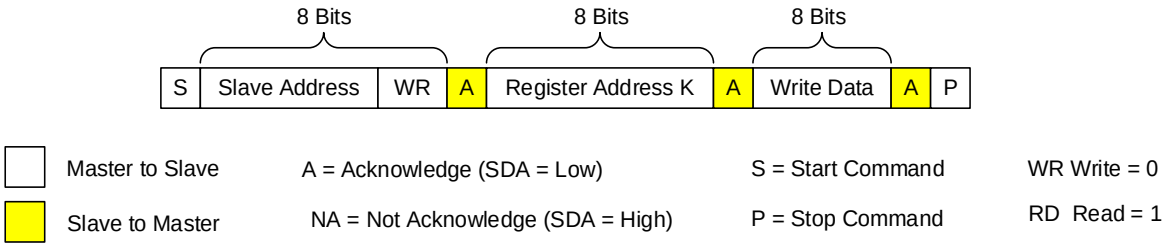

Figure 9: I²C Write Single Register Example

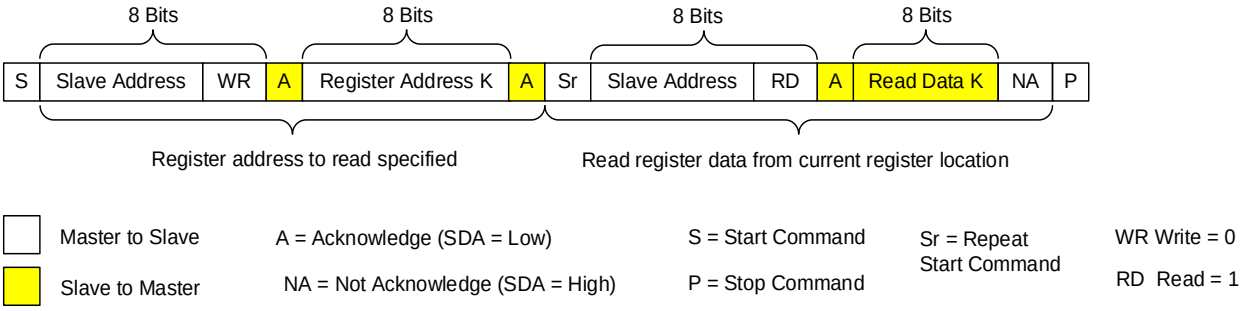

Figure 10: I²C Read Single Register Example

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SUPPORTED PMBUS COMMANDS

Command Code	Command Name	Type	Bytes
00h	STATUS_0	R	1
01h	STATUS_1	R	1
02h	BUCKA_CURRENT/PWR_METER	R	1
03h	BUCKB_CURRENT/PWR_METER	R	1
04h	BUCKC_CURRENT/PWR_METER	R	1
05h	BUCKD_CURRENT/PWR_METER	R	1
06h	BUCKX_VOLTAGE	R	1
07h	CLEAR_0	Send	1
08h	CLEAR_1	Send	1
09h	MASK_0	R/W	1
0Ah	MASK_1	R/W	1
0Bh	REMOTE_REG	R/W	1
0Ch	BUCKX_CTRL_REG	R/W	1
0Dh	PG_REG	R/W	1
0Eh	DISCHARGE_R_REG	R/W	1
0Fh	SW_FREQ_REG	R/W	1
10h	MONITOR_EN_REG	R/W	1
11h	SOFT_STOP_EN_REG	R/W	1
12h	SOFT_STOP_REG	R/W	1
13h	SOFT_START_REG	R/W	1
14h	PROTECT_REG	R/W	1
15h	BUCKA_VOUT	R/W	1
16h	BUCKB_VOUT	R/W	1
17h	BUCKC_VOUT	R/W	1
18h	BUCKD_VOUT	R/W	1
19h	PON_CONFIG_0	R/W	1
1Ah	PON_CONFIG_1	R/W	1
1Bh	PON_CONFIG_2	R/W	1
1Ch	PON_CONFIG_3	R/W	1
1Dh	PON_OFF_DELAY0	R/W	1
1Eh	PON_SEQ_DELAY_1_2	R/W	1
1Fh	PON_SEQ_DELAY_3_PG	R/W	1
20h	POFF_SEQ_CONFIG_0	R/W	1
21h	POFF_SEQ_CONFIG_1	R/W	1
22h	POFF_SEQ_CONFIG_2	R/W	1
23h	POFF_SEQ_CONFIG_3	R/W	1
24h	ADC_TEMP	R	1
25h	VOUT_RANGE_SELECT	R/W	1
26h	CLP_BUCKX	R/W	1
2Ah	OC_STATUS_CLEAR	R/W	1
30h	MTP_AUTO_REG	R/W	1

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SUPPORTED PMBUS COMMANDS *(continued)*

Command Code	Command Name	Type	Bytes
31h	PART_ID	R	1
35h	CODE_ID	R	1
36h	CODE_VERSION	R	1
71h	ACTIVE_POSITION_ENABLE_A/B	R/W	1
73h	I2C_ADDRESS	R/W	1
79h	ACTIVE_POSITION_ENABLE_C/D	R/W	1
90h	VIN_OV_REG	R/W	1
AFh	VIN_UVLO_REG	R/W	1

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REGISTER MAP

Status Registers

The status registers are updated to 1 if an event occurs, and they remain at 1 until the clear command is generated by the host, even if the failing condition is no longer present. In addition, when the input voltage (V_{INy}) (where y = 1 or 2) drops below its under-voltage lockout (UVLO) threshold, the status register is initialized to 0. The PWR_GOOD interrupt may be generated by the MPM54524 at the same time, depending on the type of event. The interrupts are only generated if they are not masked.

All read-only (RO) registers are one-time latched registers, meaning that once the MPM54524 sets the register flag, the host must explicitly clear the register. The MPM54524 does not automatically update the registers even if the event that triggered the status is no longer present.

STATUS_0 (00h)

Format: Unsigned binary

The STATUS_0 command monitors statuses including over-temperature (OT), buck output power not good, and V_{INy} over-voltage (OV).

Bits	Access	Bit Name	Default	Description
7	R	RESERVED	N/A	Reserved.
6	R	OVER_TEMP_ STATUS	1'b0	1'b0: No critical temperature shutdown occurs 1'b1: A critical temperature shutdown occurs
5	R	BUCKA_POWER_ NOT_GOOD_STATUS	1'b0	1'b0: The buck regulator A (buck A)'s output is power good 1'b1: Buck A's output is power not good
4	R	BUCKB_POWER_ NOT_GOOD_STATUS	1'b0	1'b0: The buck regulator B (buck B)'s output is power good 1'b1: Buck B's output is power not good
3	R	BUCKC_POWER_ NOT_GOOD_STATUS	1'b0	1'b0: The buck regulator C (buck C)'s output is power good 1'b1: Buck C's output is power not good
2	R	BUCKD_POWER_ NOT_GOOD_STATUS	1'b0	1'b0: The buck regulator D (buck D)'s output is power good 1'b1: Buck D's output is power not good
1	R	VIN_OV_STATUS	1'b0	1'b0: No V_{IN} OV fault occurs 1'b1: A V_{IN} OV fault occurs
0	R	RESERVED	N/A	Reserved.

STATUS_1 (01h)

Format: Unsigned binary

The STATUS_1 command monitors buck x output's OV and under-voltage (UV) status (where x = A, B, C, or D).

Bits	Access	Bit Name	Default	Description
7	R	BUCKA_OV_STATUS	1'b0	1'b0: Buck A's output indicates no OV fault 1'b1: Buck A's output indicates an OV fault
6	R	BUCKB_OV_STATUS	1'b0	1'b0: Buck B's output indicates no OV fault 1'b1: Buck B's output indicates an OV fault
5	R	BUCKC_OV_STATUS	1'b0	1'b0: Buck C's output indicates no OV fault 1'b1: Buck C's output indicates an OV fault
4	R	BUCKD_OV_STATUS	1'b0	1'b0: Buck D's output indicates no OV fault 1'b1: Buck D's output indicates an OV fault
3	R	BUCKA_UV_STATUS	1'b0	1'b0: Buck A's output indicates no UV fault 1'b1: Buck A's output indicates an UV fault

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2	R	BUCKB_UV_STATUS	1'b0	1'b0: Buck B's output indicates no UV fault 1'b1: Buck B's output indicates an UV fault
1	R	BUCKC_UV_STATUS	1'b0	1'b0: Buck C's output indicates no UV fault 1'b1: Buck C's output indicates an UV fault
0	R	BUCKD_UV_STATUS	1'b0	1'b0: Buck D's output indicates no UV fault 1'b1: Buck D's output indicates an UV fault

BUCKA_CURRENT/PWR_METER (02h)

Format: Direct

The BUCKA_CURRENT/PWR_METER command monitors buck A's output current (I_{OUTA}) and output power (P_{OUTA}).

Bits	Access	Bit Name	Description
7:0	R	BUCKA_ADC_ CURRENT/POWER	If 10h, bit[3] = 0, this measures buck A's I_{OUTA} or P_{OUTA}. The I_{OUTA} analog-to-digital converter (ADC) report values are listed below: 8'b 0000 0000: Reserved 8'b 0000 0001: 0.125A or 125mW 8'b 0000 0010: 0.25A or 250mW 8'b 0000 0011: 0.375A or 375mW …… 8'b 0011 1100 = 7.5A or 7500mW 8'b 0011 1101 = 7.625A or 7625mW 8'b 0011 1110 = 7.75A or 7750mW 8'b 0011 1111 ≥ 7.875A or 7875mW If 10h, bit[3] = 1, this indicates the sum of P_{OUTA}, buck B's output power (P_{OUTB}), buck C's output power (P_{OUTC}), and buck D's output power (P_{OUTD}). 8'b 0000 0000: Reserved 8'b 0000 0001: 125mW 8'b 0000 0010: 250mW 8'b 0000 0011: 375mW …… 8'b 1111 1100 = 31500mW 8'b 1111 1101 = 31625mW 8'b 1111 1110 = 31750mW 8'b 1111 1111 ≥ 31875mW

BUCKB_CURRENT/PWR_METER (03h)

Format: Direct

The BUCKB_CURRENT/PWR_METER command monitors buck B's output current (I_{OUTB}) and P_{OUTB}.

Bits	Access	Bit Name	Description
7:0	R	BUCKB_ADC_ CURRENT/POWER	The I_{OUTB} or P_{OUTB} ADC report values are listed below: 8'b 0000 0000: Reserved 8'b 0000 0001: 0.125A or 125mW 8'b 0000 0010: 0.25A or 250mW 8'b 0000 0011: 0.375A or 375mW …… 8'b 0011 1100 = 7.5A or 7500mW 8'b 0011 1101 = 7.625A or 7625mW 8'b 0011 1110 = 7.75A or 7750mW 8'b 0011 1111 ≥ 7.875A or 7875mW

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BUCKC_CURRENT/PWR_METER (04h)

Format: Direct

The BUCKC_CURRENT/PWR_METER command monitors buck C's output current (I_{OUTC}) and P_{OUTC}.

Bits	Access	Bit Name	Description
7:0	R	BUCKC_ADC_ CURRENT/POWER	The I_{OUTC} or P_{OUTC} ADC report values are listed below: 8'b 0000 0000: Reserved 8'b 0000 0001: 0.125A or 125mW 8'b 0000 0010: 0.25A or 250mW 8'b 0000 0011: 0.375A or 375mW …… 8'b 0011 1100 = 7.5A or 7500mW 8'b 0011 1101 = 7.625A or 7625mW 8'b 0011 1110 = 7.75A or 7750mW 8'b 0011 1111 ≥ 7.875A or 7875mW

BUCKD_CURRENT/PWR_METER (05h)

Format: Direct

The BUCKD_CURRENT/PWR_METER command monitors buck D's output current (I_{OUTD}) and P_{OUTD}.

Bits	Access	Bit Name	Description
7:0	R	BUCKD_ADC_ CURRENT/POWER	The I_{OUTD} or P_{OUTD} ADC report values are listed below: 8'b 0000 0000: Reserved 8'b 0000 0001: 0.125A or 125mW 8'b 0000 0010: 0.25A or 250mW 8'b 0000 0011: 0.375A or 375mW …… 8'b 0011 1100 = 7.5A or 7500mW 8'b 0011 1101 = 7.625A or 7625mW 8'b 0011 1110 = 7.75A or 7750mW 8'b 0011 1111 ≥ 7.875A or 7875mW

BUCKX_VOLTAGE (06h)

Format: Direct

The BUCKX VOLTAGE command monitors V_{OUTx}.

Bits	Access	Bit Name	Description
7:0	R	BUCKX_ADC_ VOLTAGE	Changes V_{OUTx} based on 10h, bits[6:[5]. 8'b 0000 0000 = Undefined 8'b 0000 0001 = 15mV 8'b 0000 0010 = 30mV …… 8'b 1111 1111 ≥ 3825mV

Clear Registers

For each real-time status register (00h and 01h), the MPM54524 offers a way to clear the status of events. All clear registers are write-1-to-clear (W1C) registers. If 1 is written to any of the clear registers, the MPM54524 updates the status registers to the default state and removes the interrupt condition on the PWR_GOOD output signal, assuming that the event is no longer present. If the failing condition is still present, the status register remains at 1. Note that the PWR_GOOD interrupt is only applicable if the event is not masked.

The MPM54524 offers a global clear command by writing 1 to 07h, bit[0]. This command works the same way as the individual clear command. This command can be used by the host if more than one clear command is required to different registers.

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CLEAR_0 (07h)

Format: Unsigned binary

The CLEAR_0 command clears the buck's output power not good and V_{INy} over-voltage protection (OVP) status, in addition to providing a global clear.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	N/A	Reserved.
5	R/W	CLEAR_BUCKA_ POWER_NOT_GOOD_ STATUS	1'b0	1'b1: Clears the status of 00h, bit[5]
4	R/W	CLEAR_BUCKB_ POWER_NOT_GOOD_ STATUS	1'b0	1'b1: Clears the status of 00h, bit[4]
3	R/W	CLEAR_BUCKC_ POWER_NOT_GOOD_ STATUS	1'b0	1'b1: Clears the status of 00h, bit[3]
2	R/W	CLEAR_BUCKD_ POWER_NOT_GOOD_ STATUS	1'b0	1'b1: Clears the status of 00h, bit[2]
1	R/W	CLEAR_VIN_OVP_ STATUS	1'b0	1'b1: Clears the status of 00h, bit[1]
0	R/W	CLEAR_GLOBAL	1'b0	1'b1: Clears all the statuses of 00h and 01h

CLEAR_1 (08h)

Format: Unsigned binary

The CLEAR_1 command clears the buck x's OV and UV status (where x = A, B, C, or D).

Bits	Access	Bit Name	Default	Description
7	R/W	CLEAR_BUCKA_OV_ STATUS	1'b0	1'b1: Clears the status of 01h, bit[7]
6	R/W	CLEAR_BUCKB_OV_ STATUS	1'b0	1'b1: Clears the status of 01h, bit[6]
5	R/W	CLEAR_BUCKC_OV_ STATUS	1'b0	1'b1: Clears the status of 01h, bit[5]
5	R/W	CLEAR_BUCKD_OV_ STATUS	1'b0	1'b1: Clears the status of 01h, bit[4]
3	R/W	CLEAR_BUCKA_UV_ STATUS	1'b0	1'b1: Clears the status of 01h, bit[3]
2	R/W	CLEAR_BUCKB_UV_ STATUS	1'b0	1'b1: Clears the status of 01h, bit[2]
1	R/W	CLEAR_BUCKC_UV_ STATUS	1'b0	1'b1: Clears the status of 01h, bit[1]
0	R/W	CLEAR_BUCKD_UV_ STATUS	1'b0	1'b1: Clears the status of 01h, bit[0]

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Mask Registers

For each real-time status register, the MPM54524 offers a way to mask the status of events.

MASK_0 (09h)

Format: Unsigned binary

The MASK_0 command masks buck x's output power not good and the V_{INy} OVP status.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	N/A	Reserved.
5	R/W	MASK_BUCKA_ POWER_NOT_GOOD_ STATUS	1'b0	1'b1: Masks the status of 00h, bit[5]
4	R/W	MASK_BUCKB_ POWER_NOT_GOOD_ STATUS	1'b0	1'b1: Masks the status of 00h, bit[4]
3	R/W	MASK_BUCKC_ POWER_NOT_GOOD_ STATUS	1'b0	1'b1: Masks the status of 00h, bit[3]
2	R/W	MASK_BUCKD_ POWER_NOT_GOOD_ STATUS	1'b0	1'b1: Masks the status of 00h, bit[2]
1	R/W	MASK_VIN_OVP_ STATUS	1'b0	1'b1: Masks the status of 00h, bit[1]
0	R	RESERVED	N/A	Reserved.

MASK_1 (0Ah)

Format: Unsigned binary

The MASK_1 command masks buck x's output OV and over-current (OC) status.

Bits	Access	Bit Name	Default	Description
7	R/W	MASK_BUCKA_OV_ STATUS	1'b0	1'b1: Masks the status of 01h, bit[7]
6	R/W	MASK_BUCKB_OV_ STATUS	1'b0	1'b1: Masks the status of 01h, bit[6]
5	R/W	MASK_BUCKC_OV_ STATUS	1'b0	1'b1: Masks the status of 01h, bit[5]
4	R/W	MASK_BUCKD_OV_ STATUS	1'b0	1'b1: Masks the status of 01h, bit[4]
3	R/W	MASK_BUCKA_OC_ STATUS	1'b0	1'b1: Masks the status of 01h, bit[3]
2	R/W	MASK_BUCKB_OC_ STATUS	1'b0	1'b1: Masks the status of 01h, bit[2]
1	R/W	MASK_BUCKC_OC_ STATUS	1'b0	1'b1: Masks the status of 01h, bit[1]
0	R	MASK_BUCKD_OC_ STATUS	1'b0	1'b1: Masks the status of 01h, bit[0]

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Threshold and Configuration Registers

REMOTE_REG (0Bh)

Format: Unsigned binary

The REMOTE_REG command sets buck x's remote sensing.

Bits	Access	Bit Name	Default	Description
7	R/W	BUCKA_REMOTE_EN	1'b0	Selects buck A's remote sensing. 1'b0: Disables remote sensing 1'b1: Enables remote sensing
6	R/W	BUCKB_REMOTE_EN	1'b0	Selects buck's B remote sensing. 1'b0: Disables remote sensing 1'b1: Enables remote sensing
5	R/W	BUCKC_REMOTE_EN	1'b0	Selects buck C's remote sensing. 1'b0: Disables remote sensing 1'b1: Enables remote sensing
4:0	R	RESERVED	N/A	Reserved.

BUCKX_CTRL_REG (0Ch)

Format: Unsigned binary

The BUCKx_CTRL_REG command sets buck x's output regulator in pulse-frequency modulation (PFM) or pulse-width modulation (PWM) mode.

Bits	Access	Bit Name	Default	Description
7	R/W	BUCKA_EN	1'b1	Enables buck A's output regulator. 1'b 0: Disabled 1'b 1: Enabled
6	R/W	BUCKB_EN	1'b1	Enables buck B's output regulator. 1'b0: Disabled 1'b1: Enabled
5	R/W	BUCKC_EN	1'b1	Enables buck C's output regulator. 1'b0: Disabled 1'b1: Enabled
4	R/W	BUCKD_EN	1'b1	Enables buck D's output regulator. 1'b0: Disabled 1'b1: Enabled
3	R/W	PWM_BUCKA	1'b0	Sets buck A's automatic mode or forced PWM mode. 1'b0: Forced PWM 1'b1: Automatic mode
2	R/W	PWM_BUCKB	1'b0	Sets buck B's automatic mode or forced PWM mode. 1'b0: Forced PWM 1'b1: Automatic mode
1	R/W	PWM_BUCKC	1'b0	Sets buck C's automatic mode or forced PWM mode. 1'b0: Forced PWM 1'b1: Automatic mode

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0	R/W	PWM_BUCKD	1'b0	Sets buck D's automatic mode or forced PWM mode. 1'b0: Forced PWM 1'b1: Automatic mode

PG_REG (0Dh)

Format: Unsigned binary

The PG_REG command sets buck x's power good (PG) threshold.

Bits	Access	Bit Name	Default	Description
7	R	RESERVED	N/A	Reserved.
6	R	RESERVED	N/A	Reserved.
5	R	RESERVED	N/A	Reserved.
4	R	RESERVED	N/A	Reserved.
3	R/W	PG_%_BUCKA	1'b0	Sets the PG threshold for buck A. 1'b0 = 5% 1'b1 = 7%
2	R/W	PG_%_BUCKB	1'b0	Sets the PG threshold for buck B. 1'b0 = 5% 1'b1 = 7%
1	R/W	PG_%_BUCKC	1'b0	Sets the PG threshold for buck C. 1'b0 = 5% 1'b1 = 7%
0	R/W	PG_%_BUCKD	1'b0	Sets the PG threshold for buck D 1'b0 = 5% 1'b1 = 7%

DISCHARGE_R_REG (0Eh)

Format: Unsigned binary

The DISCHARGE_R_REG command sets buck x's automatic discharge mode and discharge resistance.

Bits	Access	Bit Name	Default	Description
7	R/W	AUTODIS_1	1'b1	Sets the automatic discharge mode for buck A. 1'b 0: No discharge 1'b 1: Discharges
6	R/W	AUTODIS_2	1'b1	Sets the automatic discharge mode for buck B. 1'b 0: No discharge 1'b 1: Discharges
5	R/W	AUTODIS_3	1'b1	Sets the automatic discharge mode for buck C. 1'b 0: No discharge 1'b 1: Discharges
4	R/W	AUTODIS_4	1'b1	Sets the automatic discharge mode for buck D. 1'b 0: No discharge 1'b 1: Discharges
3	R/W	DIS_R_1	1'b1	Sets the discharge resistance for buck A. 1'b0: 10Ω 1'b1: 2Ω

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2	R/W	DIS_R_2	1'b1	Sets the discharge resistance for buck B. 1'b0: 10Ω 1'b1: 2Ω
1	R/W	DIS_R_3	1'b1	Sets the discharge resistance for buck C. 1'b0: 10Ω 1'b1: 2Ω
0	R/W	DIS_R_4	1'b1	Sets the discharge resistance for buck D. 1'b0: 10Ω 1'b1: 2Ω

SW_FREQ_REG (0Fh)

Format: Unsigned binary

The SW_FREQ_REG command sets buck x's switching frequency (f_{SW}).

Bits	Access	Bit Name	Default	Description
7:6	R/W	BUCKA_OUTPUT_REGULATOR_SWITCHING_FREQUENCY	2'b10	Sets buck A's output regulator f_{SW}. 2'b00: 500kHz 2'b01: 750kHz 2'b10: 1000kHz 2'b11: 1250kHz
5:4	R/W	BUCKB_OUTPUT_REGULATOR_SWITCHING_FREQUENCY	2'b10	Sets buck B's output regulator f_{SW}. 2'b00: 500kHz 2'b01: 750kHz 2'b10: 1000kHz 2'b11: 1250kHz
3:2	R/W	BUCKC_OUTPUT_REGULATOR_SWITCHING_FREQUENCY	2'b10	Sets buck C's output regulator f_{SW}. 2'b00: 500kHz 2'b01: 750kHz 2'b10: 1000kHz 2'b11: 1250kHz
1:0	R/W	BUCKD_OUTPUT_REGULATOR_SWITCHING_FREQUENCY	2'b10	Sets buck D's output regulator f_{SW}. 2'b00: 500kHz 2'b01: 750kHz 2'b10: 1000kHz 2'b11: 1250kHz

MONITOR_EN_REG (10h)

Format: Unsigned binary

The MONITOR_EN_REG command enables V_{OUTx} and I_{OUTx} monitoring.

Bits	Access	Bit Name	Default	Description
7	R/W	MON_V_EN	1'b1	Enables V_{OUTx} monitoring. 1'b0: Disabled 1'b1: Enabled
6:5	R/W	MON_V_SEL	2'b00	Selects V_{OUTx} monitoring. 2'b00: Buck A 2'b01: Buck B 2'b10: Buck C 2'b11: Buck D

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4	R/W	MON_IP_SEL	1'b0	Selects I_{OUTx} or the power. 1'b0: Buck x's I_{OUTx} 1'b1: Buck x's power
3	R/W	MON_TP_SEL	1'b0	Selects buck A's power or the total power. 1'b0: Buck A's I_{OUT} or power 1'b1: Total power
2	R/W	MON_I_EN	1'b1	Enables I_{OUTx} monitoring. 1'b0: Disabled 1'b1: Enabled
1	R	RESERVED	N/A	Reserved.
0	R	RESERVED	N/A	Reserved.

SOFT_STOP_EN_REG (11h)

Format: Unsigned binary

The SOFT_STOP_EN_REG command enables buck x's soft shutdown.

Bits	Access	Bit Name	Default	Description
7	R/W	SOFT_STOP_BUCKA	1'b0	Enables soft shutdown for buck A. 1'b0: Disabled 1'b1: Enabled
6	R/W	SOFT_STOP_BUCKB	1'b0	Enables soft shutdown for buck B. 1'b0: Disabled 1'b1: Enabled
5	R/W	SOFT_STOP_BUCKC	1'b0	Enables soft shutdown for buck C. 1'b0: Disabled 1'b1: Enabled
4	R/W	SOFT_STOP_BUCKD	1'b0	Enables soft shutdown for buck D. 1'b0: Disabled 1'b1: Enabled
3:0	R	RESERVED	N/A	Reserved.

SOFT_STOP_REG (12h)

Format: Unsigned binary

The SOFT_STOP_REG command sets buck x's soft shutdown time.

Bits	Access	Bit Name	Default	Description
7:6	R/W	SOFT_STOP_TIME_ BUCKA	2'b00	Sets buck A's soft shutdown time. 2'b00: 0.5ms 2'b01: 1ms 2'b10: 2ms 2'b11: 4ms
5:4	R/W	SOFT_STOP_TIME_ BUCKB	2'b00	Sets buck B's soft shutdown time. 2'b00: 0.5ms 2'b01: 1ms 2'b10: 2ms 2'b11: 4ms

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3:2	R/W	SOFT_STOP_TIME_ BUCKC	2'b00	Sets buck C's soft shutdown time. 2'b00: 0.5ms 2'b01: 1ms 2'b10: 2ms 2'b11: 4ms
1:0	R/W	SOFT_STOP_TIME_ BUCKD	2'b00	Sets buck D's soft shutdown time. 2'b00: 0.5ms 2'b01: 1ms 2'b10: 2ms 2'b11: 4ms

SOFT_START_REG (13h)

Format: Unsigned binary

The SOFT_START_REG command sets buck x's soft-start time (t_{SS_x}).

Bits	Access	Bit Name	Default	Description
7:6	R/W	SOFT_START_TIME_ BUCKA	2'b11	Sets buck A's soft-start time (t_{SS_A}). 2'b00: 0.5ms 2'b01: 1ms 2'b10: 1.5ms 2'b11: 2ms
5:4	R/W	SOFT_START_TIME_ BUCKB	2'b11	Sets buck B's soft-start time (t_{SS_B}). 2'b00: 0.5ms 2'b01: 1ms 2'b10: 1.5ms 2'b11: 2ms
3:2	R/W	SOFT_START_TIME_ BUCKC	2'b11	Sets buck C's soft-start time (t_{SS_C}). 2'b00: 0.5ms 2'b01: 1ms 2'b10: 1.5ms 2'b11: 2ms
1:0	R/W	SOFT_START_TIME_ BUCKD	2'b11	Sets buck D's soft-start time (t_{SS_D}). 2'b00: 0.5ms 2'b01: 1ms 2'b10: 1.5ms 2'b11: 2ms

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PROTECT_REG (14h)

Format: Unsigned binary

The PROTECT_REG command sets the protection functions and phase regulator mode for buck A or buck B.

Bits	Access	Bit Name	Default	Description
7	R	RESERVED	N/A	Reserved.
6	R/W	MTP_W	1'b0	Sets the multiple-time programmable (MTP) memory write. 1'b0: Disabled 1'b1: Enabled
5	R/W	BUCKA/B_DUAL_EN	1'b0	Selects phase regulator mode for buck A and buck B. 1'b0: Single-phase regulator 1'b1: Dual-phase regulator
4:0	R	RESERVED	N/A	Reserved.

BUCKA_VOUT (15h)

Format: Direct

The BUCKA_VOUT command sets buck A's output voltage (V_{OUTA}).

Bits	Access	Bit Name	Default	Description
7:0	R/W	BUCKA_VOUT_ SETTING	0x8F	Sets V_{OUTA}. Note that the V_{OUTA} change slew rate is 1mV/µs. If 25h, bit[3] = 0, then buck A outputs a dynamic voltage scaling (DVS) range between 0.4V and 1.2V. 0x00: 0.4V 0x01: 0.41V 0x02: 0.42V 0x03: 0.43V …… 0x4D: 1.17V 0x4E: 1.18V 0x4F: 1.19V 0x50: 1.2V Others are reserved (0x51 to 0xFF) If 25h, bit[3] = 1, then buck A outputs a DVS range between 1.2V and 3.6V. 0x00: 1.2V 0x01: 1.215V 0x02: 1.23V 0x03: 1.245V …… 0x8C: 3.3V 0x8D: 3.315V 0x8E: 3.33V …… 0x9F: 3.585V 0xA0: 3.6V Others are reserved (0xA1 to 0xFF)

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BUCKB_VOUT (16h)

Format: Direct

The BUCKB_VOUT command sets buck B's output voltage (V_{OUTB}).

Bits	Access	Bit Name	Default	Description
7:0	R/W	BUCKB_VOUT_ SETTING	0x8F	Sets V_{OUTB}. Note that the V_{OUTB} change slew rate is 1mV/µs. If 25h, bit[2] = 0, then buck B outputs a DVS range between 0.4V and 1.2V. 0x00: 0.4V 0x01: 0.41V 0x02: 0.42V 0x03: 0.43V …… 0x4D: 1.17V 0x4E: 1.18V 0x4F: 1.19V 0x50: 1.2V Others are reserved (0x51 to 0xFF) If 25h, bit[2] = 1, then buck B outputs a DVS range between 1.2V and 3.6V. 0x00: 1.2V 0x01: 1.215V 0x02: 1.23V 0x03: 1.245V …… 0x8C: 3.3V 0x8D: 3.315V 0x8E: 3.33V …… 0x9F: 3.585V 0xA0: 3.6V Others are reserved (0xA1 to 0xFF)

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BUCKC_VOUT (17h)

Format: Direct

The BUCKC_VOUT command sets buck C's output voltage (V_{OUTC}).

Bits	Access	Bit Name	Default	Description
7:0	R/W	BUCKC_VOUT_ SETTING	0x8F	Sets V_{OUTC}. Note that the V_{OUTC} change slew rate is 1mV/µs. If 25h, bit[1] = 0, then buck C outputs a DVS range between 0.4V and 1.2V. 0x00: 0.4V 0x01: 0.41V 0x02: 0.42V 0x03: 0.43V …… 0x4D: 1.17V 0x4E: 1.18V 0x4F: 1.19V 0x50: 1.2V Others are reserved (0x51 to 0xFF) If 25h, bit[1] = 1, then buck C outputs a DVS range between 1.2V and 3.6V. 0x00: 1.2V 0x01: 1.215V 0x02: 1.23V 0x03: 1.245V …… 0x8C: 3.3V 0x8D: 3.315V 0x8E: 3.33V …… 0x9F: 3.585V 0xA0: 3.6V Others are reserved (0xA1 to 0xFF)

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BUCKD_VOUT (18h)

Format: Direct

The BUCKD_VOUT command sets buck D's output voltage (V_{OUTD}).

Bits	Access	Bit Name	Default	Description
7:0	R/W	BUCKD_VOUT_ SETTING	0x8F	Sets V_{OUTD}. Note that the V_{OUTD} change slew rate is 1mV/µs. If 25h, bit[0] = 0, then buck D outputs a DVS range between 0.4V and 1.2V. 0x00: 0.4V 0x01: 0.41V 0x02: 0.42V 0x03: 0.43V …… 0x4D: 1.17V 0x4E: 1.18V 0x4F: 1.19V 0x50: 1.2V Others are reserved (0x51 to 0xFF) If 25h, bit[0] = 1, then buck D outputs a DVS range between 1.2V and 3.6V. 0x00: 1.2V 0x01: 1.215V 0x02: 1.23V 0x03: 1.245V …… 0x8C: 3.3V 0x8D: 3.315V 0x8E: 3.33V …… 0x9F: 3.585V 0xA0: 3.6V Others are reserved (0xA1 to 0xFF)

PON_CONFIG_0 (19h)

Format: Unsigned binary

The PON_CONFIG_0 command sets the power-on sequence for configuration 0.

Bits	Access	Bit Name	Default	Description
7	R/W	PON_SEQ_CONFIG0	1'b1	Sets the power-on sequence for configuration 0. 1'b0: Does not execute configuration 0 1'b1: Executes configuration 0
6	R/W	PON_SEQ_CONFIG0_ BUCKA	1'b1	Enables buck A's output regulator. 1'b0: Disables buck A's output regulator 1'b1: Enables buck A's output regulator
5	R/W	PON_SEQ_CONFIG0_ BUCKB	1'b1	Enables buck B's output regulator. 1'b0: Disables buck B's output regulator 1'b1: Enables buck B's output regulator
4	R/W	PON_SEQ_CONFIG0_ BUCKC	1'b1	Enables buck C's output regulator. 1'b0: Disables buck C's output regulator 1'b1: Enables buck C's output regulator

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3	R/W	PON_SEQ_CONFIG0_BUCKD	1'b1	Enables buck D's output regulator. 1'b0: Disables buck D's output regulator 1'b1: Enables buck D's output regulator
2:0	R	RESERVED	N/A	Reserved.

PON_CONFIG_1 (1Ah)

Format: Unsigned binary

The PON_CONFIG_1 command sets the power-on sequence for configuration 1.

Bits	Access	Bit Name	Default	Description
7	R/W	PON_SEQ_CONFIG1	1'b0	Sets the power-on sequence for configuration 1. 1'b0: Does not execute configuration 1 1'b1: Executes configuration 1
6	R/W	PON_SEQ_CONFIG1_BUCKA	1'b0	Enables buck A's output regulator. 1'b0: Disables buck A's output regulator 1'b1: Enables buck A's output regulator
5	R/W	PON_SEQ_CONFIG1_BUCKB	1'b0	Enables buck B's output regulator. 1'b0: Disables buck B's output regulator 1'b1: Enables buck B's output regulator
4	R/W	PON_SEQ_CONFIG1_BUCKC	1'b0	Enables buck C's output regulator. 1'b0: Disables buck C's output regulator 1'b1: Enables buck C's output regulator
3	R/W	PON_SEQ_CONFIG1_BUCKD	1'b0	Enables buck D's output regulator. 1'b0: Disables buck D's output regulator 1'b1: Enables buck D's output regulator
2:0	R	RESERVED	N/A	Reserved.

PON_CONFIG_2 (1Bh)

Format: Unsigned binary

The PON_CONFIG_2 command sets the power-on sequence for configuration 2.

Bits	Access	Bit Name	Default	Description
7	R/W	PON_SEQ_CONFIG2	1'b0	Sets the power-on sequence for configuration 2. 1'b0: Does not execute configuration 2 1'b1: Executes configuration 2
6	R/W	PON_SEQ_CONFIG2_BUCKA	1'b0	Enables buck A's output regulator. 1'b0: Disables buck A's output regulator 1'b1: Enables buck A's output regulator
5	R/W	PON_SEQ_CONFIG2_BUCKB	1'b0	Enables buck B's output regulator. 1'b0: Disables buck B's output regulator 1'b1: Enables buck B's output regulator
4	R/W	PON_SEQ_CONFIG2_BUCKC	1'b0	Enables buck C's output regulator. 1'b0: Disables buck C's output regulator 1'b1: Enables buck C's output regulator
3	R/W	PON_SEQ_CONFIG2_BUCKD	1'b0	Enables buck D's output regulator. 1'b0: Disables buck D's output regulator 1'b1: Enables buck D's output regulator

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2:0	R	RESERVED	N/A	Reserved.

PON_CONFIG_3 (1Ch)

Format: Unsigned binary

The PON_CONFIG_3 command sets the power-on sequence for configuration 3.

Bits	Access	Bit Name	Default	Description
7	R/W	PON_SEQ_CONFIG3	1'b0	Sets the power-on sequence for configuration 3. 1'b0: Does not execute configuration 3 1'b1: Executes configuration 3
6	R/W	PON_SEQ_CONFIG3_BUCKA	1'b0	Enables buck A's output regulator. 1'b0: Disables buck A's output regulator 1'b1: Enables buck A's output regulator
5	R/W	PON_SEQ_CONFIG3_BUCKB	1'b0	Enables buck B's output regulator. 1'b0: Disables buck B's output regulator 1'b1: Enables buck B's output regulator
4	R/W	PON_SEQ_CONFIG3_BUCKC	1'b0	Enables buck C's output regulator. 1'b0: Disables buck C's output regulator 1'b1: Enables buck C's output regulator
3	R/W	PON_SEQ_CONFIG3_BUCKD	1'b0	Enables buck D's output regulator. 1'b0: Disables buck D's output regulator 1'b1: Enables buck D's output regulator
2:0	R	RESERVED	N/A	Reserved.

PON_OFF_DELAY0 (1Dh)

Format: Unsigned binary

The PON_OFF_DELAY0 command sets power-on/-off delay 0.

Bits	Access	Bit Name	Default	Description
7	R	RESERVED	N/A	Reserved.
6:4	R/W	PON_SEQ_DELAY0	3'b000	Sets power-on delay 0, which defines the time between V_{IN} UVLO rising or EN high and the first channel starting to rise. 3'b000: 0ms 3'b001: 1ms 3'b010: 2ms 3'b011: 3ms 3'b100: 4ms 3'b101: 5ms 3'b110: 8ms 3'b111: 10ms
3	R	RESERVED	N/A	Reserved.
2:0	R/W	POFF_SEQ_DELAY0	3'b000	Sets power-off delay 0, which defines the time between V_{IN} UVLO falling or EN low and the first channel starting to fall. 3'b000: 0ms 3'b001: 1ms 3'b010: 2ms 3'b011: 4ms 3'b100: 6ms Others are reserved.

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PON_SEQ_DELAY_1_2 (1Eh)

Format: Unsigned binary

The PON_SEQ_DELAY_1_2 command sets power-on sequence delay 1 and delay 2.

Bits	Access	Bit Name	Default	Description
7:4	R/W	PON_SEQ_DELAY1	4'b0000	Sets power-on sequence delay 1. 4'b0000: 0ms 4'b0001: 1ms 4'b0010: 2ms 4'b0011: 3ms 4'b0100: 4ms 4'b0101: 5ms 4'b0110: 6ms 4'b0111: 7ms 4'b1000: 8ms 4'b1001: 9ms 4'b1010: 10ms Others are reserved.
3:0	R/W	PON_SEQ_DELAY2	4'b0000	Sets power-on sequence delay 2. 4'b0000: 0ms 4'b0001: 1ms 4'b0010: 2ms 4'b0011: 3ms 4'b0100: 4ms 4'b0101: 5ms 4'b0110: 6ms 4'b0111: 7ms 4'b1000: 8ms 4'b1001: 9ms 4'b1010: 10ms Others are reserved.

PON_SEQ_DELAY_3_PG (1Fh)

Format: Unsigned binary

The PON_SEQ_DELAY_3_PG command sets power-on sequence delay 3 and the PG delay.

Bits	Access	Bit Name	Default	Description
7:4	R/W	PON_SEQ_DELAY3	4'b0000	Sets power-on sequence delay 3. 4'b0000: 0ms 4'b0001: 1ms 4'b0010: 2ms 4'b0011: 3ms 4'b0100: 4ms 4'b0101: 5ms 4'b0110: 6ms 4'b0111: 7ms 4'b1000: 8ms 4'b1001: 9ms 4'b1010: 10ms Others are reserved.

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3:0	R/W	PON_SEQ_DELAY_PG	4'b0000	Sets the PG delay of the power-on sequence. 4'b0000: 0ms 4'b0001: 1ms 4'b0010: 2ms 4'b0011: 3ms 4'b0100: 4ms 4'b0101: 5ms 4'b0110: 6ms 4'b0111: 7ms 4'b1000: 8ms 4'b1001: 9ms 4'b1010: 10ms Others are reserved.

POFF_SEQ_CONFIG_0 (20h)

Format: Unsigned binary

The POFF_SEQ_CONFIG_0 command sets the power-off sequence for configuration 0.

Bits	Access	Bit Name	Default	Description
7	R/W	POFF_SEQ_CONFIG0	1'b1	Sets the power-off sequence for configuration 0. 1'b0: Does not execute configuration 0 1'b1: Executes configuration 0
6	R/W	POFF_SEQ_ CONFIG0_BUCKA	1'b1	Disables buck A's output regulator. 1'b0: Does not disable buck A's output regulator 1'b1: Disables buck A's output regulator
5	R/W	POFF_SEQ_ CONFIG0_BUCKB	1'b1	Disables buck B's output regulator. 1'b0: Does not disable buck B's output regulator 1'b1: Disables buck B's output regulator
4	R/W	POFF_SEQ_ CONFIG0_BUCKC	1'b1	Disables buck C's output regulator. 1'b0: Does not disable buck C's output regulator 1'b1: Disables buck C's output regulator
3	R/W	POFF_SEQ_ CONFIG0_BUCKD	1'b1	Disables buck D's output regulator. 1'b0: Does not disable buck D's output regulator 1'b1: Disables buck D's output regulator
2:0	R/W	POFF_SEQ_DELAY1	3'b000	Sets power delay 1. 3'b000: 0ms 3'b001: 1ms 3'b010: 2ms 3'b011: 4ms 3'b100: 6ms Others are reserved.

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POFF_SEQ_CONFIG_1 (21h)

Format: Unsigned binary

The POFF_SEQ_CONFIG_1 command sets the power-off sequence for configuration 1.

Bits	Access	Bit Name	Default	Description
7	R/W	POFF_SEQ_CONFIG1	1'b0	Sets the power-off sequence for configuration 1. 1'b0: Does not execute configuration 1 1'b1: Executes configuration 1
6	R/W	POFF_SEQ_ CONFIG1_BUCKA	1'b1	Disables buck A's output regulator. 1'b0: Does not disable buck A's output regulator 1'b1: Disables buck A's output regulator
5	R/W	POFF_SEQ_ CONFIG1_BUCKB	1'b1	Disables buck B's output regulator. 1'b0: Does not disable buck B's output regulator 1'b1: Disables buck B's output regulator
4	R/W	POFF_SEQ_ CONFIG1_BUCKC	1'b1	Disables buck C's output regulator. 1'b0: Does not disable buck C's output regulator 1'b1: Disables buck C's output regulator
3	R/W	POFF_SEQ_ CONFIG1_BUCKD	1'b1	Disables buck D's output regulator. 1'b0: Does not disable buck D's output regulator 1'b1: Disables buck D's output regulator
2:0	R/W	POFF_SEQ_DELAY2	3'b000	Sets power delay 2. 3'b000: 0ms 3'b001: 1ms 3'b010: 2ms 3'b011: 4ms 3'b100: 6ms Others are reserved.

POFF_SEQ_CONFIG_2 (22h)

Format: Unsigned binary

The POFF_SEQ_CONFIG_2 command sets the power-off sequence for configuration 2.

Bits	Access	Bit Name	Default	Description
7	R/W	POFF_SEQ_CONFIG2	1'b0	Sets the power-off sequence for configuration 2. 1'b0: Does not execute configuration 2 1'b1: Executes configuration 2
6	R/W	POFF_SEQ_ CONFIG2_BUCKA	1'b1	Disables buck A's output regulator. 1'b0: Does not disable buck A's output regulator 1'b1: Disables buck A's output regulator
5	R/W	POFF_SEQ_ CONFIG2_BUCKB	1'b1	Disables buck B's output regulator. 1'b0: Does not disable buck B's output regulator 1'b1: Disables buck B's output regulator
4	R/W	POFF_SEQ_ CONFIG2_BUCKC	1'b1	Disables buck C's output regulator 1'b0: Does not disable buck C's output regulator 1'b1: Disables buck C's output regulator

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3	R/W	POFF_SEQ_ CONFIG2_BUCKD	1'b1	Disables buck D's output regulator. 1'b0: Does not disable buck D's output regulator 1'b1: Disables buck D's output regulator
2:0	R/W	POFF_SEQ_DELAY3	3'b000	Sets power delay 3. 3'b000: 0ms 3'b001: 1ms 3'b010: 2ms 3'b011: 4ms 3'b100: 6ms Others are reserved.

POFF_SEQ_CONFIG_3 (23h)

Format: Unsigned binary

The POFF_SEQ_CONFIG_3 command sets the power-off sequence for configuration 3.

Bits	Access	Bit Name	Default	Description
7	R/W	POFF_SEQ_CONFIG3	1'b0	Sets the power-off sequence for configuration 3. 1'b0: Does not execute configuration 3 1'b1: Executes configuration 3
6	R/W	POFF_SEQ_ CONFIG3_BUCKA	1'b0	Disables buck A's output regulator. 1'b0: Does not disable buck A's output regulator 1'b1: Disables buck A's output regulator
5	R/W	POFF_SEQ_ CONFIG3_BUCKB	1'b0	Disables buck B's output regulator. 1'b0: Does not disable buck B's output regulator 1'b1: Disables buck B's output regulator
4	R/W	POFF_SEQ_ CONFIG3_BUCKC	1'b0	Disables buck C's output regulator. 1'b0: Does not disable buck C's output regulator 1'b1: Disables buck C's output regulator
3	R/W	POFF_SEQ_ CONFIG3_BUCKD	1'b0	Disables buck D's output regulator. 1'b0: Does not disable buck D's output regulator 1'b1: Disables buck D's output regulator
2:0	R	RESERVED	N/A	Reserved.

ADC_TEMP (24h)

Format: Unsigned binary

The ADC_TEMP command monitors the junction temperature (T_J) of the IC.

Bits	Access	Bit Name	Description
7:5	R	ADC_TEMP_ READOUT	Measures T_J. 3'b000: <85°C 3'b001: 85°C to 95°C 3'b010: 95°C to 105°C 3'b011: 105°C to 115°C 3'b100: 115°C to 125°C 3'b101: 125°C to 135°C 3'b110: 135°C to 145°C 3'b111: >145°C
4:0	R/W	RESERVED	Reserved.

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VOUT_RANGE_SELECT (25h)

Format: Unsigned binary

The VOUT_RANGE_SELECT command selects the V_{OUTx} range.

Bits	Access	Bit Name	Default	Description
7:4	R	RESERVED	N/A	Reserved.
3	R/W	BUCKA_VOUT_ RANGE_SELECT	1'b1	Selects the V_{OUTA} range. 1'b0: 0.4V to 1.2V with 10mV/step 1'b1: 1.2V to 3.6V with 15mV/step
2	R/W	BUCKB_VOUT_ RANGE_SELECT	1'b1	Selects the V_{OUTB} range. 1'b0: 0.4V to 1.2V with 10mV/step 1'b1: 1.2V to 3.6V with 15mV/step
1	R/W	BUCKC_VOUT_ RANGE_SELECT	1'b1	Selects the V_{OUTC} range. 1'b0: 0.4V to 1.2V with 10mV/step 1'b1: 1.2V to 3.6V with 15mV/step
0	R/W	BUCKD_VOUT_ RANGE_SELECT	1'b1	Selects the V_{OUTD} range. 1'b0: 0.4V to 1.2V with 10mV/step 1'b1: 1.2V to 3.6V with 15mV/step

CLP_BUCKX (26h)

Format: Unsigned binary

The CLP_BUCKX command sets buck x's current limit (I_{LIMITx}) threshold (where x = A, B, C, or D).

Bits	Access	Bit Name	Default	Description
7:6	R/W	CLP_BUCKA	2'b10	Sets buck A's valley current limit (I_{LIMITA}). 00: 4.5A 01: 5A 10: 5.5A 11: 6A
5:4	R/W	CLP_BUCKB	2'b10	Sets buck B's valley current limit (I_{LIMITB}). 00: 4.5A 01: 5A 10: 5.5A 11: 6A
3:2	R/W	CLP_BUCKC	2'b10	Sets buck C's valley current limit (I_{LIMITC}). 00: 4.5A 01: 5A 10: 5.5A 11: 6A
1:0	R/W	CLP_BUCKD	2'b10	Sets buck D's valley current limit (I_{LIMITD}). 00: 4.5A 01: 5A 10: 5.5A 11: 6A

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OC_STATUS_CLEAR (2Ah)

Format: Unsigned binary

The OC_STATUS_CLEAR command monitors the OC status and clear register.

Bits	Access	Bit Name	Default	Description
7	R/W	CLEAR_BUCKA_OC_STATUS	1'b0	1'b1: Clears the status of 2Ah, bit[3]
6	R/W	CLEAR_BUCKB_OC_STATUS	1'b0	1'b1: Clears the status of 2Ah, bit[2]
5	R/W	CLEAR_BUCKC_OC_STATUS	1'b0	1'b1: Clears the status of 2Ah, bit[1]
4	R/W	CLEAR_BUCKD_OC_STATUS	1'b0	1'b1: Clears the status of 2Ah, bit[0]
3	R	BUCKA_OC_STATUS	1'b0	1'b0: Indicates no OC fault for buck A's output 1'b1: Indicates an OC fault for buck A's output
2	R	BUCKB_OC_STATUS	1'b0	1'b0: Indicates no OC fault for buck B's output 1'b1: Indicates an OC fault for buck B's output
1	R	BUCKC_OC_STATUS	1'b0	1'b0: Indicates no OC fault for buck C's output 1'b1: Indicates an OC fault for buck C's output
0	R	BUCKD_OC_STATUS	1'b0	1'b0: Indicates no OC fault for buck D's output 1'b1: Indicates an OC fault for buck D's output

MTP_AUTO_REG (30h)

Format: Unsigned binary

The MTP_AUTO_REG command controls MTP automatic write. The steps of MTP write operation are described below:

1. Configure all the MTP registers.
2. Write 14h, bit[6] from 0 to 1 to disable write protection.
3. Ensure that buck x is off before configuring MTP. It is recommended to pull down the external EN pin.
4. Write 30h, bit[7] from 0 to 1 to enable MTP automatic write.
5. Wait about 2s.
6. Read 30h to 0x5A to indicate that MTP configuring is finished.

Bits	Access	Bit Name	Default	Description
7	R/W	MTP_AUTO_WRITE	1'b0	If 1'b0 changes to 1'b1, this enables MTP automatic write.
6	R	MTP_WRITE_DONE	1'b0	If 1'b0 changes to 1'b1, MTP finishes.
5:0	R	RESERVED	N/A	Reserved.

PART_ID (31h)

Format: Unsigned binary

The PART_ID command sets the MPM54524's ID number.

Bits	Access	Bit Name	Default	Description
7:0	R	PART_ID	0x24	Sets the MPM54524's ID number.

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CODE_ID (35h)

Format: Unsigned binary

The CODE_ID command sets the code ID number.

Bits	Access	Bit Name	Default	Description
7:0	R	CODE_ID	0x00	Sets the code ID number.

CODE_VERSION (36h)

Format: Unsigned binary

The CODE_VERSION command sets the code version number.

Bits	Access	Bit Name	Default	Description
7:0	R	CODE_VERSION	0x00	Sets the code version number.

ACTIVE_POSITION_ENABLE_A/B (71h) (12) (13)

Format: Unsigned binary

The ACTIVE_POSITION_ENABLE_A/B command enables the active voltage positioning (AVP) function of buck A and buck B.

Bits	Access	Bit Name	Default	Description
7	R/W	AVP_EN_A/B	1'b1	Enables the AVP function of buck A and buck B. 1'b0: Disabled 1'b1: Enabled
6:0	R	RESERVED	N/A	Reserved.

I2C_ADDRESS (73h) (12) (13)

Format: Unsigned binary

The I2C_ADDRESS command sets the I²C address.

Bits	Access	Bit Name	Default	Description
7:4	R	RESERVED	N/A	Reserved.
3:1	R/W	ADDRESS_BITS	3'b 000	Defines the I²C address, bits [6:4]. The I²C address can be modified via the MTP and is changed during the next power-on.
0	R	RESERVED	N/A	Reserved.

ACTIVE_POSITION_ENABLE_C/D (79h) (13) (14)

Format: Unsigned binary

The ACTIVE_POSITION_ENABLE_C/D command enables the AVP function of buck C or buck D.

Bits	Access	Bit Name	Default	Description
7	RW	AVP_EN_C/D	1'b1	Enables the AVP function of buck C or D. 1'b0: Disabled 1'b1: Enabled
6:0	R	RESERVED	N/A	Reserved.

Notes:

13) To operate 71h, 73h, and 79h, a password must be written to the device following the steps below:
    a. Write C1h to 95h.
    b. Write C1h to 63h.
14) To write the register to the MTP, follow the steps below:
    a. Configure 71h, 73h, and 79h.
    b. Write 87h to 80h.
    c. Wait about 1s, then read 87h. If 87h is at 00h, writing to the MTP was successful; otherwise, writing to the MTP has failed.

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VIN_OV_REG (90h)

Format: Unsigned binary

The VIN_OV_REG command sets V_{INy} UVLO hysteresis and V_{INy} OVP.

Bits	Access	Bit Name	Default	Description
7:2	R	RESERVED	N/A	Reserved.
1	R/W	VIN_UVLO_ HYSTERESIS	1'b0	Selects V_{INy} UVLO hysteresis. 1'b0: 0.125V 1'b1: 0.25V
0	R/W	VIN_OVP	1'b0	Enables V_{INy} OVP. 1'b0: Disabled 1'b1: Enabled

VIN_UVLO_REG (AFh)

Format: Unsigned binary

The VIN_UVLO_REG command sets V_{INy} UVLO.

Bits	Access	Bit Name	Default	Description
7:2	R	RESERVED	N/A	Reserved.
1:0	R/W	VIN_UVLO	2'b00	Selects V_{INy} UVLO. 00: 3V 01: 3.5V 10: 3.75V 11: 4V

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APPLICATION INFORMATION

Setting the Output Voltage with an Internal Divider

The MPM54524 can set V_{OUTx} via an internal divider by connecting VOUTx to VSx+ (see Figure 13 on page 51, Figure 14 on page 51, and Figure 15 on page 52). [15]

The user can reconfigure and set the output voltages. For more details, see the VOUT_RANGE_SELECT (25h) section on page 43 [16], as well as the following sections for each output:

- BUCKA_VOUT (15h) on page 33
- BUCKB_VOUT (16h) on page 34
- BUCKC_VOUT (17h) on page 35
- BUCKD_VOUT (18h) on page 36.

Notes:

15) When an internal divider is used, the ADC readback voltage in BUCKX_VOLTAGE (06h) is the direct value of V_{OUTx}.
16) The new VOUT_RANGE_SELECT (25h) setting does not take effect until the EN pin is toggled.

Setting the Output Voltage with an External Divider

The MPM54524 can also set V_{OUTx} via an external resistor divider (see Figure 11, as well as Figure 16 on page 52, Figure 17 on page 53, and Figure 18 on page 53). [17]

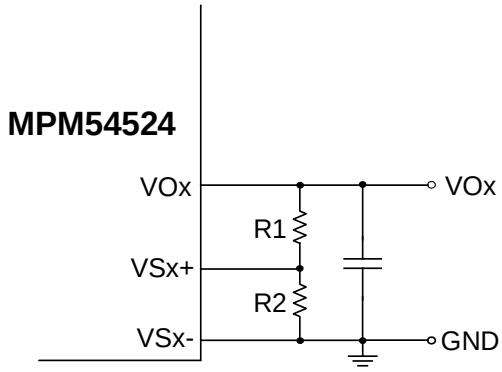

Figure 11: Feedback Network

The FB voltage (V_{FB}) is determined by the V_{OUTx} configuration registers. For example, set VOUT_RANGE_SELECT (25h) to 00h and the following V_{OUTx} registers:

- BUCKA_VOUT (15h)
- BUCKB_VOUT (16h)
- BUCKC_VOUT (17h)
- BUCKD_VOUT (18h)

to 14h to generate a 0.6V V_{FB}. [18]

Consider the tradeoff between stability and dynamic response to select a feedback resistor (R1) that is not too large or too small. R2 can be calculated with Equation (3):

$$R2 = \frac{R1}{\frac{V_{OUTx}}{V_{REF}} - 1} \quad (3)$$

Table 2 lists the recommended resistances for common V_{OUTx} values with 0.6V V_{FB}.

Table 2: Resistances for Common V_{OUTx} Values

V_{OUTx} (V)	R1 (kΩ)	R2 (kΩ)
1	10	15
1.2	10	10
1.8	10	5
2.5	10	3.15
3.3	10	2.2
5.5	10	1.23

Along with the change in resistors, VOUT_RANGE_SELECT (25h) should be set to 1'b0 for a V_{OUTx} range between 0.4V and 1.2V with 10mV/step; it should be set to 1'b1 for a 1.2V to 3.6V V_{OUTx} range with 15mV/step.

Notes:

17) After using an external divider to set V_{OUTx}, the ADC readback voltage (BUCK_XVOLTAGE (06h)) monitors V_{FB}, not V_{OUTx}. The user must multiply this value with the external resistor divider ratio to obtain the true V_{OUTx} (see Equation (3) for more details).
18) BUCKA_VOUT (15h), BUCKB_VOUT (16h), BUCKC_VOUT (17h), and BUCKD_VOUT (18h) can be set to different values but this will alter the effective V_{OUTx} in Table 2. Use Equation (3) to calculate V_{OUTx} in this case.

Selecting the Input Capacitor

The step-down converter has a discontinuous input current (I_{IN}), and requires a capacitor to supply AC current to the converter while maintaining the DC V_{IN}. For the best performance, it is recommended to use low-ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are recommended for the best results due to their low ESR and small temperature coefficients. For most applications, use a 22µF capacitor.

Since C1 absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor (C_{IN}) (I_{C1}) can be estimated with Equation (4):

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$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (4)$$

The worse-case condition occurs at V_{IN} = 2 x V_{OUT}, where I_{C1} can be calculated with Equation (5):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (5)$$

For simplification, choose C_{IN} with an RMS current rating exceeding half of the maximum load current.

C_{IN} can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g. 0.1µF) placed as close to the IC as possible. When using ceramic capacitors, ensure they have enough capacitance to provide sufficient charge, which prevents excessive voltage ripple at the input. The input voltage ripple (ΔV_{IN}) caused by the capacitance can be estimated with Equation (6):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (6)$$

Selecting the Output Capacitor for the Step-Down Regulator

The output capacitor (C_{OUT}) for the step-down regulator maintains the DC V_{OUT}. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For the best results, use low-ESR capacitors to keep the output voltage ripple (ΔV_{OUT}) low. ΔV_{OUT} can be estimated by Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C2}\right) \quad (7)$$

Where L1 is the inductance, and R_{ESR} is the equivalent series resistance (ESR) of C_{OUT}.

For ceramic capacitors, the capacitance dominates the impedance at the f_{SW}, and the capacitance causes the majority of ΔV_{OUT}. For simplification, ΔV_{OUT} can be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^{2} \times L1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (8)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at f_{SW}. For simplification, ΔV_{OUT} can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (9)$$

The C_{OUT} characteristics also affect the stability of the regulation system.

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PCB Layout Guidelines

Efficient PCB layout is very critical for stable operation. For the best results, refer to Figure 12 and follow the guidelines.

1. Connect the input ground to the GND pin using the shortest and widest trace possible.
2. Connect C_{IN} to the VINy pin using the shortest and widest trace possible.
3. Ensure all FB connections are short and direct using Kelvin connections. Place the FB resistors and compensation components as close to the chip as possible.
4. Route SWx (where x = A, B, C, or D) away from sensitive analog areas such as FB.

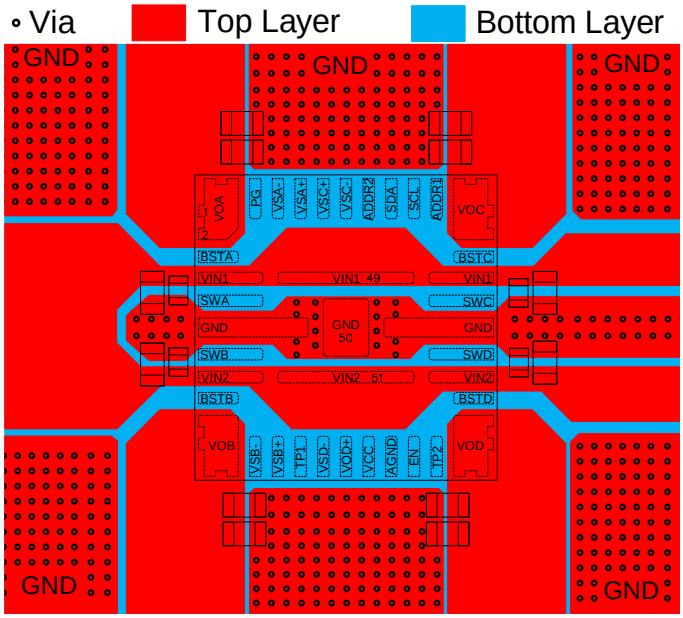

Figure 12: Recommended PCB Layout

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MULTIPLE-TIME PROGRAMMBLE (MTP) CONFIGURATION

Table 3: -0000 Suffix Code Configuration

MTP Parameters	VOA	VOB	VOC	VOD
Output voltage (V_{OUT})	3.345V	3.345V	3.345V	3.345V
Mode	FCCM	FCCM	FCCM	FCCM
Bits[6:4] of the I²C address	000			
Soft-start time (t_{SS_x})	2ms	2ms	2ms	2ms
Soft shutdown time enable/disable	Disabled	Disabled	Disabled	Disabled
Soft shutdown time	-	-	-	-
Switching frequency (f_{SW})	1000kHz	1000kHz	1000kHz	1000kHz
Valley current limit	5.5A	5.5A	5.5A	5.5A
Buck output discharge enable	Enabled	Enabled	Enabled	Enabled
Buck output discharge resistor	2Ω	2Ω	2Ω	2Ω
Power good (PG) threshold	95%	95%	95%	95%
VOA and VOB interleaving enable/disable	Disabled		Disabled	
VOA start-up delay time 0	0ms			
VOB start-up delay time 1	0ms			
VOC start-up delay time 2	0ms			
VOD start-up delay time 3	0ms			
PG start-up delay time 4	0ms			
VOA off delay time 0	0ms			
VOB off delay time 1	0ms			
VOC off delay time 2	0ms			
VOD off delay time 3	0ms			
Active voltage positioning (AVP) function enable/disable	Enabled			
Current monitor enable/disable	Enabled			
Voltage monitor enable/disable	Enabled			
Load line	40mV/A			

Table 4: -0000 Suffix Code Register Values

Register	Hex Value	Register	Hex Value	Register	Hex Value
09h	0x00	17h	0x8F	26h	0xAAh
0Ah	0x00	18h	0x8F	27h	0x00h
0Bh	0xE0	19h	0xF8	28h	0x00h
0Ch	0x00	1Ah	0x00	29h	0x00h
0Dh	0x00	1Bh	0x00	2Ah	0x00h
0Eh	0xFF	1Ch	0x00	31h	0x24h
0Fh	0xAA	1Dh	0x00	35h	0x00h
10h	0x84	1Eh	0x00	36h	0x00h
11h	0x00	1Fh	0x00	71h	0x80h
12h	0x00	20h	0xF8	73h	0x00h
13h	0xFF	21h	0x78	79h	0x80h
14h	0x00	22h	0x78	-	-
15h	0x8F	23h	0x00	-	-
16h	0x8F	25h	0x0F	-	-

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TYPICAL APPLICATION CIRCUITS

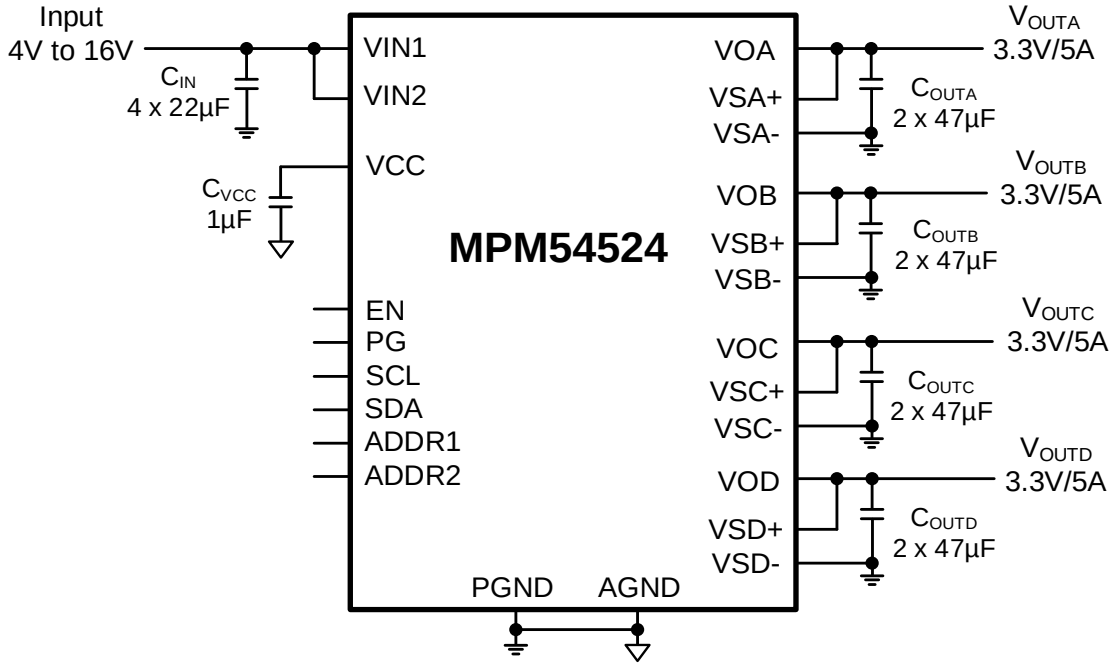

Figure 13: Typical Application Circuit (Quad 5A Outputs with an Internal Divider)

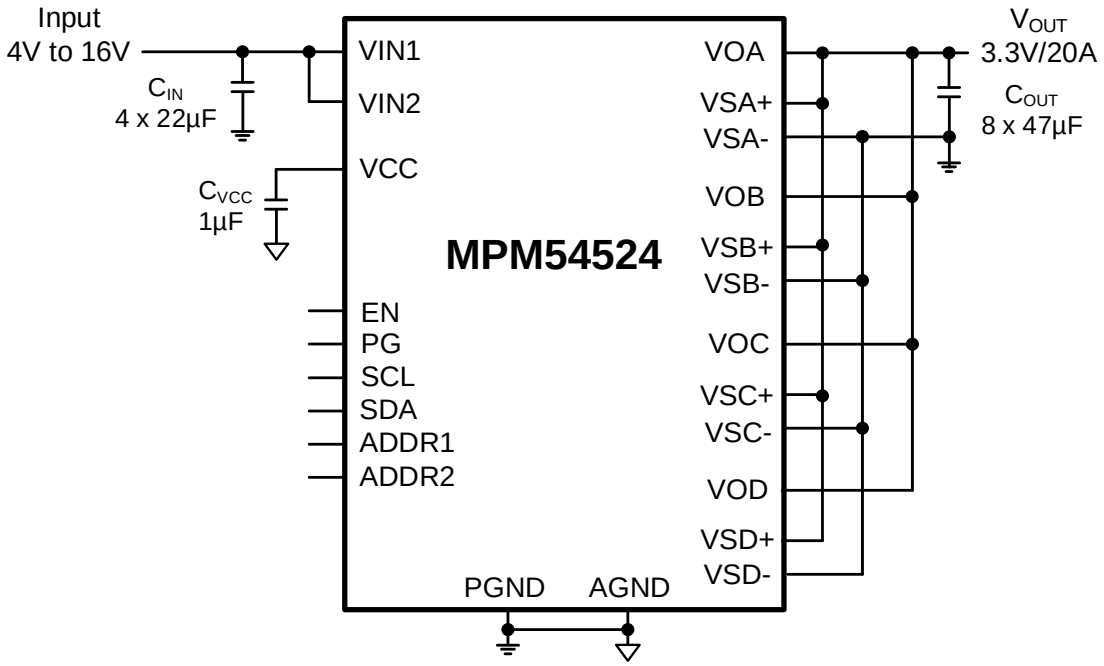

Figure 14: Typical Application Circuit (4-Phase, Single 20A Output with an Internal Divider)

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TYPICAL APPLICATION CIRCUITS *(continued)*

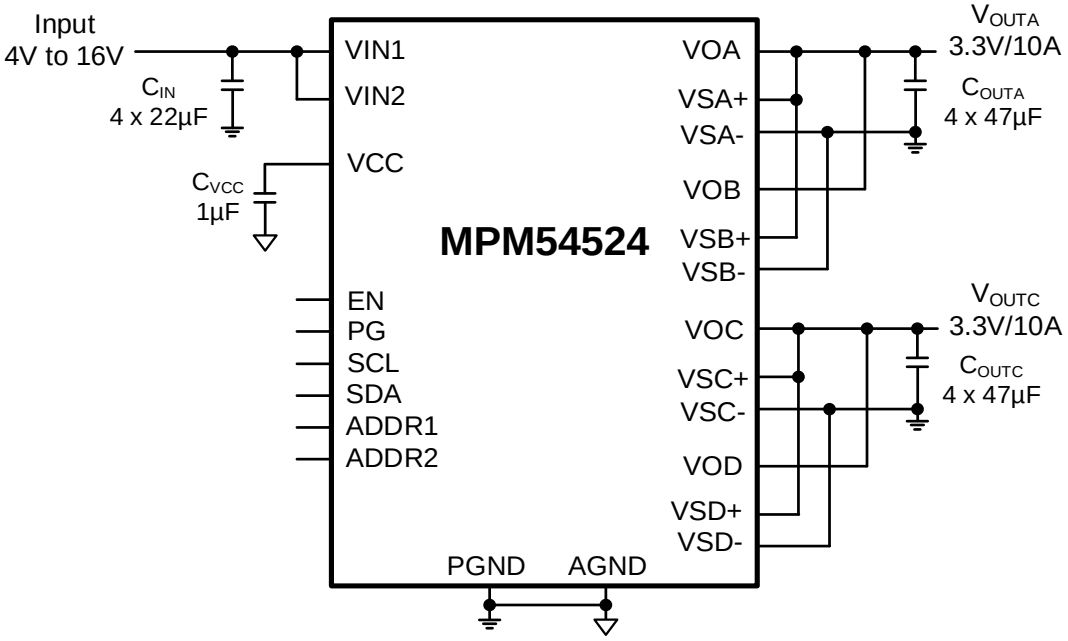

Figure 15: Typical Application Circuit (Dual 10A Outputs with an Internal Divider)

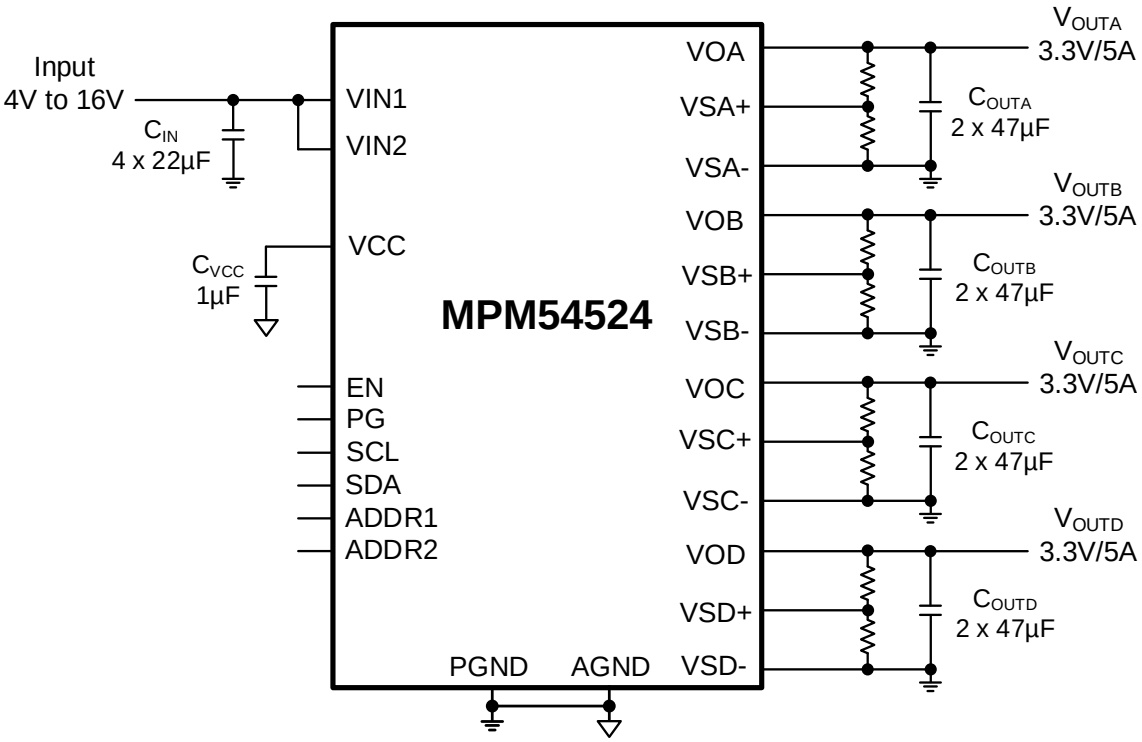

Figure 16: Typical Application Circuit (Quad 5A Outputs with an External Divider)

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TYPICAL APPLICATION CIRCUITS *(continued)*

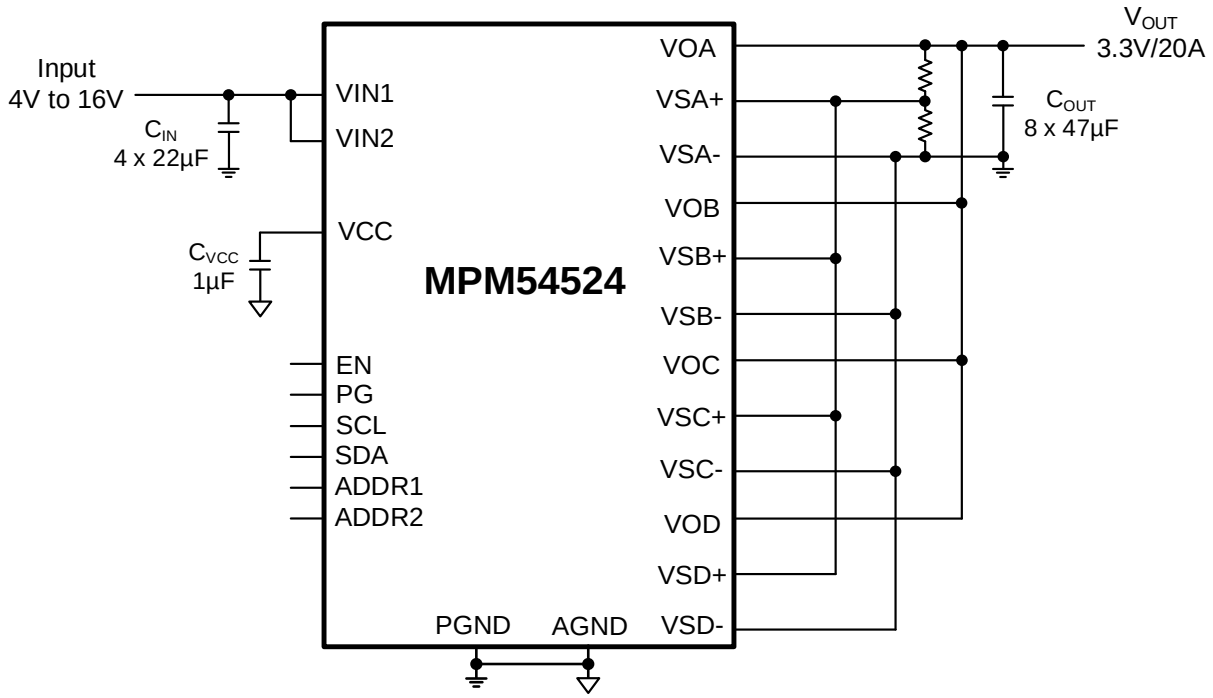

Figure 17: Typical Application Circuit (4-Phase, Single 20A Output with an External Divider)

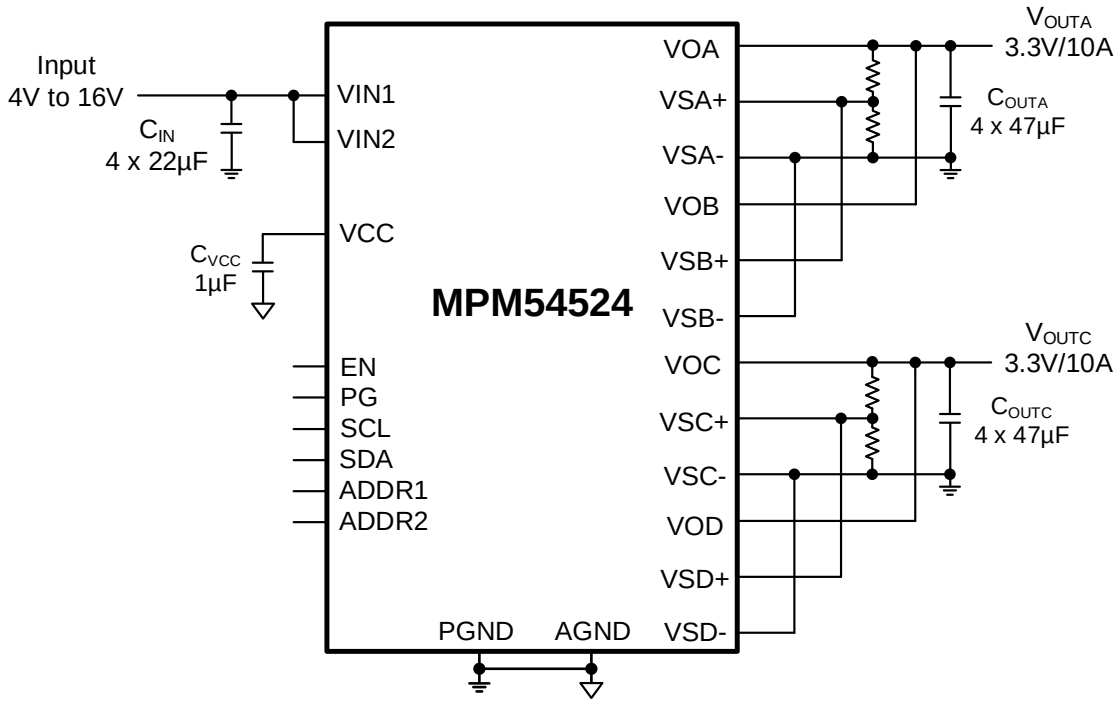

Figure 18: Typical Application Circuit (Dual 10A Outputs with an External Divider)

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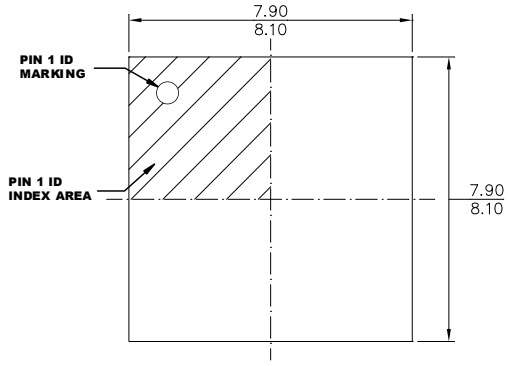
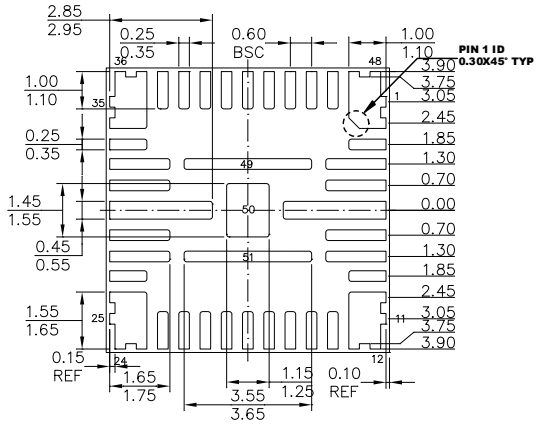
PACKAGE INFORMATION

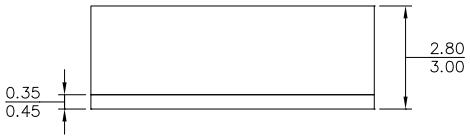
ECLGA-51 (8mmx8mmx2.9mm)



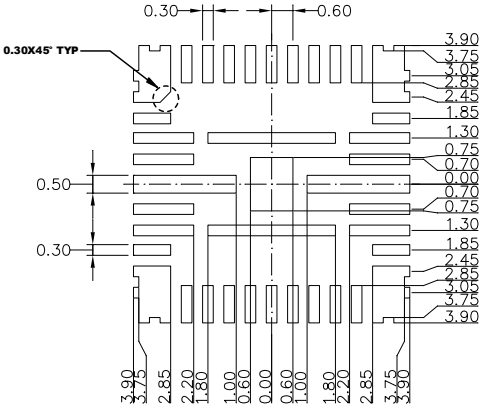
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-303.
4) DRAWING IS NOT TO SCALE.

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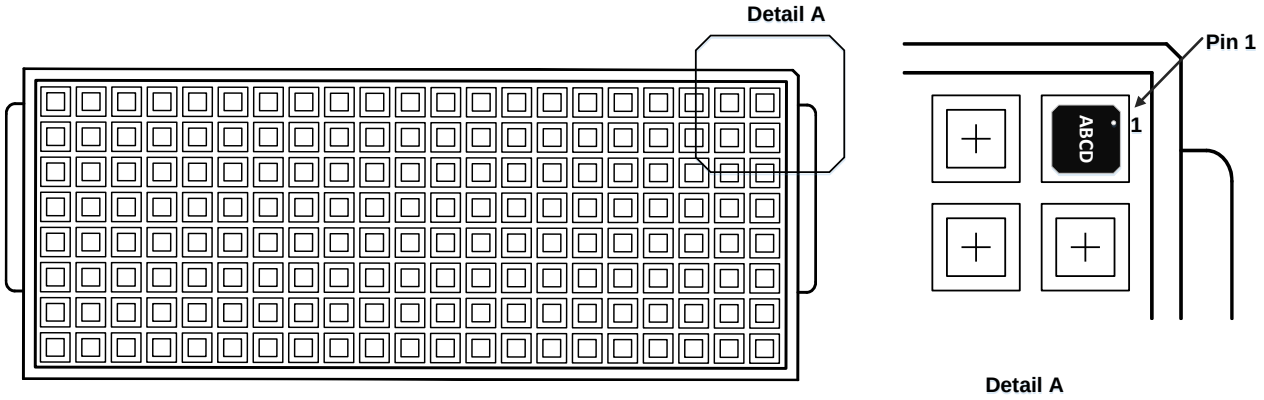
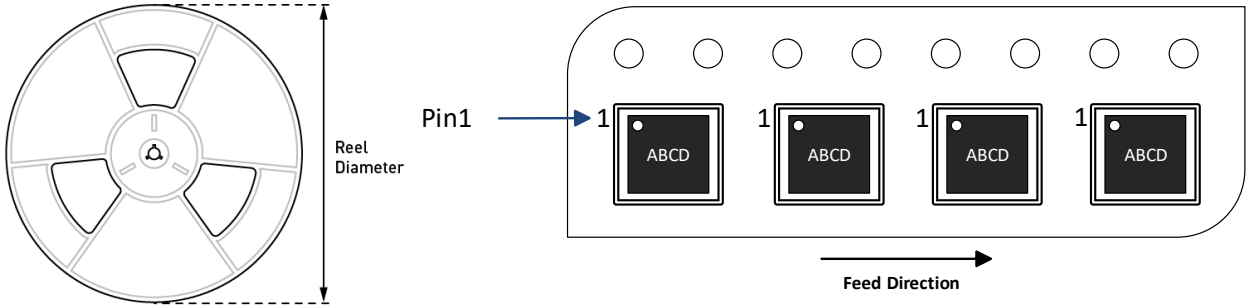
CARRIER INFORMATION (15)



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPM54524GCQ-xxxx-T	ECLGA-51 (8mmx8mmx 2.9mm)	N/A	N/A	260	N/A	N/A	N/A



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPM54524GCQ-xxxx-Z	ECLGA-51 (8mmx8mmx 2.9mm)	1000	N/A	N/A	13in	16mm	12mm

Note:

15) The schematic diagrams of Tray (-T) and Reel (-Z), respectively, where different packages correspond to different lengths, widths, and heights.

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	4/15/2024	Initial Release	-
1.1	8/7/2025	• Updated the Features section: ○ Updated “VINx (where x = A, B, C, or D)” to “VINy (where y = 1 or 2)” ○ Removed all mentions of “(where x = A, B, C, or D)” ○ Removed “switching frequency” ○ Updated all protections with their abbreviations • Moved the Typical Application section to page 1	1
		Updated all mentions of V_{INx} (where x = A, B, C, or D) to V_{INy} (where y = 1 or 2) in the following sections: • Absolute Maximum Ratings and Recommended Operating Conditions • “VIN1 or VIN2” in the Electrical Characteristics • Power Supply Input and Under-Voltage Protection (UVP), Internal VCC Supply, Enable (EN), Power-On Sequence, and Power-Off Sequence • VINy Over Voltage Protection (OVP) • Analog-to-Digital Converter (ADC), Multiple-Time Programmable (MTP) Configuration • Status Registers and STATUS_0 (00h) • CLEAR_0 (07h) • MASK_0 (09h) • VIN_OV_REG (90h) and VIN_UVLO_REG (AFh) • PCB Layout Guidelines	4–5, 15, 17–18, 23, 26–27, 46, 49
		Updated page number references in the following sections: • Power-On Sequence and Power-Off Sequence • Out-of-Phase Operation • Multiple-Time Programmable (MTP) Configuration • Transfer Dart	15, 17–19
		• Added the Setting the Output Voltage with an Internal Divider section ○ Added Note 15 and Note 16 • Updated the Setting the Output Voltage with an External Divider section: ○ Added additional figures for reference (Figure 11, Figure 16, Figure 17, and Figure 18) ○ Deleted the sentence starting with, “After using an external divider…” ○ Added Note 17 and Note 18 ○ Added sentence starting with, “Along with the change in resistors…”	47

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