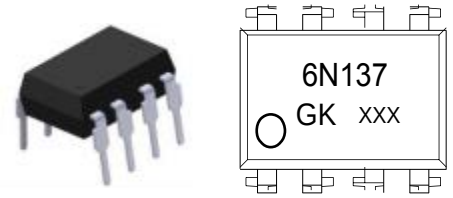
General Description

The 6N137 is consists of an infrared emitting diode optically coupled to a high speed integrated photo detector logic gate with a strobable output. It is packaged in a 8-pin DIP package and available in wide-lead spacing and SMD options.



DIP-8

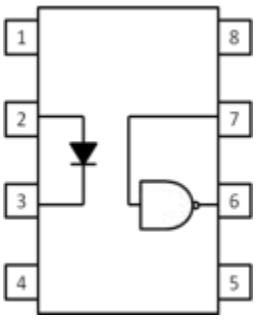
Features

- High speed 10Mbit/s
- 10kV/μs min. common mode transient immunity (EF2611)
- Guaranteed performance from -40 to 85℃
- Logic gate output
- High isolation voltage between input and output (Viso=5000 V rms)
- Pb free and RoHS compliant.

Applications

- Ground loop elimination
- LSTTL to TTL, LSTTL or 5 volt CMOS
- Line receiver, data transmission
- Data multiplexing
- Switching power supplies
- Pulse transformer replacement
- Computer peripheral interface
- High speed logic ground isolation

Schematic



Pin Configuration

1, No Connection
2, Anode
3, Cathode
4. No Connection
5, Gnd
6, V_{out}
7, V_E
8, V_{CC}

Truth Table (Positive Logic)

Input	Enable	Output
H	H	L
L	H	H
H	L	H
L	L	H
H	NC	L
L	NC	H

Absolute Maximum Ratings (Ta=25℃)

	Parameter	Symbol	Rating	Unit
	Forward current	I_F	50	mA
Input	Enable input voltage Not exceed V_{CC} by more than 500	V_E	5.5	V
	Reverse voltage	V_R	5	V
	Power dissipation	P_D	100	mW
	Power dissipation	P_C	85	mW

Absolute Maximum Ratings (Ta=25℃)

Output	Output current	I_O	50	mA
	Output voltage	V_O	7.0	V
	Supply voltage	V_{CC}	7.0	V
Output Power Dissipation		P_O	100	mW
Isolation voltage *1		V_{ISO}	5000	V rms
Operating temperature		T_{OPR}	-40 ~ +85	°C
Storage temperature		T_{STG}	-55 ~ +125	°C
Soldering temperature *2		T_{SOL}	260	°C

Notes:
*1 AC for 1 minute, R.H.= 40 ~ 60% R.H. In this test, pins 1, 2, 3 & 4 are shorted together, and pins 5, 6, 7 & 8 are shorted together.

*2 For 10 seconds.

Transfer Characteristics (Ta=-40 to 85°C unless specified otherwise)

Parameter	Symbol	Min	Typ.	Max.	Unit	Condition
HIGH Level Output Current	I_{OH}	-	2.1	100	uA	V_{CC}=5.5V, V_O=5.5V, I_F=250μA, V_E=2.0V
LOW Level Output Current	V_{OL}	-	0.35	0.6	V	V_{CC} = 5.5V, I_F=5mA, V_E=2.0V, I_{CL}=13mA
Input Threshold Current	I_{FT}	-	2.5	5	mA	V_{CC}= 5.5V, V_O=0.6V, V_E =2.0V, I_{OL}=13mA

Switching Characteristics

(T_a=-40 to 85°C, V_{CC}=5V, I_F=7.5mA unless specified otherwise)

Parameter	Symbol	Min	Typ.	Max.	Unit	Condition
Propagation delay time to output High level*5 (Fig.12)	T_{PHL}	-	35	75	ns	C_L = 15pF, R_L=350Ω, T_A=25°C
Propagation delay time to output Low level*6 (Fig.12)	T_{PLH}	-	40	75	ns	C_L = 15pF, R_L=350Ω, T_A=25°C
Pulse width distortion	|Tphl – Tplh|	-	5	35	ns	C_L = 15pF, R_L=350Ω
Output rise time*7 (Fig.12)	tr	-	40	-	ns	C_L = 15pF, R_L=350Ω
Output fall time*8 (Fig.12)	tf	-	10	-	ns	C_L = 15pF, R_L=350Ω

Parameter	Symbol	Min	Typ.	Max.	Unit	Condition
Enable Propagation Delay Time to Output High Level*9 (Fig.13)	t_{EFH}	-	15	-	ns	I_F = 7.5mA , V_{EH}=3.5V, C_L = 15pF, R_L=350Ω
Enable Propagation Delay Time to Output Low Level*10 (Fig.13)	t_{EHL}	-	15	-	ns	I_F = 7.5mA , V_{EH}=3.5V, C_L = 15pF, R_L=350Ω
Common Mode Transient Immunity at Logic High *11	CM_H	-	-	-	V/μS	I_F = 0mA , V_{OH}=2.0V, R_L=350Ω , T_A=25°C V_{CM}=10Vp-p (Fig 14)
Common Mode Transient Immunity at Logic Low *12	CM_L	-	-	-	V/μS	I_F = 7.5mA , V_{OL}=0.8V, R_L=350Ω, T_A=25°C V_{CM}=10Vp-p (Fig. 14)

Electrical Characteristics (Ta=-40 to 85°C unless specified otherwise)

Input

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Forward voltage	V_F	-	1.4	1.8	V	I_F = 10mA
Reverse voltage	V_R	5.0	-	-	V	I_R = 10μA
Temperature coefficient of forward voltage	$\Delta V_F/\Delta T_A$	-	-1.8	-	mV/°C	I_F =10mA
Input capacitance	C_{IN}	-	60	-	pF	V_F=0, f=1MHz

Output

Parameter	Symbol	Min	Typ.	Max.	Unit	Condition
High level supply current	I_{CCH}	-	7	10	mA	I_F=0mA, V_E=0.5V, V_{CC}=5.5V
Low level supply current	I_{CCL}	-	9	13	mA	I_F=10mA, V_{CC}=5.5V
High level enable current	I_{EH}	-	- 0.6	-1.6	mA	V_E=2.0 V, V_{CC}=5.5V
Low level enable current	I_{EF}	-	- 0.8	-1.6	mA	V_E=0.5 V, V_{CC}=5.5V
High level enable voltage	V_{EH}	2.0	-	-	V	I_F=10mA, V_{CC}=5.5V
Low level enable voltage*4	V_{EF}	-	-	0.8	V	I_F=10mA, V_{CC}=5.5V

Transfer Characteristics (Ta=-40 to 85°C unless specified otherwise)

Parameter	Symbol	Min	Typ.	Max.	Unit	Condition
HIGH Level Output Current	I_{OH}	-	2.1	100	uA	V_{CC}=5.5V, V_O=5.5V, I_F=250μA, V_E=2.0V
LOW Level Output Current	V_{OL}	-	0.35	0.6	V	V_{CC} = 5.5V, I_F=5mA, V_E=2.0V,I_{CL}=13mA
Input Threshold Current	I_{FT}	-	2.5	5	mA	V_{CC}= 5.5V, V_O=0.6V, V_E =2.0V,I_{OL}=13mA

RATING AND CHARACTERISTIC CURVES

Fig.1 Input Diode Forward Voltage vs. Forward Current

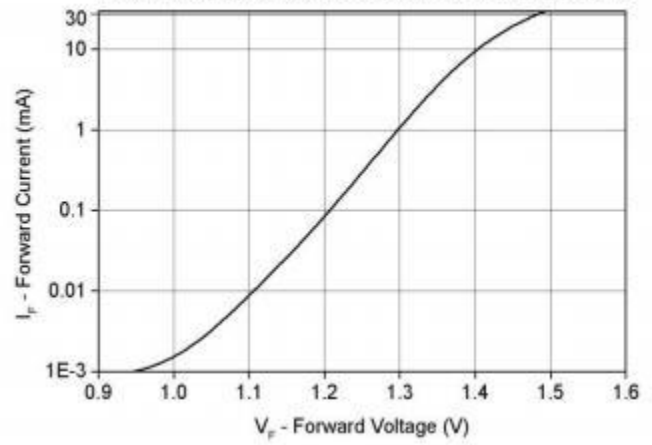


Fig.2 Low Level Output Voltage vs. Ambient Temperature

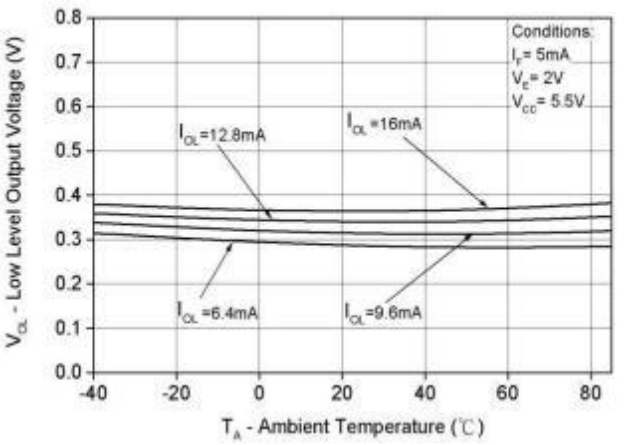


Fig.3 Low Level Output Current vs. Ambient Temperature

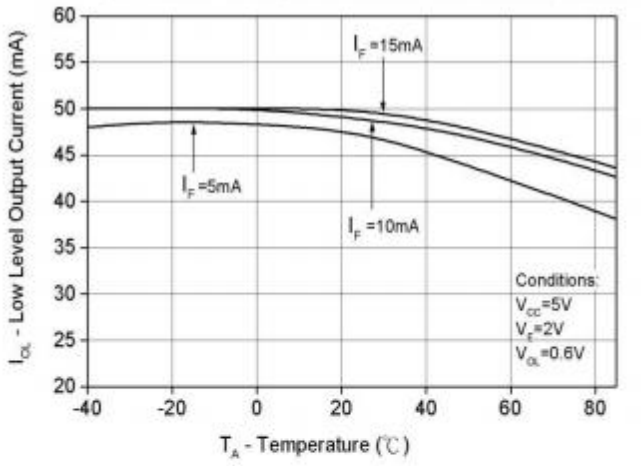


Fig.4 Input Threshold Current vs. Ambient Temperature

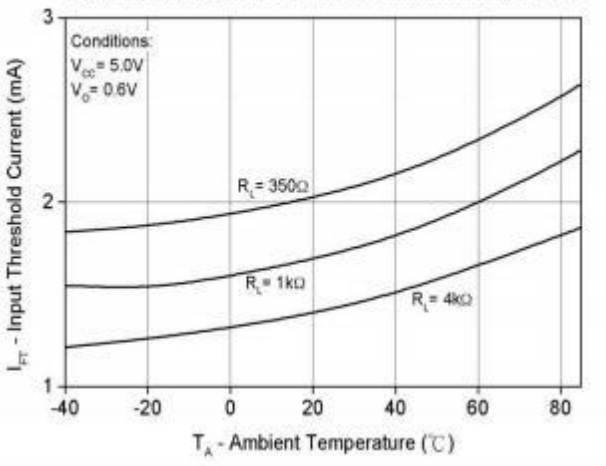


Fig.5 Output Voltage vs. Input Forward Current

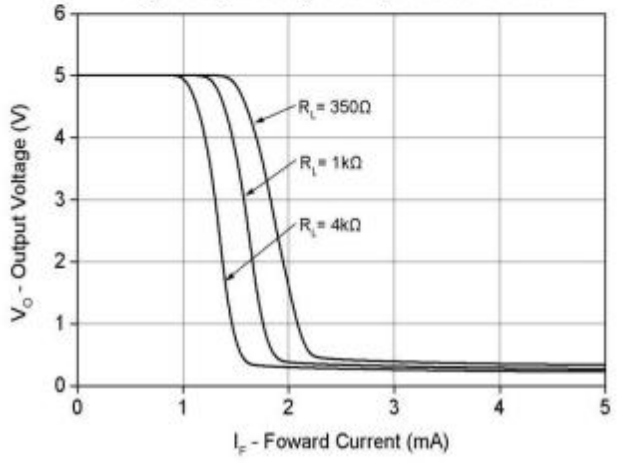
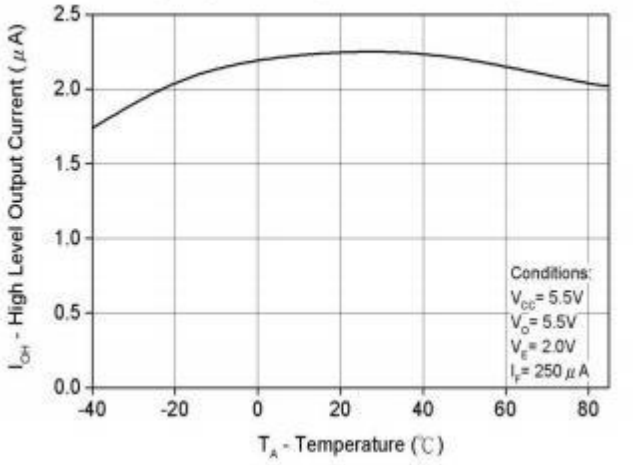


Fig.6 High Level Output Current vs. Temperature



RATING AND CHARACTERISTIC CURVES

Fig.7 Switching Time vs. Forward Current

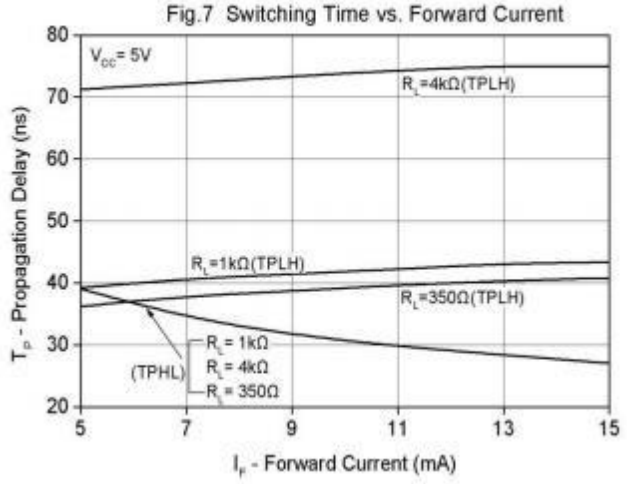


Fig.8 Switching Time vs. Temperature

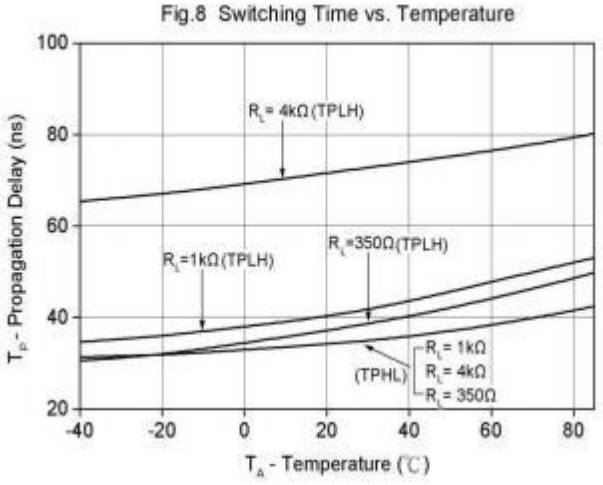


Fig.9 Pulse Width Distortion vs. Temperature

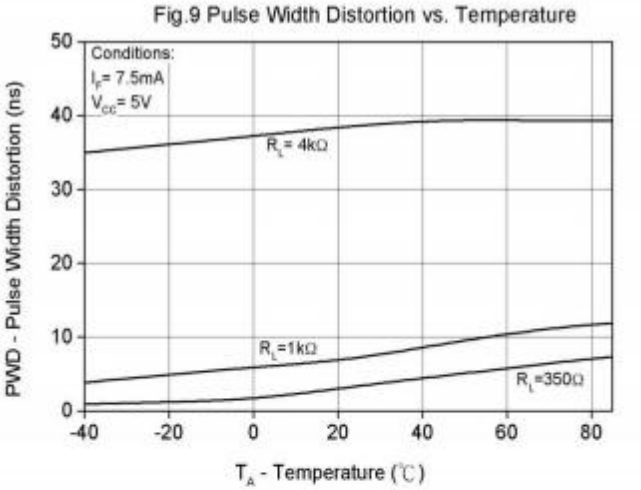


Fig.10 Rise and Fall Time vs. Temperature

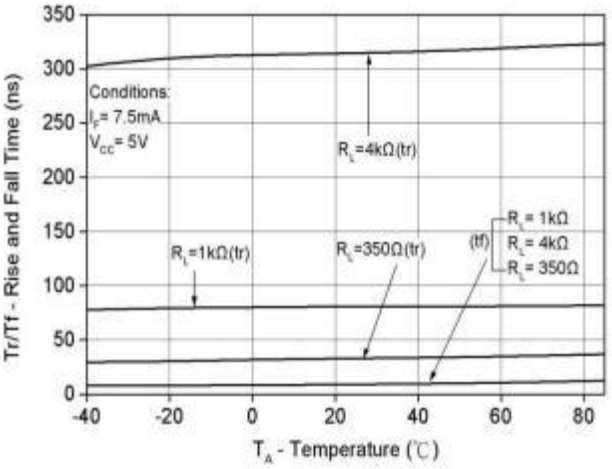
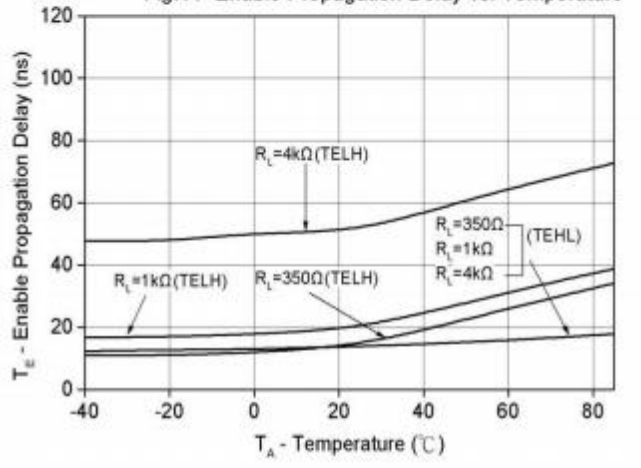


Fig.11 Enable Propagation Delay vs. Temperature



RATING AND CHARACTERISTIC CURVES

Fig. 12 Test circuit and waveforms for tPHL, tPLH, tr, and tf

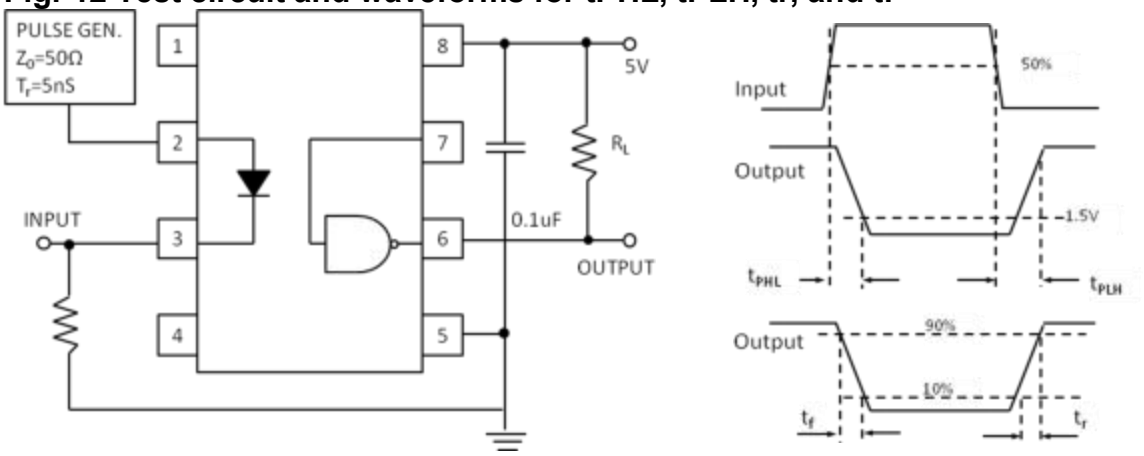


Fig. 13 Test circuit and waveform for tEHLand tEFH

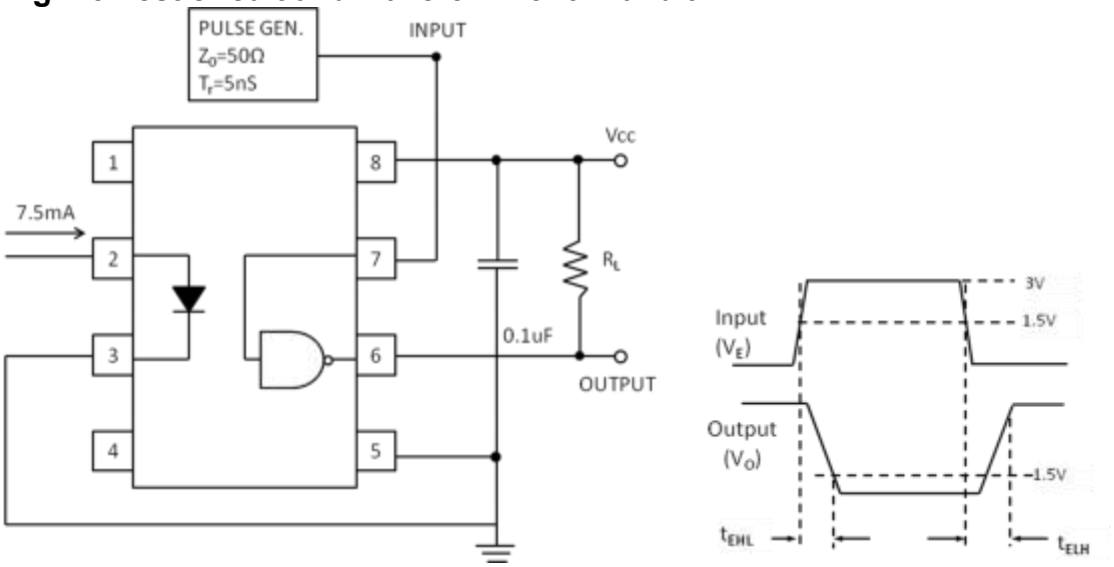
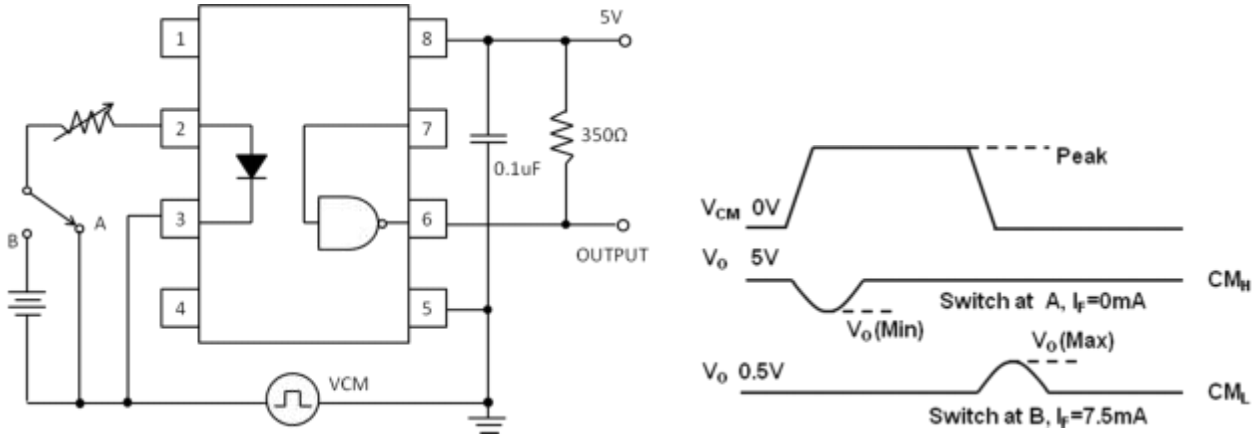
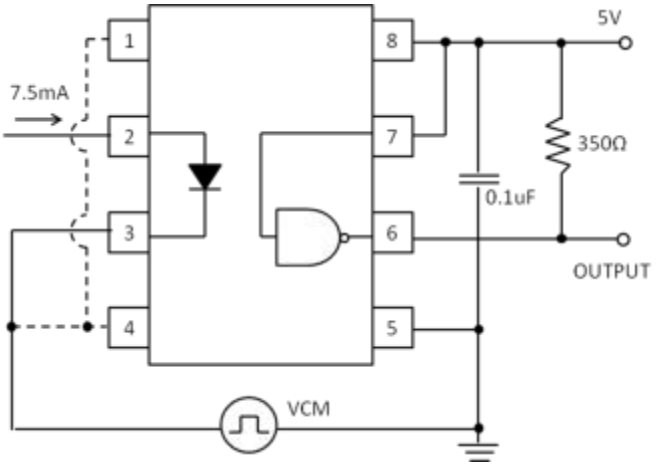


Fig. 14 Test circuit Common mode Transient Immunity



RATING AND CHARACTERISTIC CURVES

Fig. 15 Recommended drive circuit for EF2611 families for high-CMR



Note

*3 The VCC supply must be bypassed by a 0.1μF capacitor or larger. This can be either a ceramic or solid tantalum capacitor with good high frequency characteristic and should be connected as close as possible to the package VCC and GND pins

*4. Enable Input – No pull up resistor required as the device has an internal pull up resistor.

*5. tPLH – Propagation delay is measured from the 3.75mA level on the HIGH to LOW transition of the input current pulse to the 1.5 V level on the LOW to HIGH transition of the output voltage pulse.

*6. tPHL – Propagation delay is measured from the 3.75mA level on the LOW to HIGH transition of the input current pulse to the 1.5 V level on the HIGH to LOW transition of the output voltage pulse.

*7. tr – Rise time is measured from the 90% to the 10% levels on the LOW to HIGH transition of the output pulse.

*8. tf – Fall time is measured from the 10% to the 90% levels on the HIGH to LOW transition of the output pulse.

*9. tEFH – Enable input propagation delay is measured from the 1.5V level on the HIGH to LOW transition of the input voltage pulse to the 1.5V level on the LOW to HIGH transition of the output voltage pulse.

*10. tEHL – Enable input propagation delay is measured from the 1.5V level on the LOW to HIGH transition of the input voltage pulse to the 1.5V level on the HIGH to LOW transition of the output voltage pulse.

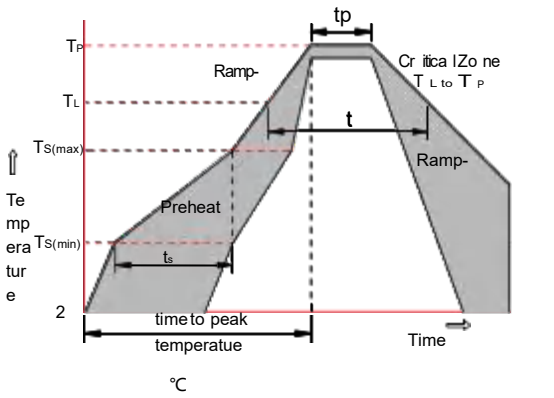
*11 CMH– The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the HIGH state (i.e., VOUT > 2.0V).

*12 CML– The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the LOW output state (i.e., VOUT < 0.8V).

Soldering parameters

Reflow Condition		Pb-Free assembly (see as bellow)
Pre Heat	-Temperature Min ($T_{s(min)}$)	+150℃
	-Temperature Max($T_{s(max)}$)	+200℃
	-Time (Min to Max) (ts)	60-180 secs.
Average ramp up rate (Liquid us Temp (T_L) to peak)		3℃/sec. Max
$T_{s(max)}$ to T_L - Ramp-up Rate		3℃/sec. Max
Reflow	-Temperature(T_L)(Liquid us)	+217℃
	-Temperature(t_L)	60-150 secs.
Peak Temp (T_p)		+260(+0/-5)℃
Time within 5℃ of actual Peak Temp (t_p)		30 secs. Max
Ramp-down Rate		6℃/sec. Max
Time 25℃ to Peak Temp (T_P)		8 min. Max
Do not exceed		+260℃

FIG5: Reflow condition



Package Dimensions & Suggested Pad Layout

DIP -8

