1 FEATURES

- LIN 2.x/ISO 17987-4:2016 (12V)/SAE J2602 compliant
- Baud rate up to 40kBd
- Very low ElectroMagnetic Emission (EME)
- High ElectroMagnetic Immunity (EMI)
- Passive behavior in unpowered state
- Input levels compatible with 3.3V and 5V devices
- Integrated termination resistor for LIN responder applications
- Very low current consumption in Sleep mode, with local and remote wake-up support
- K-line compatible
- Available in SOP8 package and DFN3x3 package
- High ESD robustness: ±6kV according to IEC 61000-4-2 for pins LIN, VBAT and WAKE_N
- Transmit data (TXD) dominant time-out function
- Bus terminal and battery pin protected against transients in the automotive environment (ISO 7637)
- Bus terminal short-circuit proof to battery and ground
- Thermally protected

2 APPLICATIONS

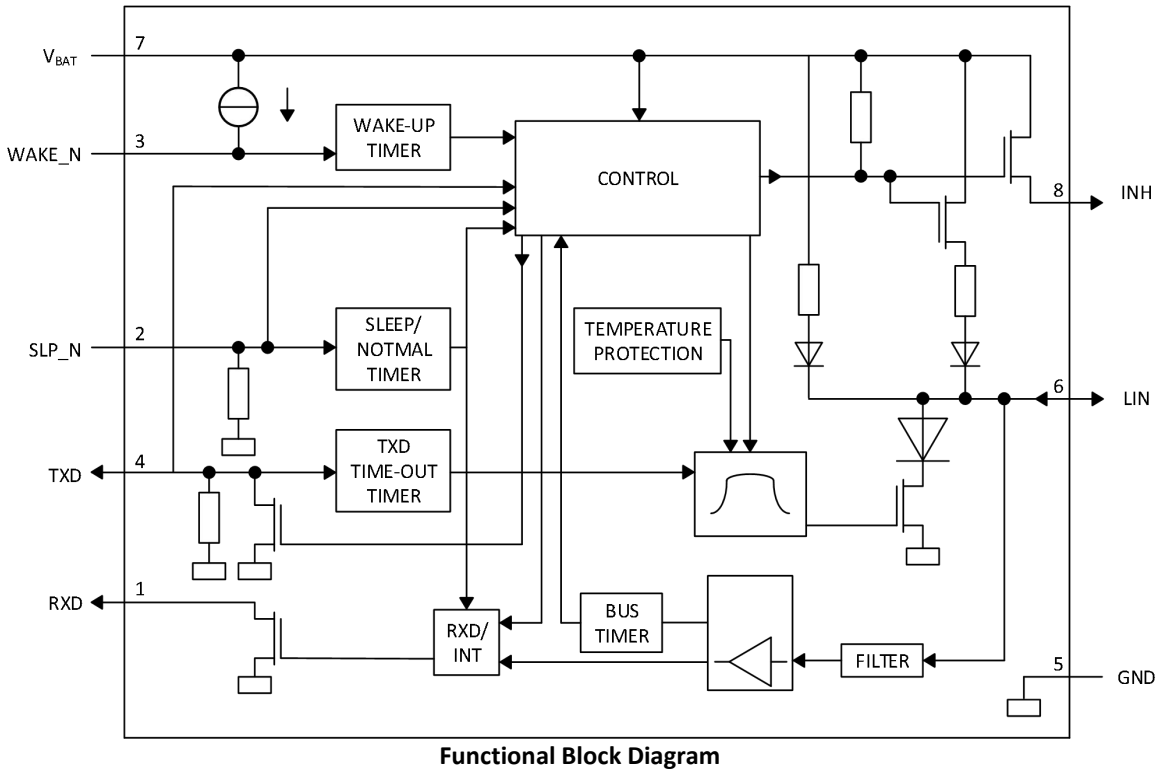
- Industrial automation, control, sensors and drive systems
- Building, security and climate control automation
- Telecom base station status and control

3 DESCRIPTION

The HMT1021T is the interface between the Local Interconnect Network (LIN) commander/responder protocol controller and the physical bus in a LIN. It is primarily intended for invehicle sub-networks using baud rates from 1kBd up to 40kBd and is compliant with LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A, SAE J2602 and ISO 17987-4:2016(12V).

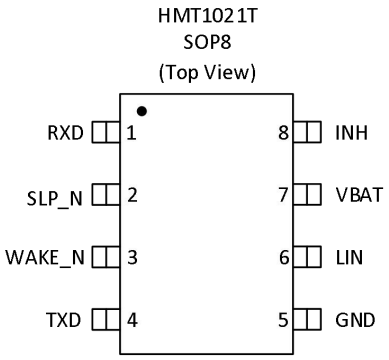
The transmit data stream of the protocol controller at the transmit data input (TXD) is converted by the HMT1021T into a bus signal with optimized slew rate and wave shaping to minimize ElectroMagnetic Emission (EME). The LIN bus output pin is pulled HIGH via an internal termination resistor. For a commander application, an external resistor in series with a diode should be connected between pin INH or pin V_{BAT} and pin LIN. The receiver detects the data stream at the LIN bus input pin and transfers it via pin RXD to the microcontroller.

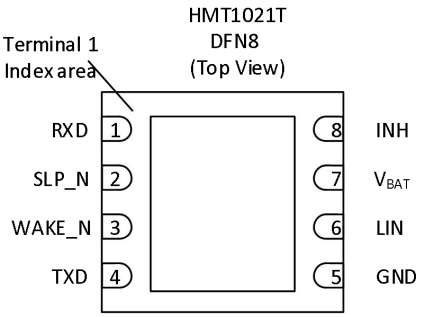
In Sleep mode, the power consumption of the HMT1021T is very low. In failure modes, the power consumption is reduced to a minimum.



Functional Block Diagram

4 Pin Configurations and Functions





Pin Functions

Pins		TYPE[1]	Description
Name	No.		
RXD	1	O	receive data output (open-drain); active LOW after a wake-up event
SLP_N	2	I	sleep control input (active LOW); controls inhibit output; resets wake up source flag on TXD and wake-up request on RXD
WAKE_N	3	I	local wake-up input (active LOW); negative edge triggered
TXD	4	I	transmit data input; active LOW output after a local wake-up event
GND	5[2]	G	ground
LIN	6	AIO	LIN bus line input/output
V_{BAT}	7	P	battery supply voltage
INH	8	O	battery related inhibit output for controlling an external voltage regulator; active HIGH after a wake-up event

(1) I: digital input; O: digital output; AIO: analog input/output; P: power supply; G: ground.
(2) DFN8 package die supply ground is s connected to both the GND pin and the exposed center pad. The GND pin must be soldered to board ground. For enhanced thermal and electrical performance, it is recommended that the exposed center pad also be soldered to board ground.

5 Specifications

5.1 Absolute Maximum Ratings

Symbol	Parameter	Conditions	MIN	MAX	UNIT
V_{BAT}	battery supply voltage[1]	with respect to GND	-0.3	+40	V
V_{TXD}	voltage on pin TXD[1]	I_{TXD} no limitation	-0.3	+6	V
		I_{TXD} < 500µA	-0.3	+7	V
V_{RXD}	voltage on pin RXD[1]	I_{RXD} no limitation	-0.3	+6	V
		I_{RXD} < 500µA	-0.3	+7	V
V_{SLP_N}	voltage on pin SLP_N[1]	I_{SLP_N} no limitation	-0.3	+6	V
		I_{SLP_N} < 500µA	-0.3	+7	V
V_{LIN}	voltage on pin LIN[1]	with respect to GND, V_{BAT} and V_{WAKE_N}	-40	+40	V
V_{WAKE_N}	voltage on pin WAKE_N[1]		-0.3	+40	V
I_{WAKE_N}	current on pin WAKE_N	only relevant if V_{WAKE_N} < V_{GND} - 0.3 current will flow into pin GND	-15	-	mA
V_{INH}	voltage on pin INH[1]		-0.3	V_{BAT}+0.3	V
$I_{O(INH)}$	output current on pin INH		-50	+15	mA
V_{trt}	transient voltage	on pin V_{BAT} via reverse polarity diode/capacitor; on pin LIN via 1nF coupling capacitor[2]			
		pulse 1	-100	-	V
		pulse 2a	-	75	V
		pulse 3a	-150	-	V
		pulse 3b	-	100	V
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 (150pF, 330Ω discharge circuit)[3]			
		on pins WAKE_N, LIN and V_{BAT}	-6	+6	kV
		Human Body Model (HBM)			
		on any pin[4]	-2	+2	kV
		on pins WAKE_N, LIN, V_{BAT} and I_{NH}[5]	-8	+8	kV
		Machine Model (MM); 200pF, 0.75µH, 10 Ω[6]			
		on any pin	-200	+200	V
		Charged Device Model (CDM)[7]			
		on any pin	-750	+750	V
T_{vj}	virtual junction temperature	[8]	-40	+150	°C
T_{stg}	storage temperature	[9]	-55	+150	°C

(1) The device can sustain voltages up to the specified values over the product lifetime, provided applied voltages (including transients) never exceed these values.
(2)Verified by an external test house according to LIN Conformance Test Specification Package for LIN 2.1; parameters for standard pulses defined in ISO 7637.
(3)Verified by an external test house according to LIN Conformance Test Specification Package for LIN 2.1.
(4)According to AEC-Q100-002.
(5)Pins stressed to reference group containing all ground and supply pins, emulating the application circuit (Figure 7). HBM pulse as specified in AECQ100-002 used.
(6)According to AEC-Q100-003.
(7)According to AEC-Q100-011.
(8)In accordance with IEC 60747-1. An alternative definition of virtual junction temperature is: Tvj = Tamb + P × Rth(vj-a), where Rth(vj-a) is a fixed value to be used for the calculation of Tvj. The rating for Tvj limits the allowable combinations of power dissipation (P) and ambient temperature (Tamb).
(9)Tstg in application according to IEC61360-4. For component transport and storage conditions, see instead IEC61760-2

5.2 Thermal characteristics

Symbol	Parameter	Conditions[1]	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	SOP8 package; in free air	93	K/W
		DFN8 package; in free air	54	K/W
Ψ_{j-top}	thermal characterization parameter from junction to top of package	SOP8 package; in free air	13	K/W
		DFN8 package; in free air	7	K/W

[1]According to JEDEC JESD51-2, JESD51-5 and JESD51-7 at natural convection on 2s2p board. Board with two inner copper layers (thickness: 35µm) and thermal via array under the exposed pad connected to the first inner copper layer (thickness: 70µm)

5.3 Static Characteristics

V_{BAT} = 5.5V to 27V; T_{vj} = -40 °C to +150 °C; $R_{L(LIN-VBAT)}$ = 500 Ω; typical values are given at V_{BAT} = 12V unless otherwise specified; all voltages are defined with respect to ground; positive currents flow into the IC.[1].

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Supply Characteristics						
I_{BAT}	battery supply current	Sleep mode; $V_{LIN} = V_{BAT}$; $V_{WAKE\_N} = V_{BAT}$; V_{TXD} = 0V; V_{SLP_N} = 0V	2	7	10	µA
		Standby mode; bus recessive; $V_{INH} = V_{BAT}$; $V_{LIN} = V_{BAT}$; $V_{WAKE\_N} = V_{BAT}$; V_{TXD} = 0V; V_{SLP_N} = 0V	100	180	360	µA
		Standby mode; bus dominant V_{BAT} = 12V; V_{INH} = 12V; V_{LIN} = 0V; V_{WAKE_N} = 12V; V_{TXD} = 0V; V_{SLP_N} = 0V	300	460	1000	µA
		Normal mode; bus recessive $V_{INH} = V_{BAT}$; $V_{LIN} = V_{BAT}$; $V_{WAKE\_N} = V_{BAT}$; V_{TXD} = 5V; V_{SLP_N} = 5V	100	180	400	µA
		Normal mode; bus dominant V_{BAT} = 12V; V_{INH} = 12V; V_{WAKE_N} = 12V; V_{TXD} = 0V; V_{SLP_N} = 5V	0.5	1	2	mA
Power-on reset						
$V_{th(POR)L}$	LOW-level power-on reset threshold voltage	power-on reset	1.5	2.1	2.9	V
$V_{th(POR)H}$	HIGH-level power-on reset threshold voltage		1.8	2.4	3.3	V
$V_{hys(POR)}$	power-on reset hysteresis voltage		0.05	0.3	1	V
$V_{th(VBATL)L}$	LOW-level V_{BAT} LOW threshold voltage		3.1	3.6	3.9	V
$V_{th(VBATL)H}$	HIGH-level V_{BAT} LOW threshold voltage		3.4	3.9	4.2	V
$V_{hys(VBATL)}$	V_{BAT} LOW hysteresis voltage		0.05	0.3	1	V
Pin TXD						
V_{IH}	HIGH-level input voltage		3	-	7	V
V_{IL}	LOW-level input voltage		-0.3	-	+0.8	V
V_{hys}	hysteresis voltage		50	200	400	mV
$R_{PD(TXD)}$	pull-down resistance on pin TXD	V_{TXD} = 5V	140	600	1200	kΩ

5.3 Static Characteristics (Continued)

V_{BAT} = 5.5V to 27V; T_{vj} = -40 °C to +150 °C; $R_{L(LIN-VBAT)}$ = 500Ω; typical values are given at V_{BAT} = 12V unless otherwise specified; all voltages are defined with respect to ground; positive currents flow into the IC.[1].

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{IL}	LOW-level input current	V_{TXD} = 0V	-5	-	+5	µA
I_{OL}	LOW-level output current	local wake-up request Standby mode; V_{WAKE_N} = 0V; V_{LIN} = V_{BAT}; V_{TXD} = 0.4V	1.5	-	-	mA
Pin SLP_N						
V_{IH}	HIGH-level input voltage		2	-	7	V
V_{IL}	LOW-level input voltage		-0.3	-	+0.8	V
V_{hys}	hysteresis voltage		50	300	700	mV
$R_{PD(SLP\_N)}$	pull-down resistance on pin SLP_N	V_{SLP_N} = 5V	140	600	1200	kΩ
I_{IL}	LOW-level input current	V_{SLP_N} = 0V	-5	0	+5	µA
Pin RXD(open-drain)						
I_{OL}	LOW-level output current	Normal mode V_{LIN} = 0V; V_{RXD} = 0.4V	1.5		-	mA
I_{LH}	HIGH-level leakage current	Normal mode V_{LIN} = V_{BAT}; V_{RXD} = 5V	-5	0	+5	µA
Pin WAKE_N						
V_{IH}	HIGH-level input voltage		V_{BAT} - 1	-	V_{BAT} + 0.3	V
V_{IL}	LOW-level input voltage		-0.3	-	V_{BAT} - 3.3	V
$I_{pu(L)}$	LOW-level pull-up current	V_{WAKE_N} = 0V	-30	-12	-1	µA
I_{LH}	HIGH-level leakage current	V_{WAKE_N} = 27V;V_{BAT} = 27V	-5	0	+5	µA
Pin INH						
$R_{sw(VBAT-INH)}$	switch-on resistance between pins V_{BAT} and I_{NH}	Standby; Normal and Poweron modes; I_{INH} =-15mA;V_{BAT} = 12V	-	20	50	Ω
I_{LH}	HIGH-level leakage current	Sleep mode V_{INH} = 27V; V_{BAT} = 27V	-5	0	+5	µA
Pin LIN						
I_{BUS_LIM}	current limitation for driver dominant state	V_{BAT} = 18V; V_{LIN} = 18V; V_{TXD} = 0V	40	-	100	mA
R_{pu}	pull-up resistance	Sleep mode; V_{SLP_N} = 0V	50	160	250	kΩ
$I_{BUS\_PAS\_rec}$	receiver recessive input leakage current	V_{LIN} = 12V; V_{BAT} = 12V; V_{TXD} = 5V	-	-	10	µA
$I_{BUS\_PAS\_dom}$	receiver dominant input leakage current including pull-up resistor	Normal mode; V_{TXD} = 5V; V_{LIN} = 0V; V_{BAT} = 12V	-600	-	-	µA
$V_{SerDiode}$	voltage drop at the serial diode	in pull-up path with R; $I_{SerDiode}$ = 10µA	0.4	-	1.0	V
$I_{BUS\_NO\_GND}$	loss-of-ground bus current	V_{BAT} = 27V; V_{LIN} = 0V	-750	-	+10	µA
$I_{BUS\_NO\_BAT}$	loss-of-battery bus current	V_{BAT} = 0V; V_{LIN} = 27V	-	-	1	µA
V_{BUSdom}	receiver dominant state		-	-	0.4V_{BAT}	V
V_{BUSrec}	receiver recessive state		0.6V_{BAT}	-	-	V
V_{BUS_CNT}	receiver center voltage	V_{BUS_CNT} = (V_{BUSrec} + V_{BUSdom}) /2	0.475V_{BAT}	0.5V_{BAT}	0.565V_{BAT}	V
V_{HYS}	receiver hysteresis voltage	V_{HYS} = V_{BUSrec} - V_{BUSdom}	-	-	0.175V_{BAT}	V
R_{res}	responder resistance	connected between pins LIN and V_{BAT}; V_{LIN} = 0V; V_{BAT} = 12V	20	30	47	kΩ
C_{LIN}	capacitance on pin LIN	[2]	-	-	30	pF

5.3 Static Characteristics (Continued)

V_{BAT} = 5.5V to 27V; T_{vj} = -40 °C to +150 °C; $R_{L(LIN-VBAT)}$ = 500 Ω; typical values are given at V_{BAT} = 12V unless otherwise specified; all voltages are defined with respect to ground; positive currents flow into the IC.[1].

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{o(dom)}$	dominant output voltage	Normal mode; V_{TXD} = 0V; V_{BAT} = 7.0V	-	-	1.4	V
		Normal mode; V_{TXD} = 0V; V_{BAT} = 18V	-	-	2.0	V
Thermal shutdown						
$T_{j(sd)}$	shutdown junction temperature	[2]	150	175	200	°C

5.4 Dynamic characteristics

V_{BAT} = 5.5V to 18V; Tvj = -40 °C to +150 °C; $R_{L(LIN-VBAT)}$ = 500Ω; typical values are given at V_{BAT} = 12V, see Figure 6,unless otherwise specified; all voltages are defined with respect to ground.[1].

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Duty cycles						
δ1	duty cycle 1	$V_{th(rec)(max)}$ = 0.744 × V_{BAT}; $V_{th(dom)(max)}$ = 0.581 × V_{BAT}; t_{bit} = 50µs; V_{BAT}= 7V to 18V [2][3][4][5]	0.396	-	-	
		$V_{th(rec)(max)}$ = 0.76 × V_{BAT}; $V_{th(dom)(max)}$ = 0.593 × V_{BAT}; t_{bit} = 50µs; V_{BAT} = 5.5V to 7.0V [2][3][4][5]	0.396	-	-	
δ2	duty cycle 2	$V_{th(rec)(min)}$ = 0.422 × V_{BAT}; $V_{th(dom)(min)}$ = 0.284 × V_{BAT}; t_{bit} = 50µs; V_{BAT} = 7.6V to 18V [2][4][6][5]	-	-	0.581	
		$V_{th(rec)(min)}$ = 0.41 × V_{BAT}; $V_{th(dom)(min)}$ = 0.275 × V_{BAT}; t_{bit} = 50µs; V_{BAT} = 6.1V to 7.6V [2][4][6][5]	-	-	0.581	
δ3	duty cycle 3	$V_{th(rec)(max)}$ = 0.778 × V_{BAT}; $V_{th(dom)(max)}$ = 0.616 × V_{BAT}; t_{bit} = 96µs; V_{BAT}= 7V to 18V [3][4][5]	0.417	-	-	
		$V_{th(rec)(max)}$ = 0.797 × V_{BAT}; $V_{th(dom)(max)}$ = 0.630 × V_{BAT}; t_{bit} = 96µs; V_{BAT} = 5.5V to 7V [3][4][5]	0.417	-	-	
δ4	duty cycle 4	$V_{th(rec)(min)}$ = 0.389 × V_{BAT}; $V_{th(dom)(min)}$ = 0.251 × V_{BAT}; t_{bit} = 96µs; V_{BAT} = 7.6V to 18V[4][6][5]	-	-	0.590	
		$V_{th(rec)(min)}$ = 0.378 × V_{BAT}; $V_{th(dom)(min)}$ = 0.242 × V_{BAT}; t_{bit} = 96µs; V_{BAT} = 6.1V to 7.6V [4][6][5]	-	-	0.590	
Timing characteristics						
t_f	fall time	[2][4]	-	-	22.5	µs
t_r	rise time	[2][4]	-	-	22.5	µs
$\Delta t_{(r-f)}$	difference between rise and fall time	V_{BAT} = 7.3V[2][4]	-5	-	+5	µs

5.4 Dynamic characteristics (Continued)

V_{BAT} = 5.5V to 18V; Tvj = -40 °C to +150 °C; $R_{L(LIN-VBAT)}$ = 500Ω; typical values are given at V_{BAT} = 12V, see Figure 4, unless otherwise specified; all voltages are defined with respect to ground.[1].

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t_{tx_pd}	transmitter propagation delay	rising and falling[2]	-	-	6	µs
t_{tx_sym}	transmitter propagation delay symmetry	[2]	-2.5	-	+2.5	µs
t_{rx_pd}	receiver propagation delay	rising and falling[7]	-	-	6	µs
t_{rx_sym}	receiver propagation delay symmetry	[7]	-2	-	+2	µs
$t_{wake(dom)LIN}$	LIN dominant wake-up time	Sleep mode[8]	30	80	150	µs
$t_{wake(dom)WAKE\_N}$	dominant wake-up time on pin WAKE_N	Sleep mode[9]	7	30	50	µs
$t_{gotonorm}$	go to normal time	time period for mode change from Sleep, Power-on or Standby mode to Normal mode[10]	2	5	10	µs
$t_{init(norm)}$	normal mode initialization time	[11]	5	-	20	µs
$t_{gotosleep}$	go to sleep time	time period for mode change from Normal mode to Sleep mode[10]	2	5	10	µs
$t_{to(dom)TXD}$	TXD dominant time-out time	V_{TXD} = 0V[12]	27	55	90	ms

[1] All parameters are guaranteed over the virtual junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage range.

[2] Not applicable for the /10 or A variants of the HMT1021T.

[3] $\delta 1, \delta 3 = \frac{t_{bus[rec][\min]}}{2 \times t_{bit}}$. Variable $t_{bus(rec)(min)}$ is illustrated in the LIN timing diagram in Figure 4.

[4] Bus load conditions are: C_{BUS} = 1nF and RBUS = 1kΩ; C_{BUS} = 6.8nF and RBUS = 660Ω; CBUS = 10nF and RBUS = 500Ω.

[5] For VBAT > 18V the LIN transmitter might be suppressed. If TXD is HIGH then the LIN transmitter output is recessive.

[6] $\delta 2, \delta 4 = \frac{t_{bus[rec][\max]}}{2 \times t_{bit}}$. Variable $t_{bus(rec)(max)}$ is illustrated in the LIN timing diagram in Figure 4.

[7] Load condition pin RXD: CRXD = 20pF and RRXD = 2.4kΩ.

[8] A falling edge on pin LIN, followed by LOW level of least tmax, followed by a rising edge on pin LIN is guaranteed to trigger a remote wake-up (see Section 6.6. A LOW level of less than t_{min} will not trigger a wake-up event).

[9] A falling edge on pin WAKE_N, followed by a LOW level of least t_{max} is guaranteed to trigger a local wake-up (Section 6.6). A LOW level of less than t_{min} will not trigger a wake-up event.

[10] Mode change is guaranteed to have been completed after t_{max} and will not be completed before t_{min}.

[11] LIN transmit and receive functions are guaranteed to have been enabled after t_{max} and will not be enabled before t_{min}.

[12] Time-out is guaranteed to have been triggered after t_{max} and will not be triggered before t_{min}.

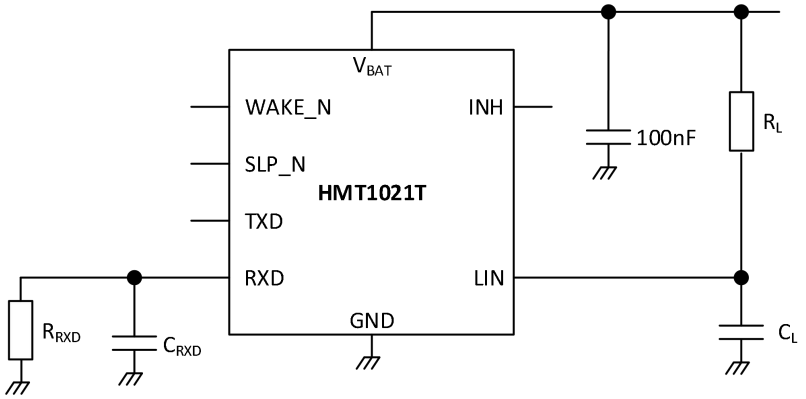


Figure 3. Timing test circuit for LIN transceiver

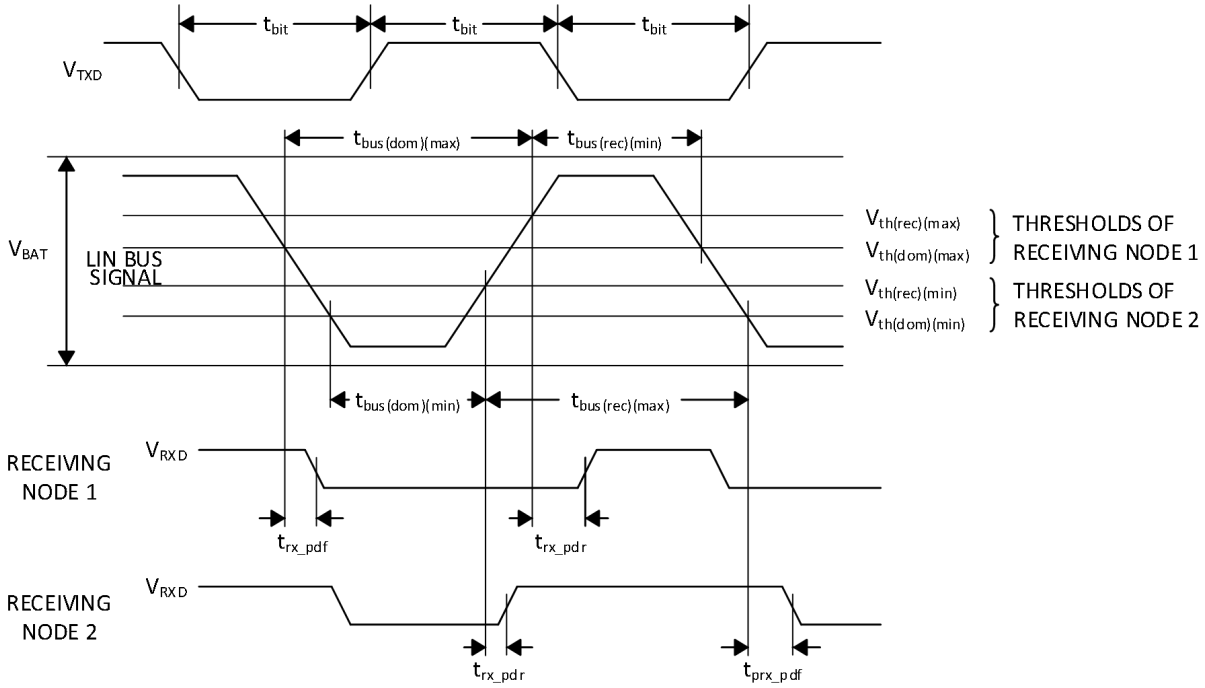


Figure 4. Timing diagram LIN transceiver

6 Functional Description

Overview

The HMT1021T is the interface between the LIN commander/responder protocol controller and the physical bus in a Local Interconnect Network (LIN). The HMT1021T is LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A, SAE J2602 and ISO 17987-4:2016 (12V) compliant and provides optimum ElectroMagnetic Compatibility (EMC) performance due to wave shaping of the LIN output.

The LIN physical layer is independent of higher OSI model layers (e.g., the LIN protocol). Consequently, nodes containing an ISO 17987-compliant physical layer can be combined, without restriction, with LIN physical layer nodes that comply with earlier revisions (LIN 1.0, LIN 1.1, LIN 1.2, LIN 1.3, LIN 2.0, LIN 2.1, LIN 2.2 and LIN 2.2A).

6.1 Functional Block Diagram

The HMT1021T supports modes for normal operation (Normal mode), power-up (Power-on mode) and very-low-power operation (Sleep mode). An intermediate wake-up mode between Sleep and Normal modes is also supported (Standby mode). Figure 5 shows the state diagram.

Mode	SLP_N	TXD(output)	RXD	INH	Transmitter	Remarks
Sleep mode	0	weak pull-down	floating	floating	off	no wake-up request detected
Standby mode[1]	0	weak pull-down if remote wake-up; strong pull-down if local wake-up[2]	LOW[3]	HIGH	off	wake-up request detected; in this mode The microcontroller can read the wakeup source: remote or local wake-up
Normal mode	1	HIGH: recessive state LOW: dominant state	HIGH: recessive state LOW: dominant state	HIGH	Normal mode	[2][3][4]
Power-on mode	0	weak pull-down	floating	HIGH	off	[5]

[1] Standby mode is entered automatically upon any local or remote wake-up event during Sleep mode. Pin INH and the 30kΩ termination resistor at pin LIN are switched on.
[2] The internal wake-up source flag (set if a local wake-up did occur and fed to pin TXD) will be reset after a positive edge on pin SLP_N.
[3] The wake-up interrupt (on pin RXD) is released after a positive edge on pin SLP_N.
[4] Normal mode is entered after a positive edge on SLP_N. As long as TXD is LOW, the transmitter is off. In the event of a short-circuit to ground on pin TXD, the transmitter will be disabled.
[5] Power-on mode is entered after switching on V_{BAT}

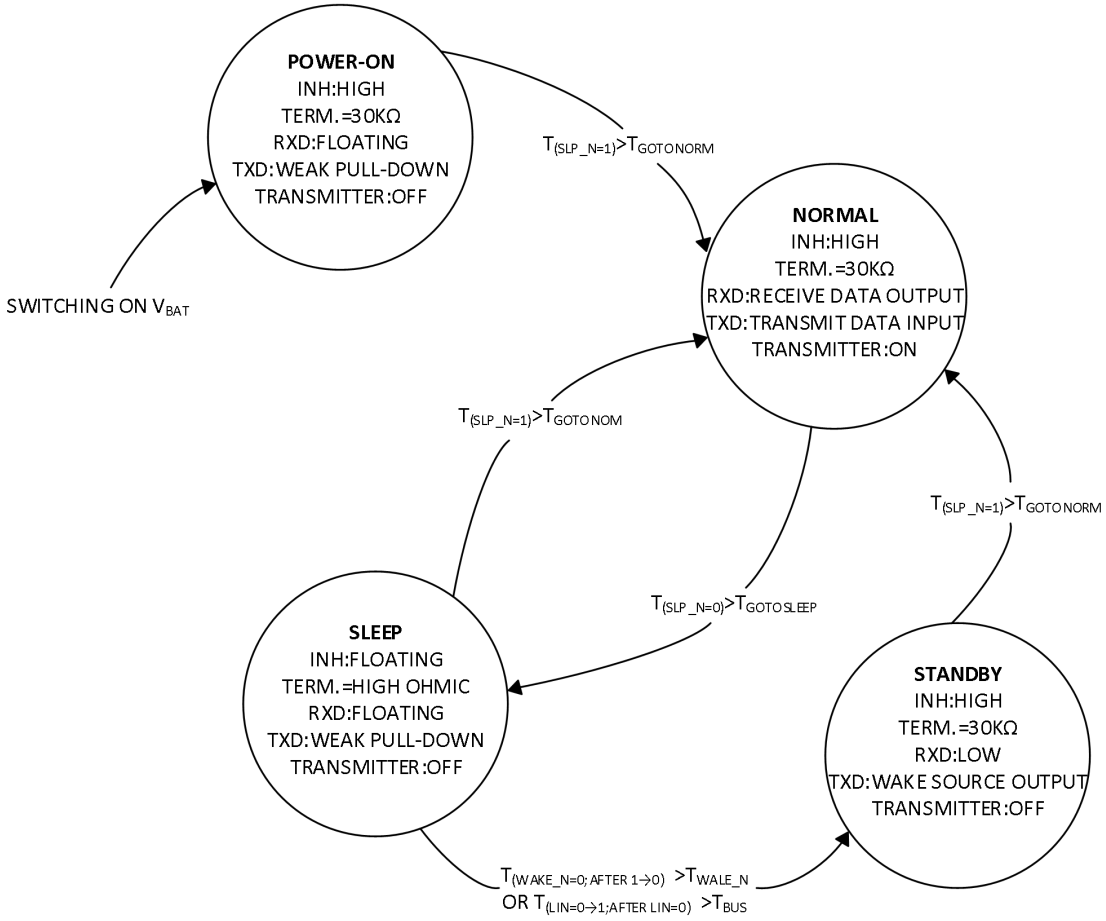


Figure 5. State diagram

6.2 Sleep mode

This mode is the most power-saving mode of the HMT1021T. Despite its extreme low current consumption, the HMT1021T can still be woken up remotely via pin LIN, or woken up locally via pin WAKE_N, or activated directly via pin SLP_N. Filters at the inputs of the receiver (LIN), of pin WAKE_N and of pin SLP_N prevent unwanted wake-up events due to automotive transients or EMI. All wake-up events must be maintained for a certain time period ($t_{wake(dom)LIN}$, $t_{wake(dom)WAKE\_N}$ and $t_{gotonorm}$).

Sleep mode is initiated by a falling edge on pin SLP_N in Normal mode. To enter Sleep mode successfully (INH becomes floating), the sleep command (pin SLP_N = LOW) must be maintained for at least $t_{gotosleep.}$

In Sleep mode the internal responder termination between pins LIN and V_{BAT} is disabled to minimize the power dissipation in the event that pin LIN is short-circuited to ground. Only a weak pull-up between pins LIN and V_{BAT} is present.

Sleep mode can be activated independently from the actual level on pin LIN, pin TXD or pin WAKE_N. This guarantees that the lowest power consumption is achievable even in case of a continuous dominant level on pin LIN or a continuous LOW on pin WAKE_N.

When V_{BAT} drops below the power-on-reset threshold $V_{th(POR)L}$, the HMT1021T enters Sleep mode.

6.3 Standby mode

Standby mode is entered automatically whenever a local or remote wake-up occurs while the HMT1021T is in Sleep mode. These wake-up events activate pin INH and enable the responder termination resistor at the pin LIN. As a result of the HIGH condition on pin INH the voltage regulator and the microcontroller can be activated.Standby mode is signalled by a LOW-level on pin RXD which can be used as an interrupt for the microcontroller.

In Standby mode (pin SLP_N is still LOW), the condition of pin TXD (weak pull-down or strong pull-down) indicates the wake-up source: weak pull-down for a remote wake-up request and strong pull-down for a local wake-up request.

Setting pin SLP_N HIGH during Standby mode results in the following events:

• An immediate reset of the wake-up source flag; thus releasing the possible strong pulldown at pin TXD before the actual mode change (after $t_{gotonorm}$) is performed

• A change into Normal mode if the HIGH level on pin SLP_N has been maintained for a certain time period ($t_{gotonorm}$)

• An immediate reset of the wake-up request signal on pin RXD

6.4 Normal mode

In Normal mode the HMT1021T is able to transmit and receive data via the LIN bus line.The receiver detects the data stream at the LIN bus input pin and transfers it via pin RXD to the microcontroller (see Figure 1): HIGH at a recessive level and LOW at a dominant level on the bus. The receiver has a supply-voltage related threshold with hysteresis and an integrated filter to suppress bus line noise. The transmit data stream of the protocol controller at the TXD input is converted by the transmitter into a bus signal with optimized slew rate and wave shaping to minimize EME. The LIN bus output pin is pulled HIGH via an internal responder termination resistor. For a commander application an external resistor in series with a diode should be connected between pin INH or V_{BAT} on one side and pin LIN on the other side (see Figure 7).

When in Sleep, Standby or Power-up mode, the HMT1021T enters Normal mode whenever a HIGH level on pin SLP_N is maintained for a time of at least $t_{gotonorm}$. The LIN transmit and receive functions are enabled after an initialization time, $t_{init(norm)}$.

The HMT1021T switches to Sleep mode in case of a LOW-level on pin SLP_N, maintained for a time of at least $t_{gotosleep}$.

6.5 Wake-up

When V_{BAT} exceeds the power-on-reset threshold voltage $V_{th(POR)H}$, the HMT1021T enters Power-on mode. Though the HMT1021T is powered-up and INH is HIGH, both the transmitter and receiver are still inactive.

If SLP_N = 1 for t > $t_{gotonorm}$, the HMT1021T enters Normal mode.

There are three ways to wake-up a HMT1021T which is in Sleep mode:

1. Remote wake-up via a dominant bus state of at least $t_{wake(dom)LIN}$
2. Local wake-up via a negative edge at pin WAKE_N
3. Mode change (pin SLP_N is HIGH) from Sleep mode to Normal mode.

6.6 Remote and local wake-up

A falling edge at pin LIN followed by a LOW level maintained for a certain time period ($t_{wake(dom)LIN}$) and a rising edge at pin LIN respectively (see Figure 6) results in a remote wake-up. It should be noted that the time period $t_{wake(dom)LIN}$ is measured either in Normal mode while TXD is HIGH, or in Sleep mode irrespective of the status of pin TXD.A falling edge at pin WAKE_N followed by a LOW level maintained for a certain time period ($t_{wake(dom)WAKE\_N}$) results in a local wake-up. The pin WAKE_N provides an internal pull-up towards pin V_{BAT}. In order to prevent EMI issues, it is recommended to connect an unused pin WAKE_N to pin V_{BAT}.
After a local or remote wake-up, pin INH is activated (it goes HIGH) and the internal responder termination resistor is switched on. The wake-up request is indicated by a LOW active wake-up request signal on pin RXD to interrupt the microcontroller.

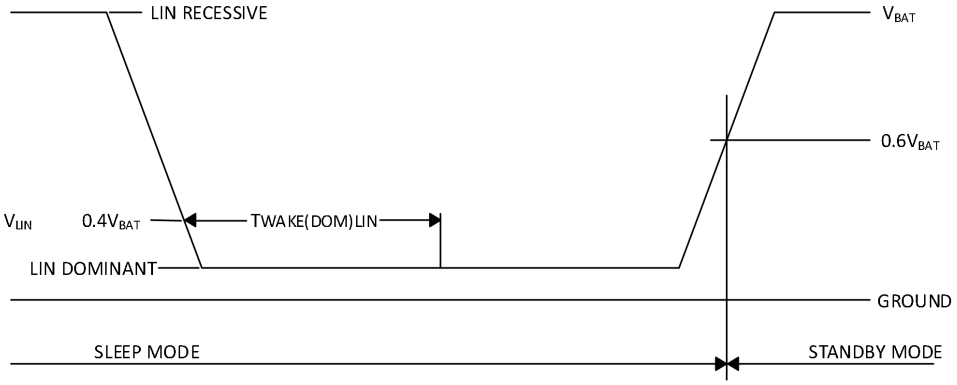


Figure 6. Remote wake-up behavior

6.7 Wake-up via mode transition

It is also possible to set pin INH HIGH with a mode transition towards Normal mode via pin SLP_N. This is useful for applications with a continuously powered microcontroller.

6.8 Wake-up source recognition

The HMT1021T can distinguish between a local wake-up request on pin WAKE_N and a remote wake-up request via a dominant bus state. A local wake-up request sets the wake-up source flag. The wake-up source can be read on pin TXD in the Standby mode. If an external pull-up resistor on pin TXD to the power supply voltage of the microcontroller has been added, a HIGH level indicates a remote wake-up request (weak pull-down at pin TXD) and a LOW level indicates a local wake-up request (strong pulldown at pin TXD; much stronger than the external pull-up resistor).The wake-up request flag (signalled on pin RXD) as well as the wake-up source flag (signalled on pin TXD) are reset immediately after the microcontroller sets pin SLP_N HIGH.

6.9 TXD dominant time-out function

A TXD dominant time-out timer circuit prevents the bus line from being driven to a permanent dominant state (blocking all network communication) if pin TXD is forced permanently LOW by a hardware and/or software application failure. The timer is triggered by a negative edge on pin TXD. If the duration of the LOW-level on pin TXD exceeds the internal timer value ($t_{to(dom)TXD}$), the transmitter is disabled, driving the bus line into a recessive state. The timer is reset by a positive edge on pin TXD.

6.10 Fail-safe features

Pin TXD provides a pull-down to GND in order to force a predefined level on input pin TXD in case the pin TXD is unsupplied.
Pin SLP_N provides a pull-down to GND in order to force the transceiver into Sleep mode in case the pin SLP_N is unsupplied.
Pin RXD is set floating in case of lost power supply on pin V_{BAT}.
The current of the transmitter output stage is limited in order to protect the transmitter against short circuit to pins V_{BAT} or GND.
A loss of power (pins V_{BAT} and GND) has no impact on the bus line and the microcontroller. There are no reverse currents from the bus. The LIN transceiver can be disconnected from the power supply without influencing the LIN bus.
The output driver at pin LIN is protected against overtemperature conditions. If the junction temperature exceeds the shutdown junction temperature $T_{j(sd)}$, the thermal protection circuit disables the output driver. The driver is enabled again when the junction temperature has dropped below $T_{j(sd)}$ and a recessive level is present at pin TXD.
If V_{BAT} drops below $V_{th(VBATL)L}$, a protection circuit disables the output driver. The driver is enabled again when V_{BAT} > $V_{th(VBATL)H}$ and a recessive level is present at pin TXD.

7 Application information

The minimum external circuitry needed with the HMT1021T is shown in Figure 7.

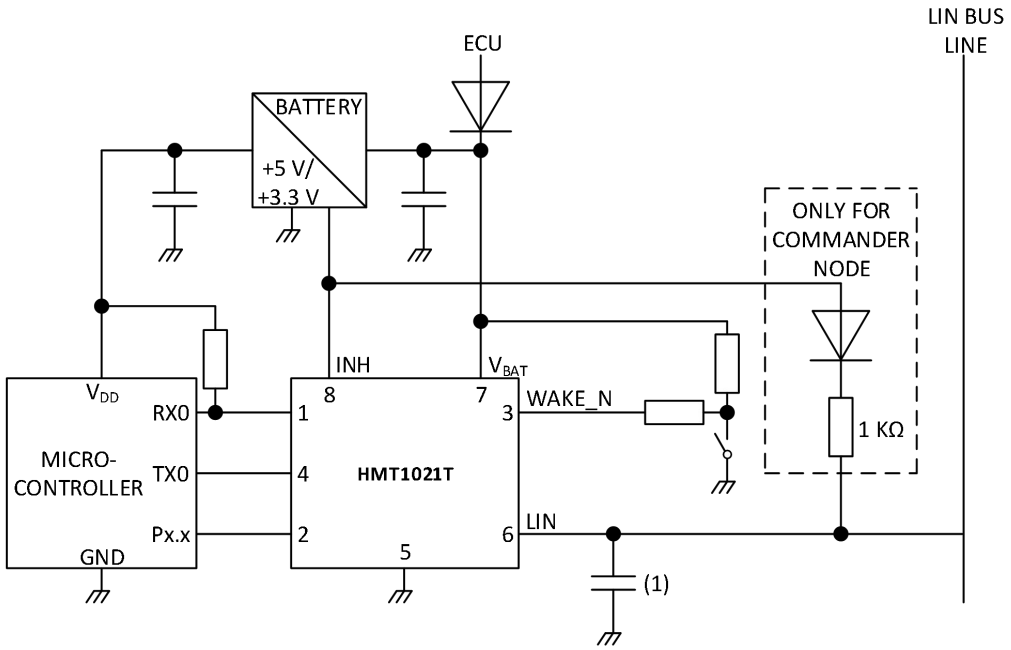


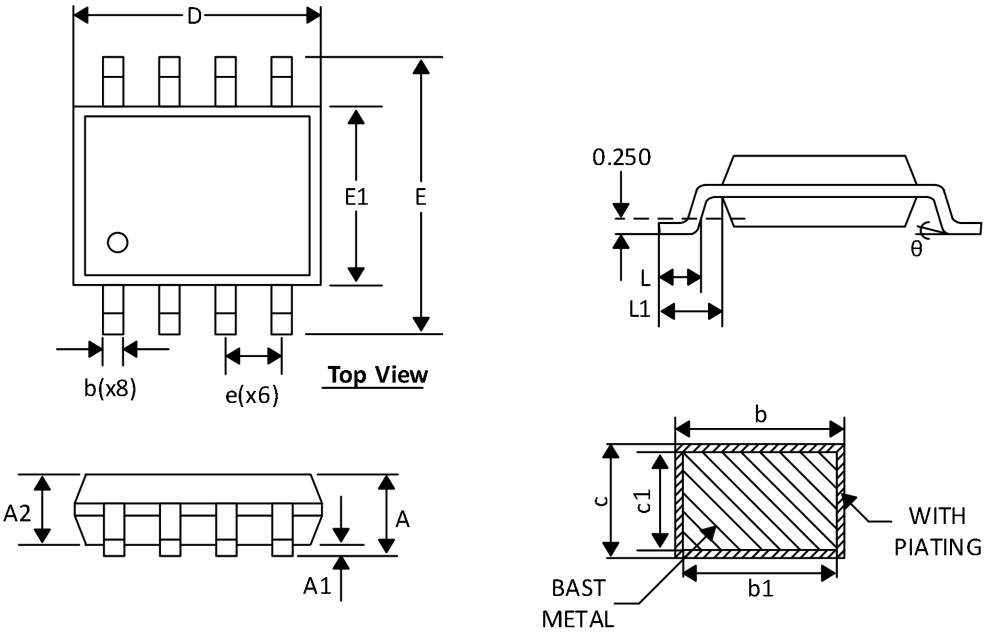
Figure 7. Typical application of the HMT1021T

8 Quality information

This product has been qualified in accordance with the Automotive Electronics Council(AEC) standard Q100 Rev-G - Failure mechanism based stress test qualification for integrated circuits, and is suitable for use in automotive applications.

PACKAGE DIMENSION

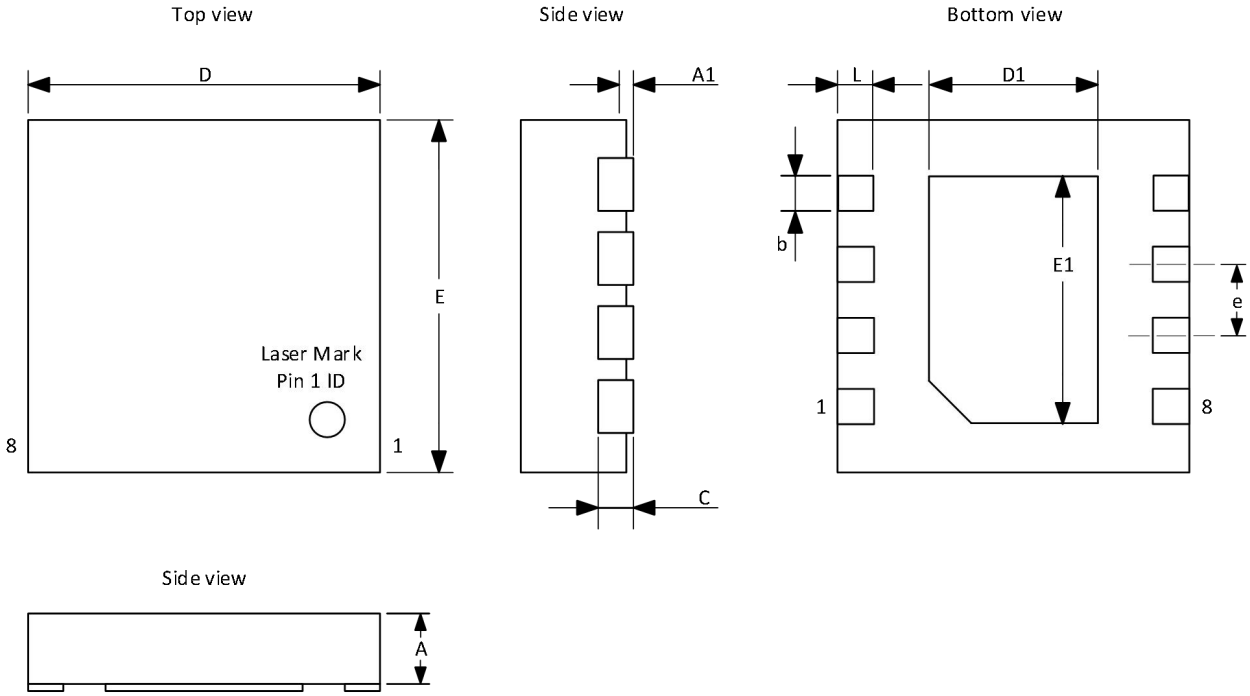
SOP8



SYMBOLS	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.75
A1	0.10	0.175	0.25
A2	1.30	1.40	1.50
b	0.31	-	0.50
b1	0.30	0.40	0.45
c	0.20	-	0.24
c1	0.19	0.203	0.21
D	4.80	-	5.00
E	5.80	6.00	6.20
E1	3.80	-	4.00
e	1.27 BSC		
L	0.40	-	0.80
L1	1.05 REF		
θ	0°	-	8°

PACKAGE DIMENSION

DFN8-EP(3x3)



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	-	0.05
b	0.23	0.28	0.33
c		0.203REF	
D	2.925	3.00	3.075
D1	1.40	1.50	1.60
E	2.925	3.00	3.075
E1	2.20	2.30	2.40
e		0.650BSC	
L	0.25	0.30	0.35

ORDER INFORMATION

Order number	Package	Marking information	Operation Temperature Range	MSL Grade	Ship, Quantity	Green
HMT1021T	SOP8	HMT1021T	-40 to 125°C	3	T&R, 2500	Rohs
HMT1021TK	DFN8	HMT1021TK	-40 to 125°C	3	T&R, 3000	Rohs