



钜地半导体
Tudi Semiconductor

Product Specification

TUDI-SN65/75HVD10/11/12

3.3-V RS-485 TRANSCEIVERS

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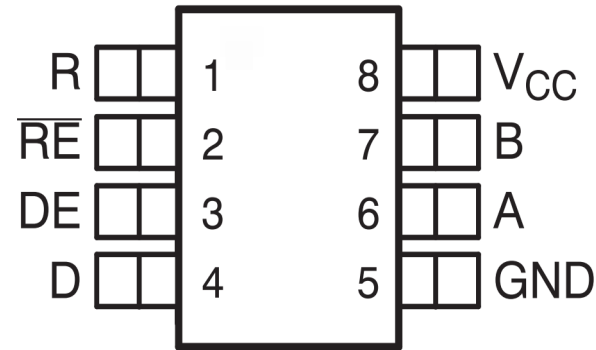
**semiconductor device
manufacturer**

- Design
- research and development
- production
- and sales



FEATURES

- Operates With a 3.3-V Supply
- Bus-Pin ESD Protection Exceeds 16 kV HBM
- 1/8 Unit-Load Option Available (Up to 256 Nodes on the Bus)
- Optional Driver Output Transition Times for Signaling Rates of 1 Mbps, 10 Mbps, and 32 Mbps
- Meets or Exceeds the Requirements of ANSI TIA/EIA-485-A
- Bus-Pin Short Circuit Protection From -7 V to 12 V
- Low-Current Standby Mode . . . $1\text{ }\mu\text{A}$ Typical
- Open-Circuit, Idle-Bus, and Shorted-Bus Failsafe Receiver
- Thermal Shutdown Protection
- Glitch-Free Power-Up and Power-Down Protection for Hot-Plugging Applications



Pin Diagram

DESCRIPTION

The SN65HVD10, SN75HVD10, SN65HVD11, SN75HVD11, SN65HVD12, and SN75HVD12 combine a 3-state differential line driver and differential input line receiver that operate with a single 3.3-V power supply. They are designed for balanced transmission lines and meet or exceed ANSI standard TIA/EIA-485-A and ISO 8482:1993. These differential bus transceivers are monolithic integrated circuits designed for bidirectional data communication on multipoint bus-transmission lines. The drivers and receivers have active-high and active-low enables respectively, that can be externally connected together to function as direction control. Very low device standby supply current can be achieved by disabling the driver and the receiver. The driver differential outputs and receiver differential inputs connect internally to form a differential input/output (I/O) bus port that is designed to offer minimum loading to the bus whenever the driver is disabled or $V_{CC} = 0$. These parts feature wide positive and negative common-mode voltage ranges, making them suitable for party-line applications.

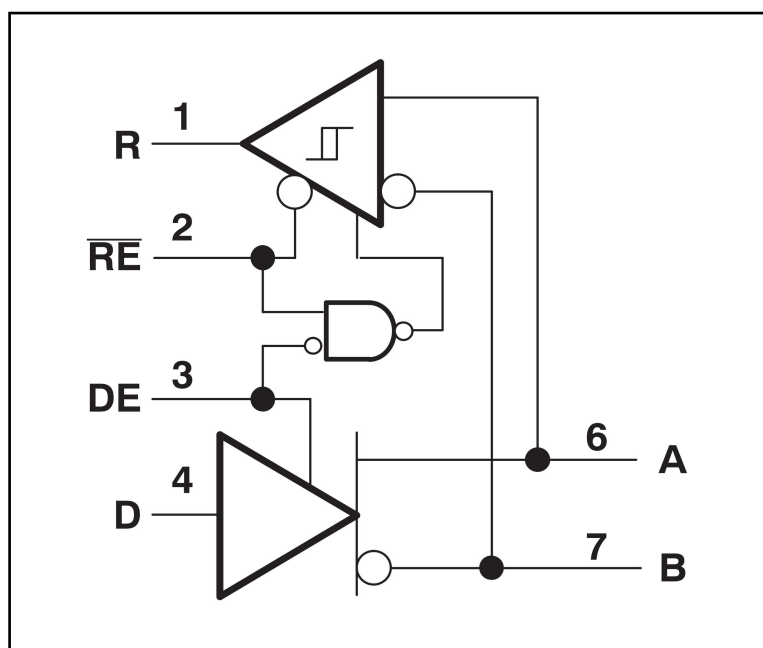
APPLICATIONS

- Digital Motor Control
- Utility Meters
- Chassis-to-Chassis Interconnects
- Electronic Security Stations
- Industrial Process Control
- Building Automation
- Point-of-Sale (POS) Terminals and Networks

Table 1.Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
A	6	Bus input/output	Driver output or receiver input (complementary to B)
B	7	Bus input/output	Driver output or receiver input(complementary to A)
D	4	Digital input	Driver data input
DE	3	Digital input	Active-high driver enable
GND	5	Reference potential	Local device ground
R	1	Digital output	Receive data output
RE	2	Digital input	Active-low receiver enable
Vcc	8	Supply	3-V to 3.6-V supply

Simplified Schematic





ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted ^{(1) (2)}

			UNIT
V _{cc}	Supply voltage range		-0.3 V to 6V
	Voltage range at A or B		-9 V to 14V
	Input voltage range at D,DE,R or RE		-0.5V to V _{cc} +0.5V
	Voltage input range,transient pulse,A and B,through 100 Ω,see Figure 11		-50 V to 50V
I _o	Receiver output current		-11 mA to 11 mA
Electrostaticdischarge	Human body model ⁽³⁾	A,B,and GND	±16kV
		All pins	±4kV
	Charged-device model ⁽⁴⁾	All pins charge	±1 kV
Continuous total power dissipation			See Dissipation Rating Table
Electrical Fast Transient/Burst ⁽⁵⁾		A,B,and GND	±4 kV
T _J Junction temperature			170℃

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

(3) Tested in accordance with JEDEC Standard 22, Test Method A114-A and IEC 60749-26.

(4) Tested in accordance with JEDEC Standard 22, Test Method C101.

(5) Tested in accordance with IEC 61000-4-4.



PACKAGE DISSIPATION RATINGS

PACKAGE	TA≤25℃ POWER RATING	DERATING FACTOR ⁽¹⁾ ABOVE TA=25℃	TA=70℃ POWER RATING	TA=85℃ POWER RATING	TA=125℃ POWER RATING
D ⁽²⁾	597 mW	4.97 mW/℃	373 mW	298 mW	100 mW
D ⁽³⁾	990 mW	8.26 mW/℃	620 mW	496 mW	165 mW
P	1290 mW	10.75 mW/℃	806 mW	645 mW	215 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

(2) Tested in accordance with the Low-K thermal metric definitions of EIA/JESD51-3.

(3) Tested in accordance with the High-K thermal metric definitions of EIA/JESD51-7

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range unless otherwise noted

			MIN	NOM	MAX	UNIT
V _{CC} Supply voltage			3		3.6	V
V _I or V _{IC} Voltage at any bus terminal (separately or common mode)			-7 ⁽¹⁾		12	
V _{IH} High-level input voltage	D,DE,RE		2		V _{CC}	
V _{IL} Low-level input voltage	D,DE,RE		0		0.8	
V _{ID} Differential input voltage	Figure 7		-12		12	
I _{OH} High-level output current	Driver		-60			mA
	Receiver		-8			
I _{OL} Low-level output current	Driver				60	mA
	Receiver				8	
R _L Differential load resistance			54	60		Ω
C _L Differential load capacitance				50		pF
Signaling rate		HVD10			32	Mbps
		HVD11			10	
		HVD12			1	
T _J ⁽²⁾ Junction temperature					145	°C



- (1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.
(2) See thermal characteristics table for information regarding this specification.

THERMAL CHARACTERISTICS

over operating free-air temperature range unless otherwise noted ⁽¹⁾

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
θ_{JA} Junction-to-ambient thermal resistance ⁽²⁾	High-K board ⁽³⁾ , No airflow	D pkg		121		$^{\circ}\text{C}/\text{W}$
	No airflow ⁽⁴⁾	P pkg		93		
θ_{JB} Junction-to-board thermal resistance	High-K board	D pkg		67		
	See ⁽⁴⁾	P pkg		57		
θ_{JC} Junction-to-case thermal resistance		D pkg		41		
		P pkg		55		
P_D Device power dissipation	$R_L=60\Omega, C=50\text{ pF}, DE$ at V_{CC} , RE at 0 V , Input to Da 50% duty cycle squarewave at indicated signaling rate	HVD10 (32Mbps)		198	250	mW
		HVD11 (10Mbps)		141	176	
		HVD12 (500kbps)		133	161	
T_A Ambient air temperature	High-K board, No airflow	D pkg	-40		116	$^{\circ}\text{C}$
	No airflow ⁽⁴⁾	P pkg	-40		123	
T_{JSD} Thermal shutdown junction temperature				165		

(1) See Application Information section for an explanation of these parameters.

(2) The intent of θ_{JA} specification is solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment.

(3) JSD51-7, High Effective Thermal Conductivity Test Board for Leadless Surface Mount Packages.

(4) JE51-10, Test Boards for Through-Hole Perimeter Lead Package Thermal Measurements



DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18\text{mA}$	-1.5			V
$ V_{OD} $	Differential output voltage ⁽²⁾	$I_O = 0$	2		V_{CC}	V
		$R_L = 54\Omega$, See Figure 1	1.5			
		$V_{test} = -7\text{V}$ to 12V , See Figure 2	1.5			
$\Delta V_{OD} $	Change in magnitude of differential output voltage	See Figure 1 and Figure 2	-0.2		0.2	V
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage	See Figure 3		400		mV
$V_{OC(SS)}$	Steady-state common-mode output voltage		1.4		2.5	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage		-0.05		0.05	V
I_{OZ}	High-impedance output current	See receiver input currents				
I_I	Input current	D	-100		0	μA
		DE	0		100	
I_{OS}	Short-circuit output current	$-7\text{V} \leq V_O \leq 12\text{V}$	-250		250	mA
$C_{(OD)}$	Differential output capacitance	$V_{OD} = 0.4 \sin(4E6\pi t) + 0.5\text{V}$, DE at 0V		16		pF
I_{CC}	Supply current	RE at V_{CC} , D & DE at V_{CC} , No load		9	15.5	mA
		RE at V_{CC} , D at V_{CC} , DE at 0V, No load		1	5	μA
		RE at 0V, D & DE at V_{CC} , No load		9	15.5	mA



(1) All typical values are at 25 ° C and with a 3.3-V supply.

(2) For $T_A > 85^\circ\text{C}$, V_{CC} is $\pm 5\%$.

DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	HVD10	5	8.5	16	ns
		HVD11	18	25	40	
		HVD12	135	200	300	
t_{PHL}	Propagation delay time, high-to-low-level output	HVD10	5	8.5	16	ns
		HVD11	18	25	40	
		HVD12	135	200	300	
t_r	Differential output signal rise time	HVD10	3	4.5	10	ns
		HVD11	10	20	30	
		HVD12	100	170	300	
t_f	Differential output signal fall time	HVD10	3	4.5	10	ns
		HVD11	10	20	30	
		HVD12	100	170	300	
$t_{SK(P)}$	Pulse skew ($ t_{PHL} - t_{PLH} $)	HVD10			1.5	ns
		HVD11			2.5	
		HVD12			7	
$t_{SK(PP)}^{(2)}$	Part-to-part skew	HVD10			6	ns
		HVD11			11	
		HVD12			100	

$R_L = 54\Omega$, $C_L = 50\text{ pF}$,
See Figure 4



t _{PZH} Propagation delay time,high-impedance-to-high-level output	HVD10	R _L =110Ω,RE at 0V ,See Figure 5			31	ns
	HVD11				55	
	HVD12				300	
t _{PHZ} Propagation delay time,high-level-to-high-impedance output	HVD10	R _L =110Ω,RE at 0V ,See Figure 5			25	ns
	HVD11				55	
	HVD12				300	
t _{PZL} Propagation delay time,high-impedance-to-low-level output	HVD10	R _L =110Ω,RE at 0V ,See Figure 6			26	ns
	HVD11				55	
	HVD12				300	
t _{PLZ} Propagation delay time,low-level-to-high-impedance output	HVD10	R _L =110Ω,RE at 3V ,See Figure 6			26	ns
	HVD11				75	
	HVD12				400	
t _{PZH} Propagation delay time,standby-to-high-level output		R _L =110 Ω,RE at 3V,See Figure 5			6	μs
t _{PZL} Propagation delay time,standby-to-low-level output		R _L =110Ω,RE at 3V ,See Figure 6			6	μ s

(1) All typical values are at 25 ° C and with a 3.3-V supply.

(2) tsk(pp) is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.



RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{IT+}	Positive-going input threshold voltage	I _O = -8 mA		-0.065	-0.01	V
V _{IT-}	Negative-going input threshold voltage	I _O =8 mA	-0.2	-0.1		
V _{hys}	Hysteresis voltage (V _{IT+} -V _{IT-})			35		mV
V _{IK}	Enable-input clamp voltage	I _I = -18mA	-1.5			V
V _{OH}	High-level output voltage	V _{ID} =20mV, I _{OH} = -8 mA, See Figure 7	2.4			V
V _{OL}	Low-level output voltage	V _{ID} = -200 mV, I _{OL} =8 mA, See Figure 7			0.4	V
I _{OZ}	High-impedance-state output current	V _O =0 or V _{CC} RE at V _{CC}	-1		1	μA
I _I	Bus input current	V _A or V _B =12V		0.05	0.11	mA
		V _A or V _B =12V, V _{CC} =0V		0.06	0.13	
		V _A or V _B = -7V	-0.1	-0.05		
		V _A or V _B = -7V, V _{CC} =0V	-0.05	-0.04		
		V _A or V _B =12V		0.2	0.5	mA
		V _A or V _B =12V, V _{CC} =0V		0.25	0.5	
		V _A or V _B = -7 V	-0.4	-0.2		
		V _A or V _B = -7V, V _{CC} =0V	-0.4	-0.15		
I _{IH}	High-level input current,RE	V _{IH} =2V	-30		0	μA
I _{IL}	I Low-level input current,RE	V _{IL} =0.8V	-30		0	μA
C _{ID}	Differential input capacitance	V _{ID} =0.4 sin(4E6πt)+0.5V,DE at 0V		15		pF



I _{CC} Supply current	RE at 0V, D&DE at 0V, No load	Receiver enabled and driverdisabled		4	8	mA
	RE at V _{CC} , D at V _{CC} , DE at 0V, No load	Receiver disabled and driverdisabled(standby)		1	5	μA
	RE at 0V, D&DE at V _{CC} , No load	Receiver enabled and driverenabled		9	15.5	mA

(1) All typical values are at 25 ° C and with a 3.3-V supply

RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
t _{PLH}	Propagation delay time,low-to-high -level output	HVD10	V _{ID} = -1.5V to 1.5V, CL=15 pF, See Figure 8	12.5	20	25	ns
t _{PHL}	Propagation delay time,high-to- low-level output	HVD10		12.5	20	25	
t _{PLH}	Propagation delay time,low-to- high-level output	HVD11 HVD12		30	55	70	ns
t _{PHL}	Propagation delay time,high-to- low-level output	HVD11 HVD12		30	55	70	ns
t _{SK(P)}	Pulse skew (t _{PHL} -t _{LHI})	HVD10				1.5	ns
		HVD11				4	
		HVD12				4	
t _{SK(PP)} ⁽²⁾	Part-to-part skew	HVD10				8	ns
		HVD11				15	
		HVD12				15	
t _r	Output signal rise time		CL=15 pF, See Figure 8	1	2	5	ns
t _f	Output signal fall time			1	2	5	



$t_{PZH}^{(1)}$	Output enable time to high level	$C_L=15\text{ pF}$, DE at 3 V, See Figure 9			15	ns
$t_{PZL}^{(1)}$	Output enable time to low level				15	
t_{PHZ}	Output disable time from high level				20	
t_{PLZ}	Output disable time from low level				15	
$t_{PZH}^{(2)}$	Propagation delay time,standby-to-high-level output	$C_L=15\text{ pF}$, DE at 0, See Figure 10			6	$\mu\text{ s}$
$t_{PZL}^{(2)}$	Propagation delay time,standby-to-low-level output				6	

(1) All typical values are at 25 ° C and with a 3.3-V supply

(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.



PARAMETER MEASUREMENT INFORMATION

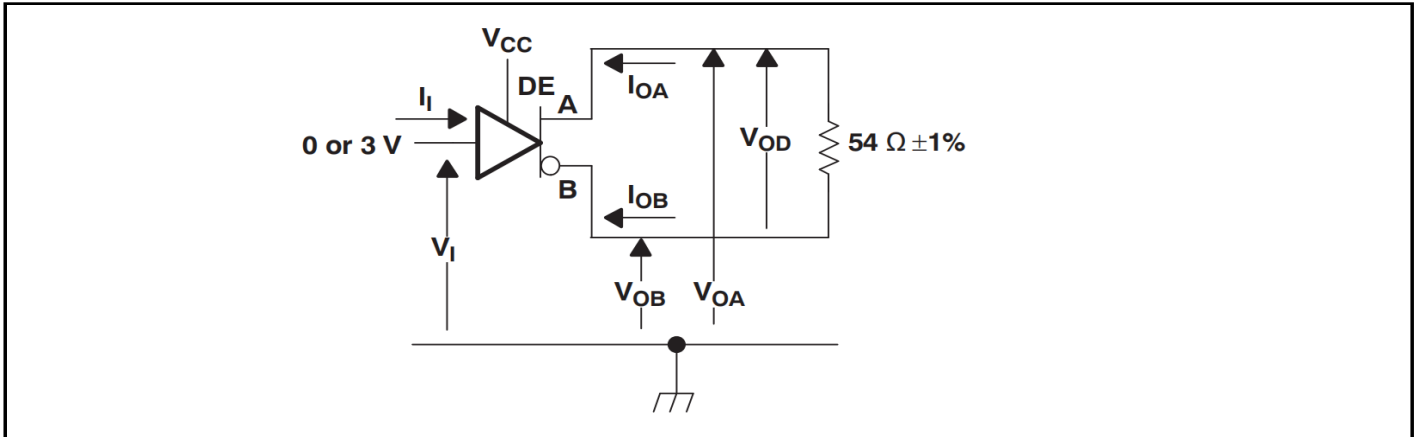


Figure 1. Driver V_{OD} Test Circuit and Voltage and Current Definitions

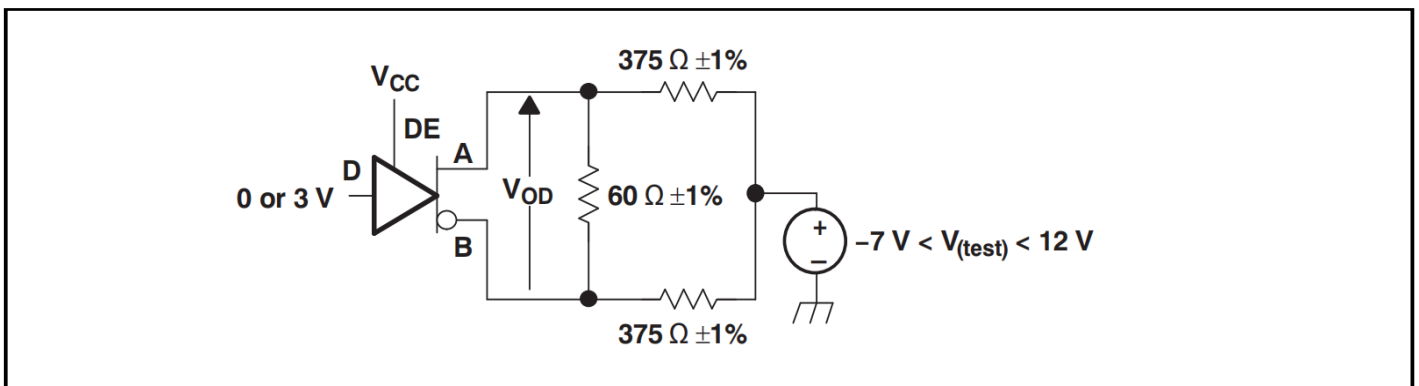
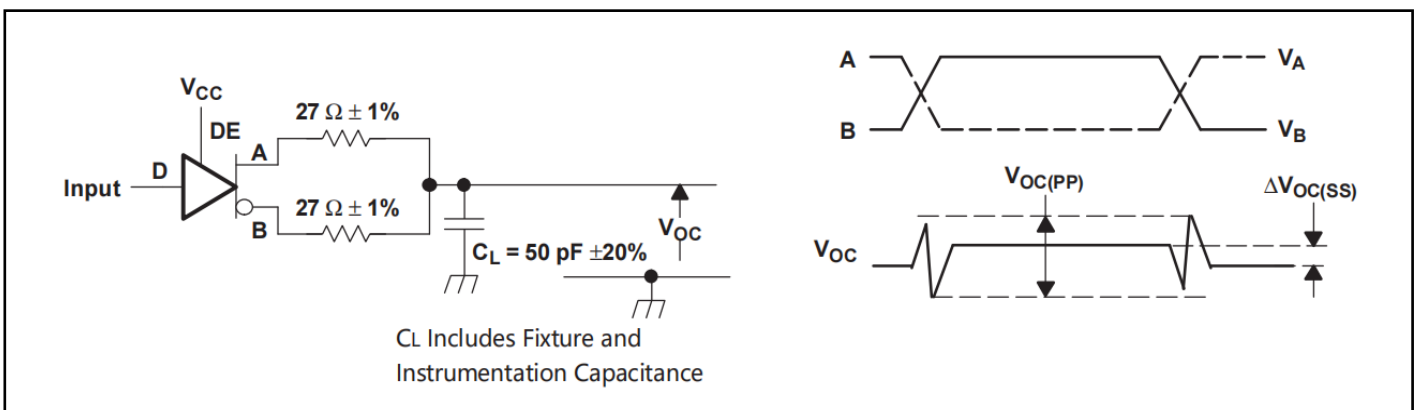


Figure 2. Driver V_{OD} With Common-Mode Loading Test Circuit



Input: PRR = 500 kHz, 50% Duty Cycle, $t_r < 6\text{ns}$, $t_f < 6\text{ns}$, $Z_O = 50\ \Omega$

Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

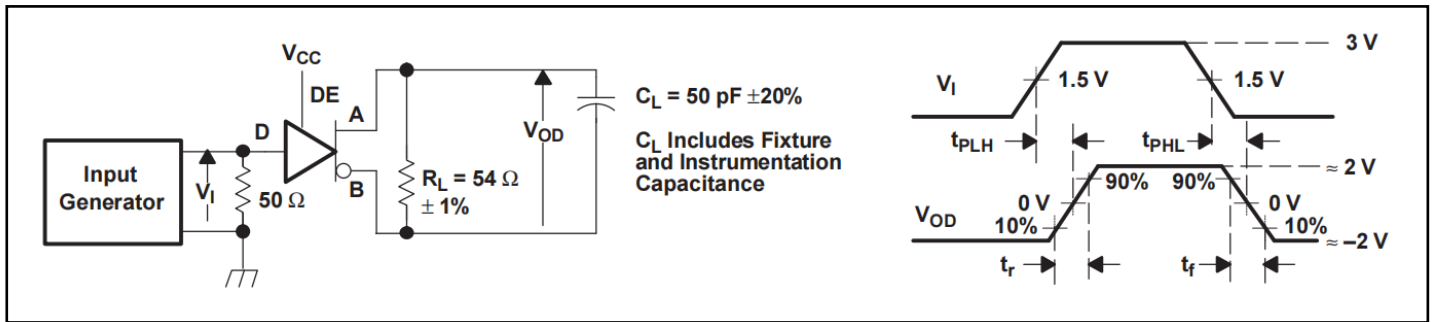


Figure 4. Driver Switching Test Circuit and Voltage Waveforms

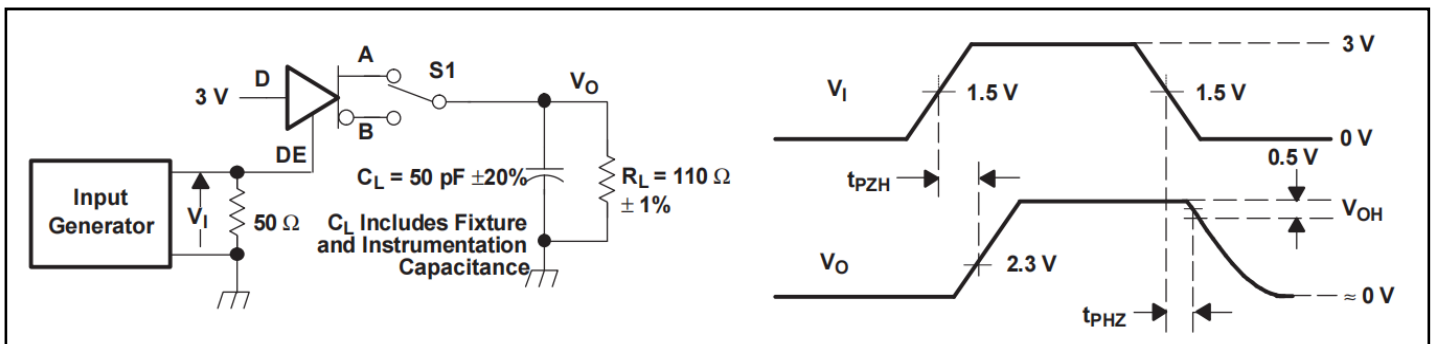


Figure 5. Driver High-Level Enable and Disable Time Test Circuit and Voltage Waveforms

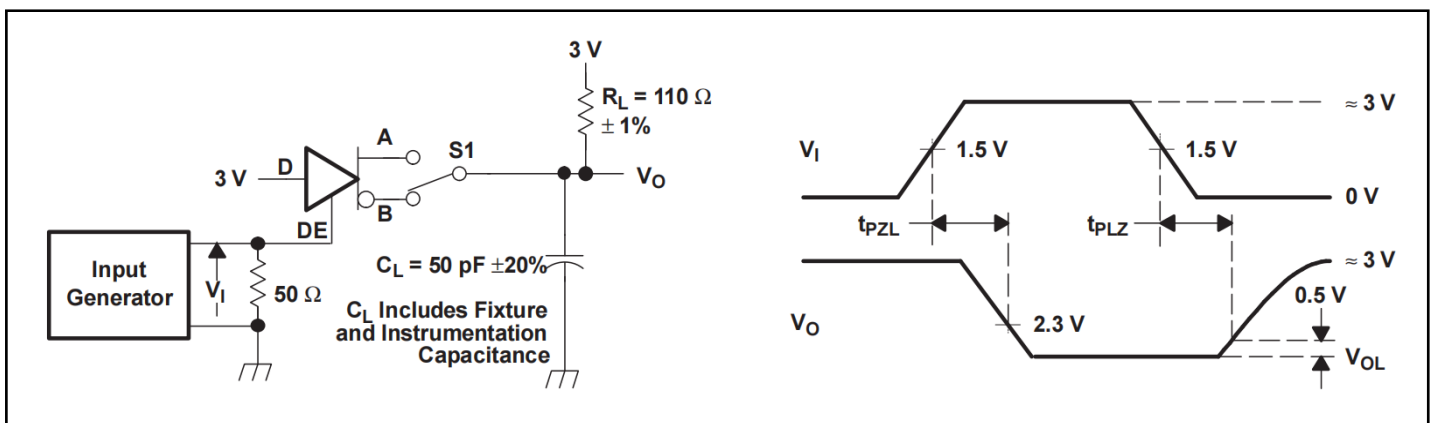


Figure 6. Driver Low-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms

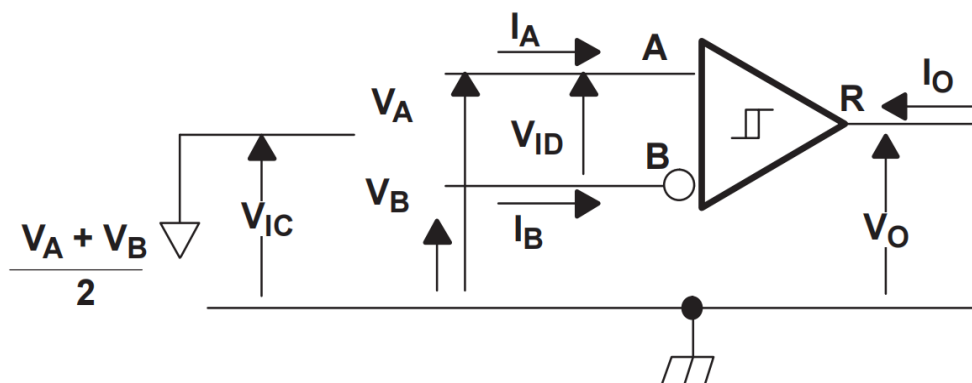
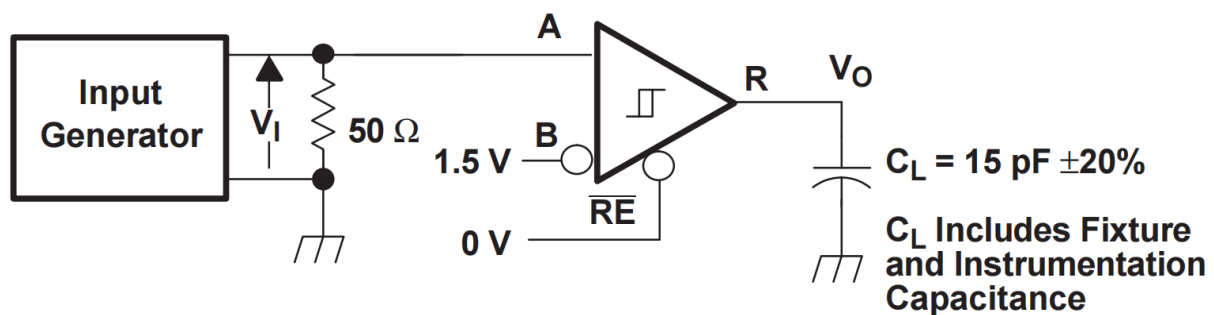
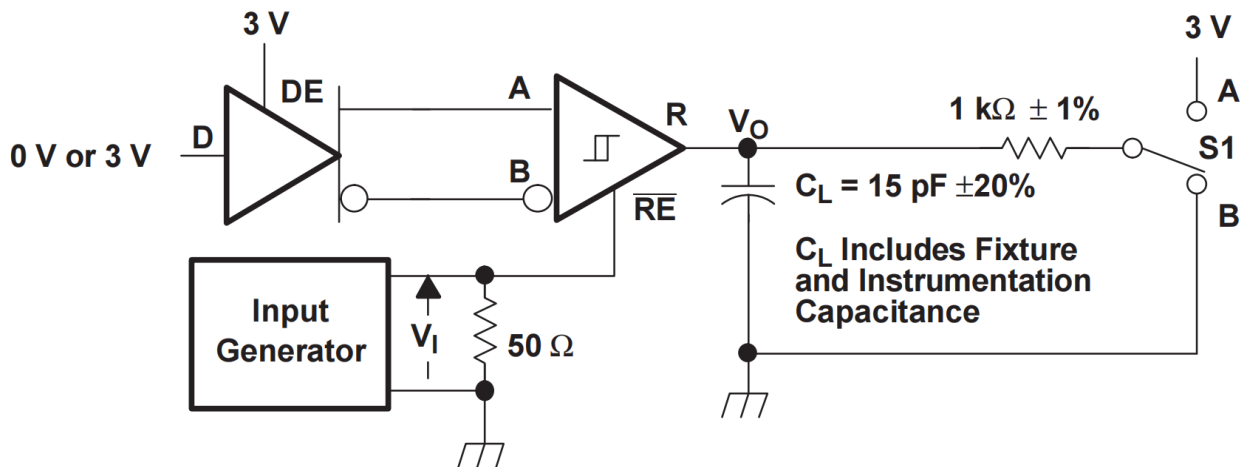


Figure 7. Receiver Voltage and Current Definitions



Generator: PRR = 500 kHz, 50% Duty Cycle, $t_r < 6$ ns, $t_f < 6$ ns, $Z_o = 50 \Omega$

Figure 8. Receiver Switching Test Circuit and Voltage Waveforms



Generator: PRR = 500 kHz, 50% Duty Cycle, $t_r < 6 \text{ ns}$, $t_f < 6 \text{ ns}$, $Z_o = 50 \Omega$

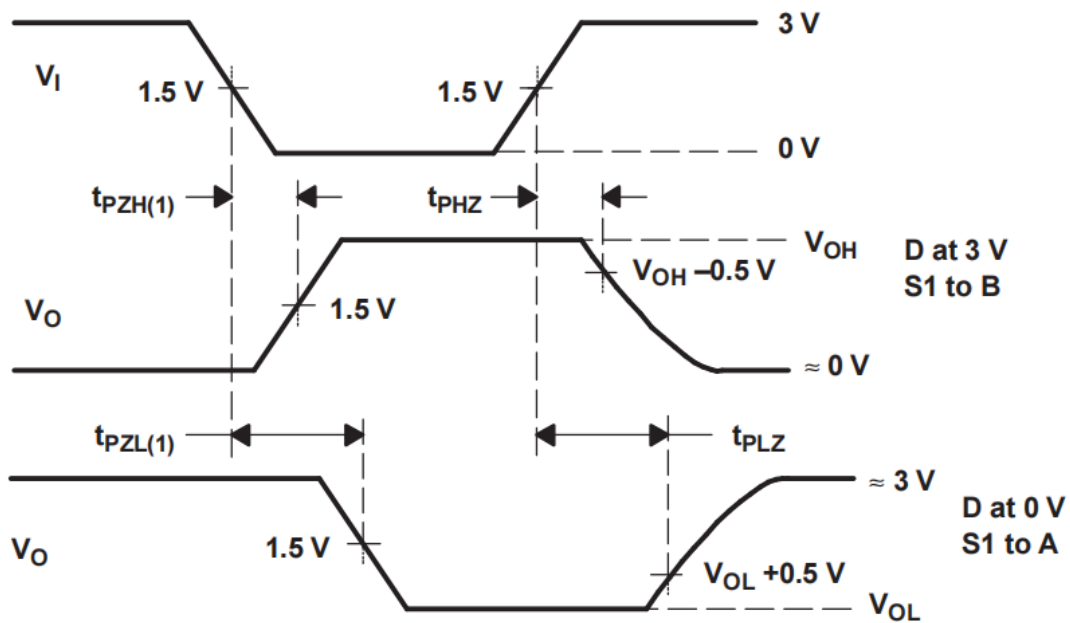


Figure 9. Receiver Enable and Disable Time Test Circuit and Voltage Waveforms With Drivers Enabled

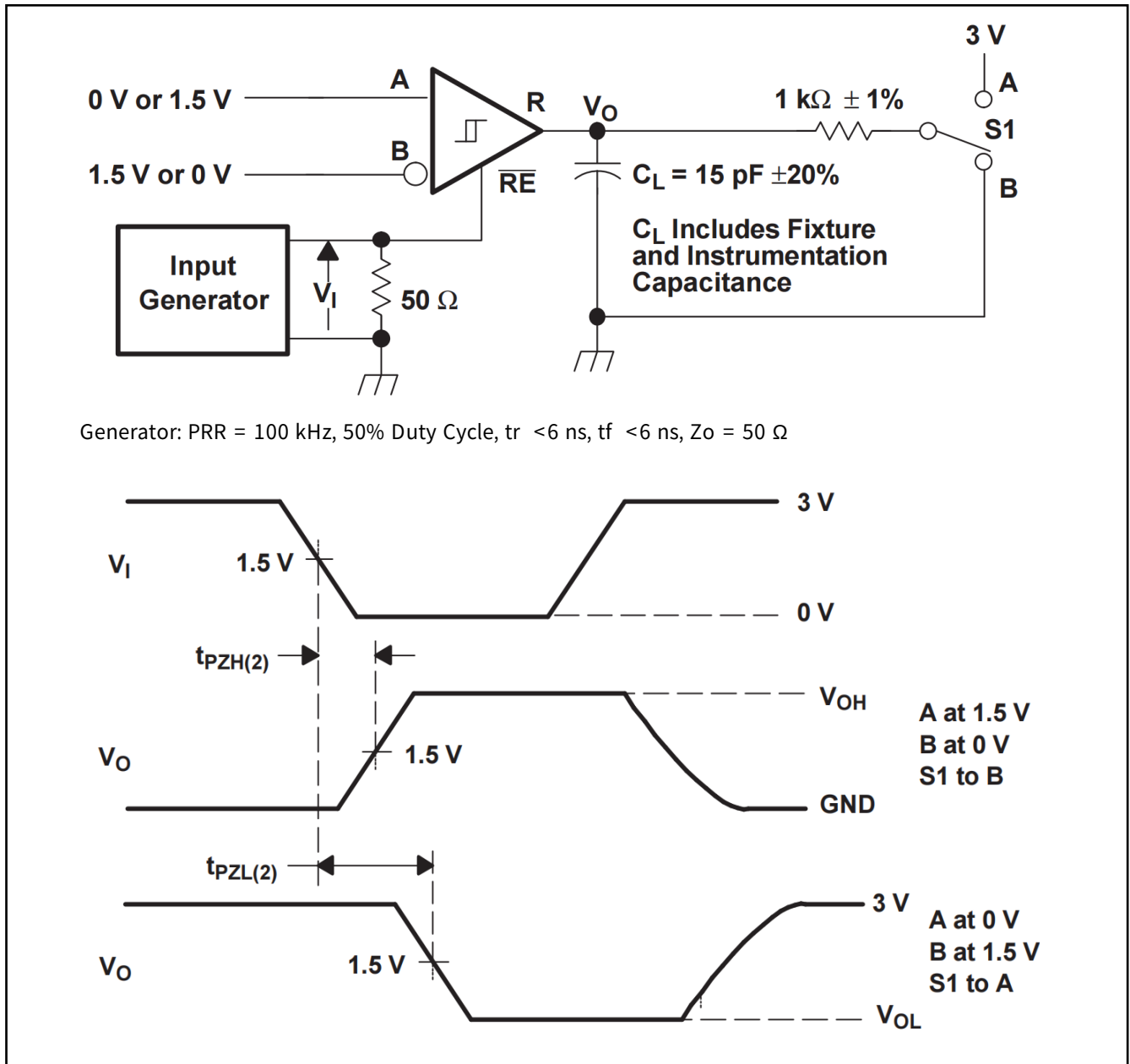
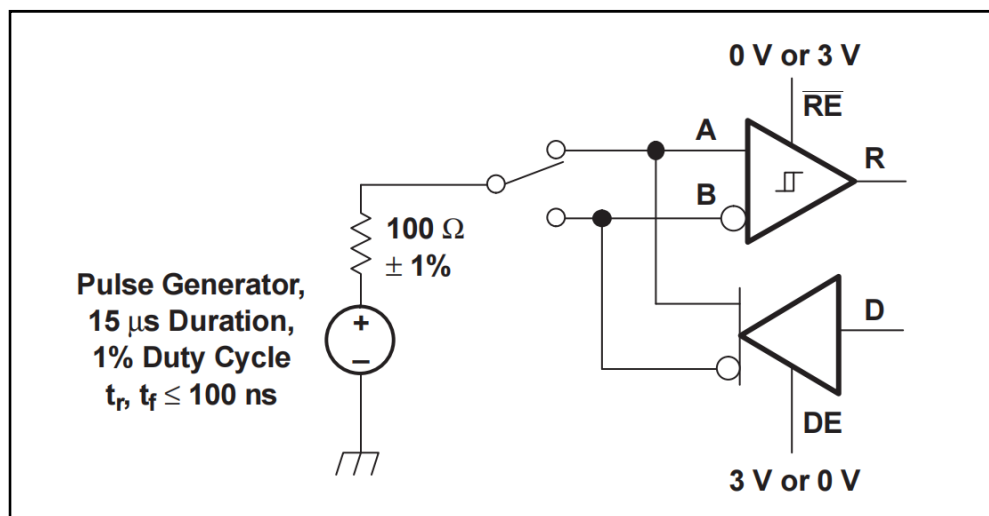


Figure 10. Receiver Enable Time From Standby (Driver Disabled)



NOTE: This test is conducted to test survivability only. Data stability at the R output is not specified

Figure 11. Test Circuit, Transient Over Voltage Test

FUNCTION TABLES

Table 1. DRIVER⁽¹⁾

		OUTPUTS	
INPUT D	ENABLEDE	A	B
H	H	H	L
L	H	L	H
X	L	Z	Z
Open	H	H	L

(1) H = high level; L = low level; Z = high impedance; X = irrelevant; ? = indeterminate



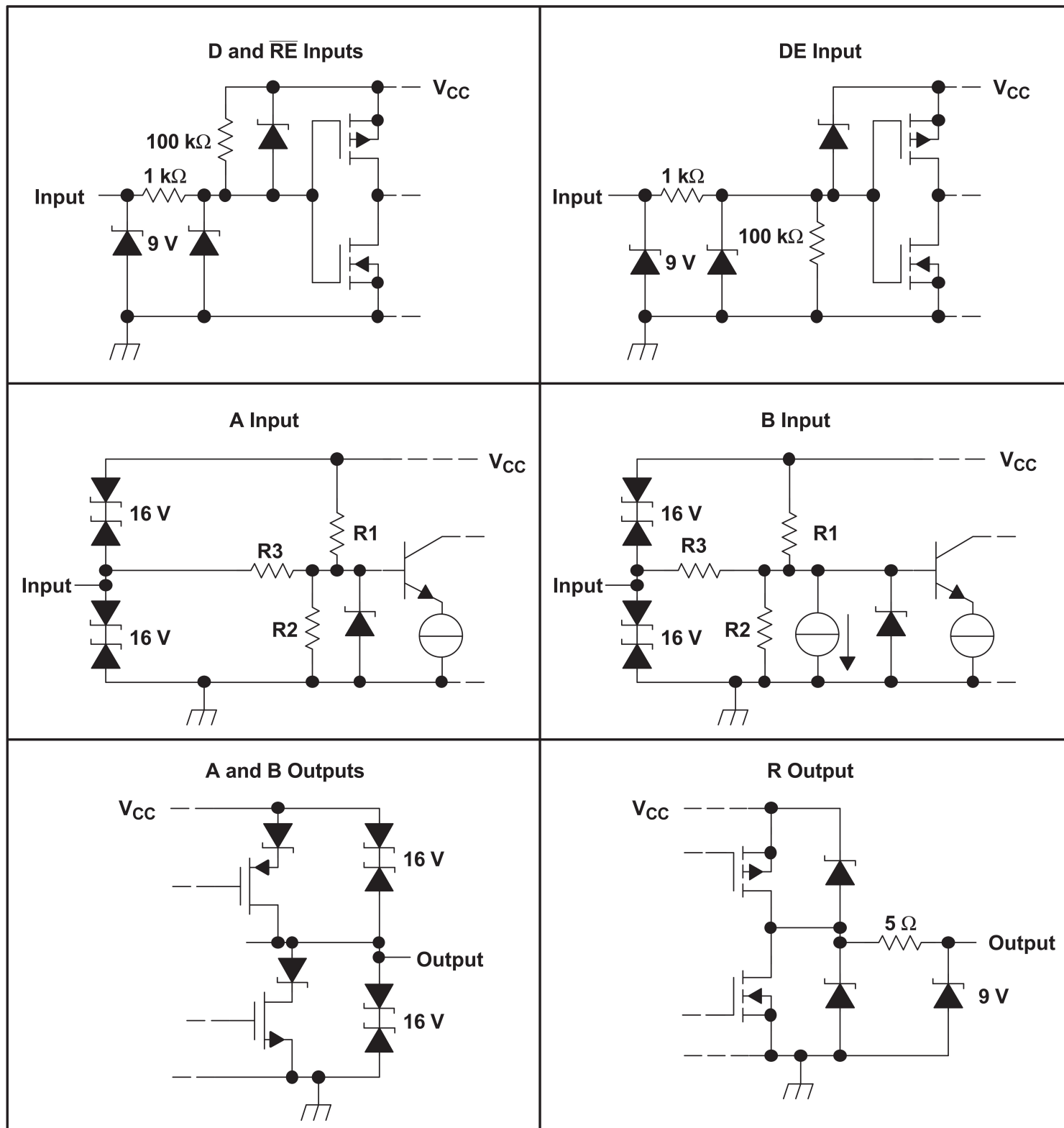
Table 2. RECEIVER⁽¹⁾

DIFFERENTIAL INPUTS $V_{ID}=V_A-V_B$	ENABLE RE	OUTPUT R
$V_{ID} \leq -0.2V$	L	L
$-0.2V < V_{ID} < -0.01V$	L	?
$-0.01V \leq V_{ID}$	L	H
X	H	Z
Open Circuit	L	H
Short circuit	L	H

(1) H = high level; L = low level; Z = high impedance; X = irrelevant; ? = indeterminate



EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS





	R1/R2	R3
SN65HVD10	9k Ω	45 k Ω
SN65HVD11	36 k Ω	180 k Ω
SN65HVD12	36 k Ω	180 k Ω

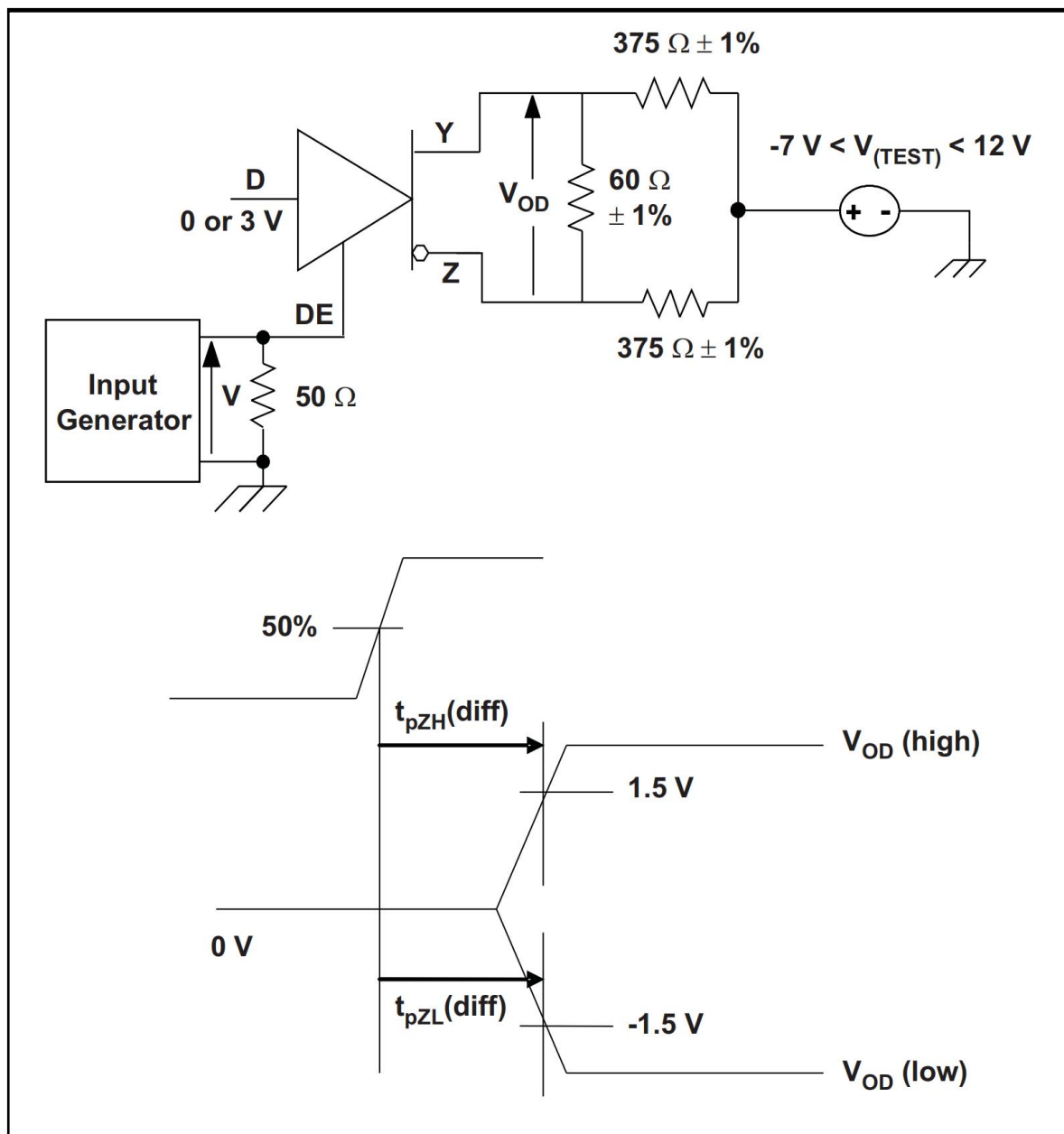
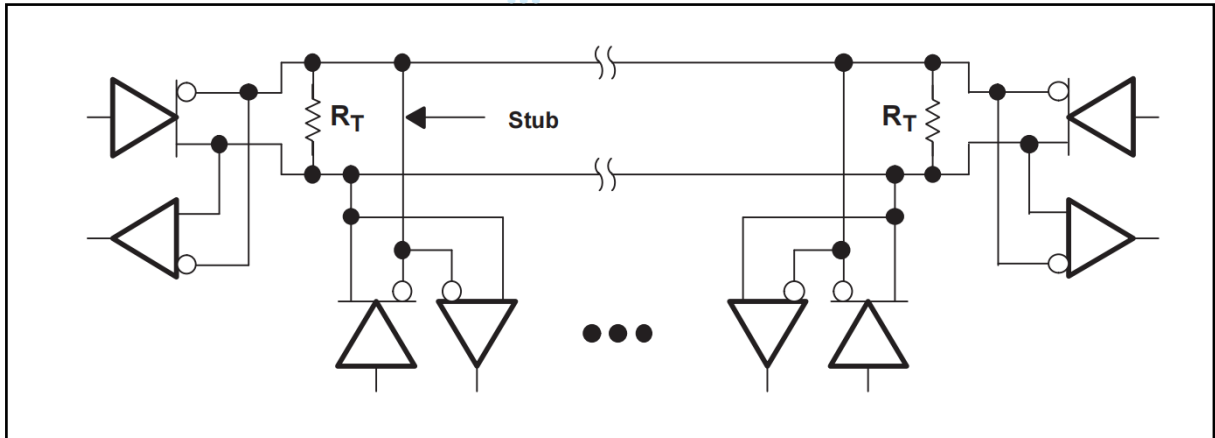


Figure 12 Driver Enable Time From DE to V_{OD}

The time $t_{pZL(x)}$ is the measure from DE to $V_{OD(x)}$. V_{OD} is valid when it is greater than 1.5 V



Device	Number of Devices on Bus
HVD10	64
HVD11	256
HVD12	256

NOTE: The line should be terminated at both ends with its characteristic impedance ($R_T = Z_0$). Stub lengths off the main line should be kept as short as possible.

LOW-POWER STANDBY MODE

When both the driver and receiver are disabled (DE low and RE high) the device is in standby mode. If the enable inputs are in this state for less than 60 ns, the device does not enter standby mode. This guards against inadvertently entering standby mode during driver/receiver enabling. Only when the enable inputs are held in this state for 300 ns or more, the device is assured to be in standby mode. In this low-power standby mode, most internal circuitry is powered down, and the supply current is typically less than 1 nA. When either the driver or the receiver is re-enabled, the internal circuitry becomes active.



THERMAL CHARACTERISTICS OF IC PACKAGES

θ_{JA} (Junction-to-Ambient Thermal Resistance) is defined as the difference in junction temperature to ambient temperature divided by the operating power.

θ_{JA} is not a constant and is a strong function of:

- the PCB design (50% variation)
- altitude (20% variation)
- device power (5% variation)

θ_{JA} can be used to compare the thermal performance of packages if the specific test conditions are defined and used. Standardized testing includes specification of PCB construction, test chamber volume, sensor locations, and the thermal characteristics of holding fixtures. θ_{JA} is often misused when it is used to calculate junction temperatures for other installations.

TI uses two test PCBs as defined by JEDEC specifications. The low-k board gives average in-use condition thermal performance, and it consists of a single copper trace layer 25 mm long and 2-oz thick. The high-k board gives best case in-use condition, and it consists of two 1-oz buried power planes with a single copper trace layer 25 mm long and 2-oz thick. A 4% to 50% difference in θ_{JA} can be measured between these two test cards.

θ_{JC} (Junction-to-Case Thermal Resistance) is defined as difference in junction temperature to case divided by the operating power. It is measured by putting the mounted package up against a copper block cold plate to force heat to flow from die, through the mold compound into the copper block.

θ_{JC} is a useful thermal characteristic when a heatsink is applied to package. It is not a useful characteristic to predict junction temperature because it provides pessimistic numbers if the case temperature is measured in a nonstandard system and junction temperatures are backed out. It can be used with θ_{JB} in 1-dimensional thermal simulation of a package system.

θ_{JB} (Junction-to-Board Thermal Resistance) is defined as the difference in the junction temperature and the PCB temperature at the center of the package (closest to the die) when the PCB is clamped in a cold-plate structure. θ_{JB} is only defined for the high-k test card.

θ_{JB} provides an overall thermal resistance between the die and the PCB. It includes a bit of the PCB thermal resistance (especially for BGAs with thermal balls) and can be used for simple 1-dimensional network analysis of package system

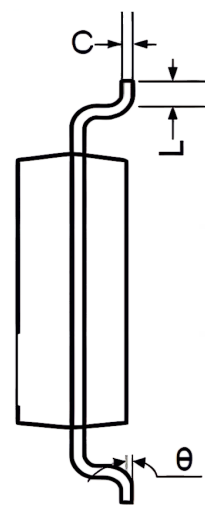
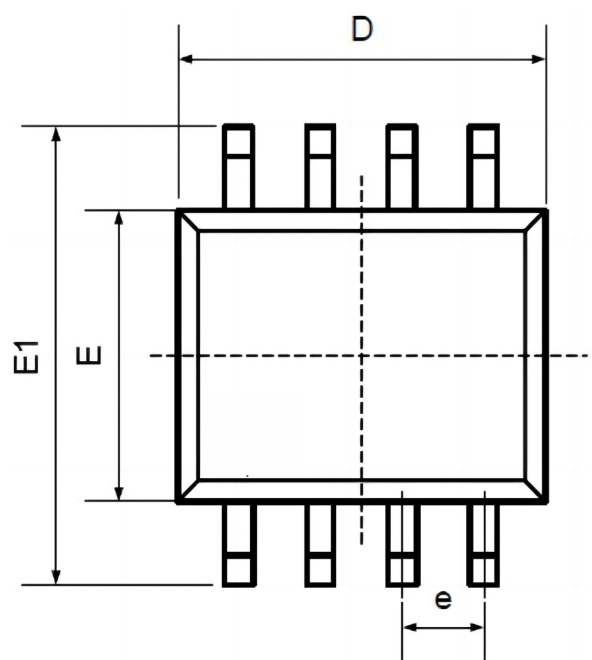


PACKAGING INFORMATION

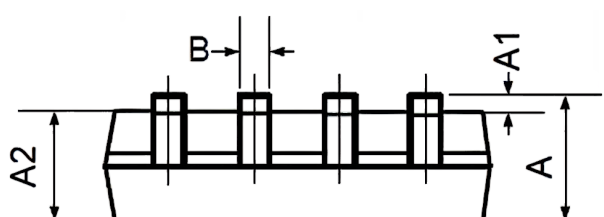
Order Number	Package	Package Quantity	Marking On The park	Temperature
SN75HVD10DR-TUDI	SOP8	Tape,Reel,4000	VN10	0°C to 70°C
SN75HVD10P-TUDI	DIP8	Tube,50,A box of 2000	75HVD10	
SN75HVD11DR-TUDI	SOP8	Tape,Reel,4000	VN11	
SN75HVD11P-TUDI	DIP8	Tube,50,A box of 2000	75HVD11	
SN75HVD12DR-TUDI	SOP8	Tape,Reel,4000	VN12	
SN75HVD12P-TUDI	DIP8	Tube,50,A box of 2000	75HVD12	
SN65HVD10DR-TUDI	SOP8	Tape,Reel,4000	VP10	-40°C to 85°C
SN65HVD10P-TUDI	DIP8	Tube,50,A box of 2000	65HVD10	
SN65HVD11DR-TUDI	SOP8	Tape,Reel,4000	VP11	
SN65HVD11P-TUDI	DIP8	Tube,50,A box of 2000	65HVD11	
SN65HVD12DR-TUDI	SOP8	Tape,Reel,4000	VP12	
SN65HVD12P-TUDI	DIP8	Tube,50,A box of 2000	65HVD12	
SN65HVD10QDR-TUDI	SOP8	Tape,Reel,4000	VP10Q	-40°C to 125°C
SN65HVD11QDR-TUDI	SOP8	Tape,Reel,4000	VP11Q	



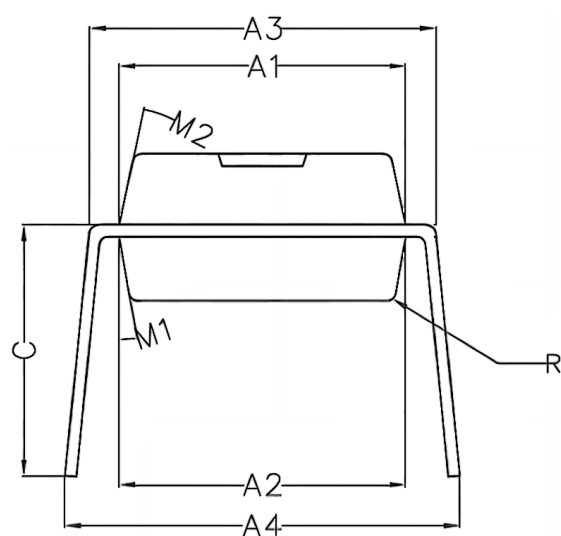
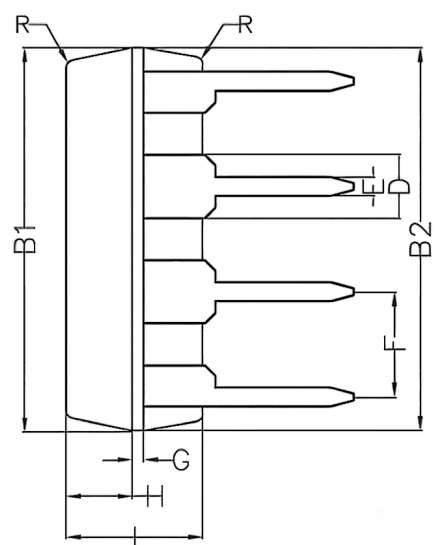
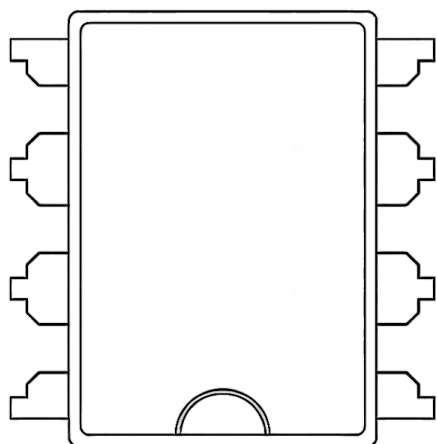
Package SOP8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



Package DIP8



Symbol	Min	Non	Max
A1	6.28	6.33	6.38
A2	6.33	6.38	6.43
A3	7.52	7.62	7.72
A4	7.80	8.40	9.00
B1	9.15	9.20	9.25
B2	9.20	9.25	9.30
C		5.57	
D		1.52	
E	0.43	0.45	0.47
F		2.54	
G		0.25	
H	1.54	1.59	1.64
I	3.22	3.27	3.32
R		0.20	
M1	9°	10°	11°
M2	11°	12°	13°



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