PLD1B

DYSIS2 for LED Driver

Description

PLD1B is the extension of dimmable single-stage PFC LED driver, aiming to provide dimmable LED driver with shimmer/flicker reduction (SR), which can be used alone or in combination with WarmGlow(WG) feature while on the side providing a substantial reduction in stroboscopic effect.

With an integrated 20V/1Ω SR MOSFET (MW) and a 200V/200mA WG MOSFET (MA).

PLD1B offers rich protection functions including VDD under voltage protection, DW over voltage protection, thermal regulation and over temperature protection.

Features

- Integrated 20V/1Ω MOSFET(MW)
- Integrated 200V/200mA MOSFET(MA)
- Adjustable SR Range
- Adjustable WG Range
- VDD Under Voltage Protection
- DW Over Voltage Protection
- Thermal Regulation Function
- Over Temperature Protection
- Available in SOP8 Package

Applications

- dimmable LED Lamp
- E14/E27 filament lamp
- GU10/E27 LED Bulb, Spot Light
- Other LED Lighting

Typical Application

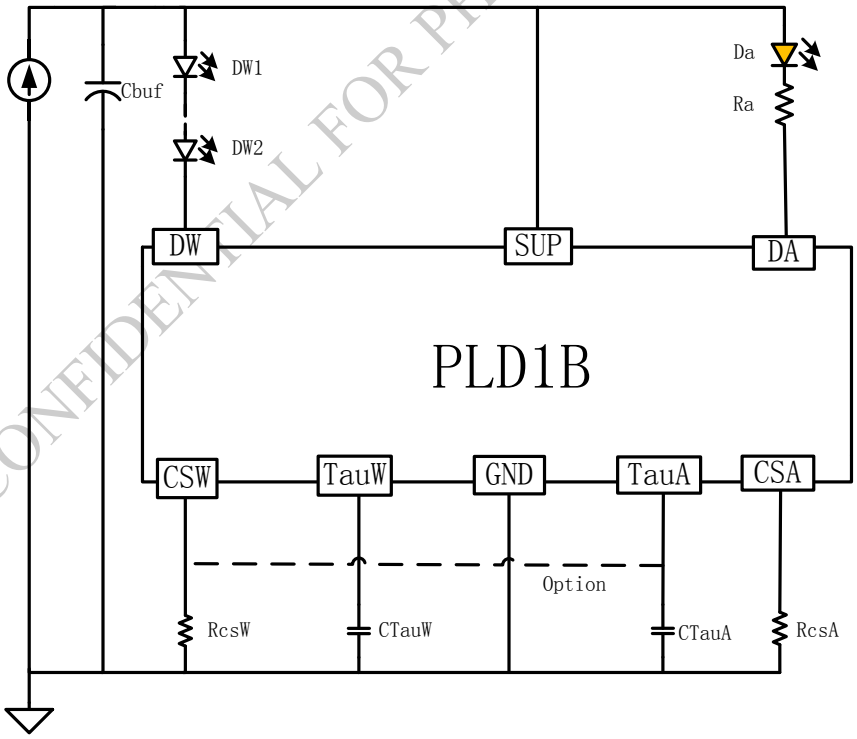
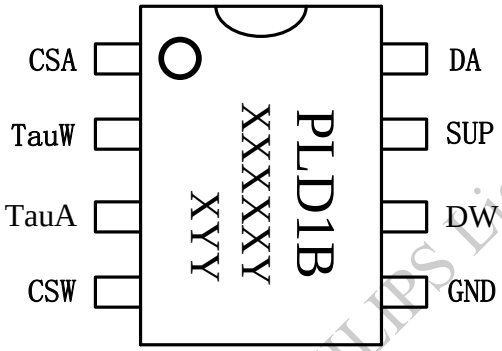


Figure 1. Typical application

Ordering Information

Part Number	Package	Package Method	Marking
PLD1B	SOP8	Tape 4,000 Piece/Roll	PLD1B XXXXXY XYY

Pin Configuration and Marking Information



XXXXXY: Lot Code
X: Year
YY: Week

Figure 2. Pin configuration

Pin Definition

Pin No.	Name	Description
1	CSA	WG Current Sense Pin.
2	TauW	SR Loop Compensation Pin.
3	TauA	WG Loop Compensation Pin.
4	CSW	SR Current Sense Pin.
5	GND	Ground Pin.
6	DW	Drain Connection of SR MOSFET MW.
7	SUP	IC Power Supply Pin.
8	DA	Drain Connection of WG MOSFET MA.

Absolute Maximum Ratings (note1)

Symbol	Parameters	Range	Units
DW	SR MOSFET MW drain voltage	-0.3~20	V
DA	WG MOSFET MW drain voltage	-0.3~200	V
$I_{D\_MAX\_MA}$	MA Saturation current	250	mA
CSW	SR CS pin voltage	-0.3~6	V
CSA	WG CS pin voltage	-0.3~6	V
SUP	JFET supply voltage	-0.3~200	V
TauW	SR Compensation pin voltage	-0.3~6	V
TauA	WG Compensation pin voltage	-0.3~6	V
P_{DMAX}	Power dissipation (note 2)	0.45	W
θ_{JA}	Thermal resistance (Junction to Ambient)	145	℃/W
T_J	Operating junction temperature	-40 to 150	℃
T_{STG}	Storage temperature range	-55 to 150	℃
	ESD (note3)	2	KV

Note 1: *Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. Under "recommended operating conditions" the device operation is assured, but some particular parameter may not be achieved. The electrical characteristics table defines the operation range of the device, the electrical characteristics is assured on DC and AC voltage by test program. For the parameters without minimum and maximum value in the EC table, the typical value defines the operation range, the accuracy is not guaranteed by spec.*

Note 2: *The maximum power dissipation decrease if temperature rise, it is decided by T_{JMAX}, θ_{JA}, and environment temperature (T_A). The maximum power dissipation is the lower one between $P_{DMAX} = (T_{JMAX} - T_A)/\theta_{JA}$ and the number listed in the maximum table.*

Note 3: *Human Body mode, 100pF capacitor discharge on 1.5KΩ resistor*

Electrical Characteristics (Notes 4, 5) (Unless otherwise specified, T_A=25 ℃)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Supply Section						
V_{SUP}	JFET Supply Voltage		7		200	V
I_{JFET_MAX}	JFET Peak Current	Sup=40V		6mA		mA
I_{CC}	IC Operation Current	Sup=40V		200	300	uA
Over Voltage Protection Section						
V_{DW_OVP}	DW Pin Over Voltage			10		V
Compensation Section						
Compensation Section						
V_{TauW}	Maximum TauW Operation Voltage		5			V
Gm_{OTA}	OTA Gm			5		uA/V
$V_{NonLinear}$	Non-Linear Trigger Point of TauW			4.5		V
Current Sense Section						
V_{REFW}	SR Active Current Sense Voltage			240		mV
V_{REFA}	WG Active Current Sense Voltage		97	100	103	mV
WalmGrow Section						
Ratio1	WG/SR Activation Current Ratio			1.75		Ω/Ω
Ratio2	WG/SR Activation Current Ratio	TauA Pin Shorted to CSW Pin		0.75		Ω/Ω
MOSFET Section						
$R_{DS\_ON\_MW}$	MW Static Drain-source On-resistance	I_D=100mA		0.7		Ω
$I_{D\_MAX\_MA}$	MA Saturation Current		200			mA
Thermal Regulation Section						
T_{REG}	Thermal Regulation Temperature			140		℃
T_{SD}	Thermal Shutdown			160		℃
T_{SD_Hyst}	Thermal Shutdown Hysteresis			30		℃

Note4: *production testing of the chip is performed at 25°C.*

Note5: *the maximum and minimum parameters specified are guaranteed by test, the typical value are guaranteed by design, characterization and statistical analysis*

Internal Block Diagram

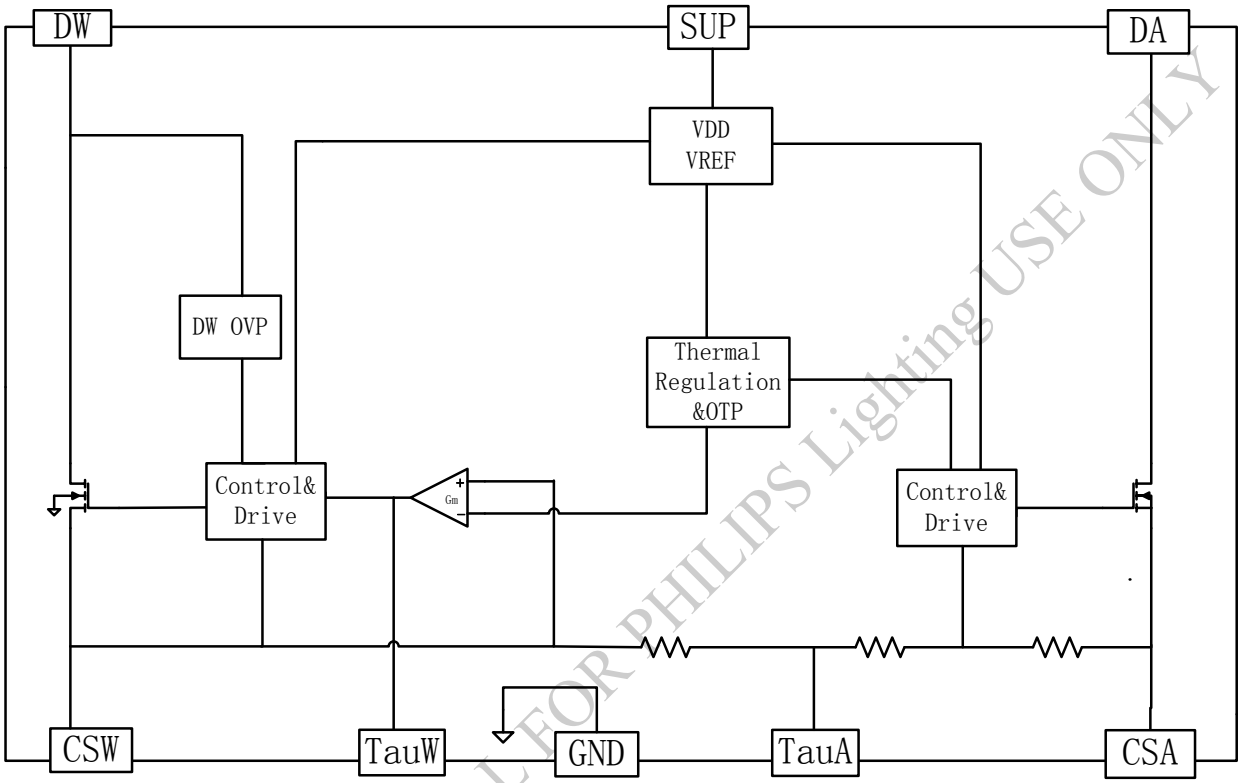


Figure 3. PLD1A Internal Block Diagram

Application Information

PLD1B is the extension of dimmable single-stage PFC LED driver, aiming to provide dimmable LED driver with shimmer/flicker reduction, which can be used alone or in combination with WG feature while on the side providing a substantial reduction in stroboscopic effect.

Start Up

The PLD1B integrates a HV JFET. After system power on, the chip is supplied by JEFT through SUP. When the internal VDD voltage reaches the turn on threshold, the internal circuits start operating. The HV JEFT will still supply operating current when the IC is working.

Shimmer / Flicker Reduction (SR)

SR suppresses repetitive and/or irregular visible low frequency variations in light level, resulting from variations in the dimming angle and/or mains voltage amplitude. SR is achieved by connecting an analog current source in series with the LED(s), the current adjusts itself slowly to maintain a relatively low average voltage (up to about 5V) across MW. The CSW voltage at the start of SR is $V_{REFW.}$

DW Over Voltage Protection

In order to prevent too high voltage across the MW, the voltage across MW needs to be clamped. DW

Over Voltage Protection (DW OVP) occurs when the output current quickly goes from low to high. The OVP comparator threshold is 10V.

Thermal Regulation

The PLD1B integrates thermal regulation function. When the system is over temperature, the $V_{REFW.}$ reference voltage for SR will be reduced. This will lower the voltage drop across the SR MOSFET MW, and thus directly reduce dissipation in MW. The $V_{REFA.}$ reference voltage for WG will also be reduced. In the WG analog range, this will reduce the current through the WG MOSFET MA, and thus ultimately reduce dissipation in MA. The system temperature is regulated and the system reliability is improved. The thermal regulation temperature is set to 140℃ internally.

PCB Layout

The following rules should be followed in DLP1B PCB layout:

Bypass Capacitor

The TauW and TauA bypass capacitors need to be placed as close as possible to the device.

Ground Path

Minimize ground noise by connecting the IC-GND lead, the input bypass capacitor ground lead, and the output filter capacitor ground lead to a single point. A ground plane is required. Minimize lead lengths to reduce stray capacitance, trace resistance, and radiated noise.

The power ground path for current sense resistor should be short and wide, and it should be as close as possible to the IC ground.

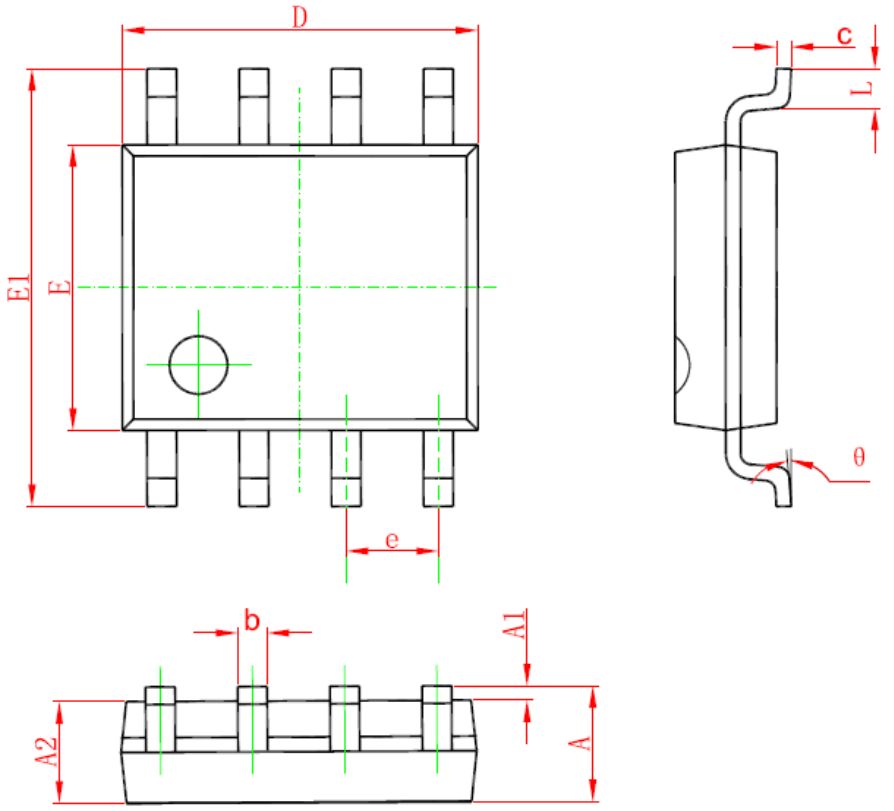
The copper area of the IC should be as large as possible for better thermal dissipation.

The Trace

When laying out a board, minimize trace lengths between the chip and Rcs, and the input capacitor. Keep traces short, direct, and wide. Keep HV traces, such as the SUP node trace, away from TauW and TauA.

Physical Dimensions

SOP8 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°