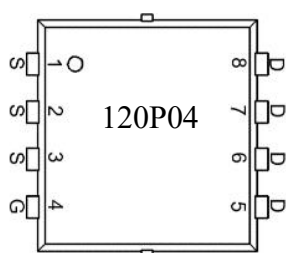


**Features**

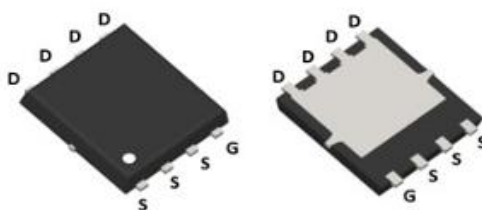
- 100% EAS Guaranteed
- Green Device Available
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- Advanced high cell density Trench technology

Bvdss**-40V*****Rdson*****3.1mΩ*****ID*****-120A****Application**

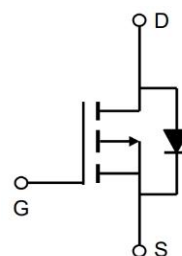
- Battery protection
- Load switch
- Uninterruptible power supply

RoHS**Package**

Marking and pin assignment



PDFN5x6-8L top view



Schematic diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Quantity
120P04	HL120P04F	PDFN5x6-8L	5000

Absolute Maximum Ratings ($T_C=25^{\circ}\text{C}$ unless otherwise specified)

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	-40	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current, $V_{GS}@10V^1$	$T_C = 25^{\circ}\text{C}$	I_D	-120	A
	$T_C = 100^{\circ}\text{C}$	I_D	-90	A
Pulsed Drain Current ²		I_{DM}	-576	A
Single Pulse Avalanche Energy ³		EAS	583	mJ
Avalanche Current		I_{AS}	-54	A
Total Power Dissipation ⁴		P_D	147	W
Operating Junction Temperature Range		T_J	-55 ~ 150	$^{\circ}\text{C}$
Storage Temperature Range		T_{STG}	-55 ~ 150	$^{\circ}\text{C}$

Thermal Resistance Ratings

Parameter	Symbol	Value	Unit
Thermal Resistance from Junction-to-Ambient ¹	$R_{\theta JA}$	53	$^{\circ}\text{C/W}$
Thermal Resistance from Junction-to-Case ¹	$R_{\theta JC}$	0.85	$^{\circ}\text{C/W}$



Ordering Information

Ordering Number	Package	Pin Assignment			Packing
Halogen Free		G	D	S	
HL120P04F	PDFN5x6-8L	4	5,6,7,8	1,2,3	Tape Reel

Electrical Characteristics ($T_J=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-40	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-40V, V_{GS}=0V$	-	-	-1	μA
Gate-body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=-250\mu A$	-1.2	-	-2.5	V
Static Drain-Source On-Resistance ²	$R_{DS(on)}$	$V_{GS} = -10V, I_D = -1A$	-	3.1	4.3	m Ω
		$V_{GS} = -4.5V, I_D = -1A$	-	4.4	5.4	
Input Capacitance	C_{iss}	$V_{DS}=-20V, V_{GS}=0V, f=1.0MHz$	-	7290	-	pF
Output Capacitance	C_{oss}		-	790	-	
Reverse Transfer Capacitance	C_{rss}		-	725	-	
Forward Transconductance	g_{fs}	$V_{DS}=-10V, I_D=-20A$	-	97	-	S
Gate resistance	R_g	$V_{DS}=0V, V_{GS}=0V, f=1.0MHz$	-	4.8	-	Ω
Total Gate Charge	Q_g	$V_{DS}=-20V, I_D=-20A,$ $V_{GS}=-10V$	-	250	-	nC
Gate Source Charge	Q_{gs}		-	23	-	
Gate Drain ("Miller") Charge	Q_{gd}		-	51	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DS}=-20V, R_g=3.3\Omega,$ $V_{GS}=-10V$	-	42	-	ns
Turn-On Rise Time	t_r		-	47	-	
Turn-Off Delay Time	$t_{d(off)}$		-	486	-	
Turn-Off Fall Time	t_f		-	249	-	
Drain to Source Diode Forward Voltage ²	V_{SD}	$V_{GS}=0V, I_S=-13A$	-	-	-1.2	V
Continuous Source Current ^{1,4}	I_S	$V_G=V_D=0V, \text{Force Current}$	-	-	-120	A
Reverse Recovery Time	t_{rr}	-	-	-	-	ns
Reverse Recovery Charge	Q_{rr}		-	-	-	nC

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
- 3.The EAS data shows Max. rating . The test condition is $T_J=25^{\circ}\text{C}, V_{DD}=-40V, V_G=-10V, R_g=25\Omega, L=0.5mH$.
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.



Typical Performance Characteristics

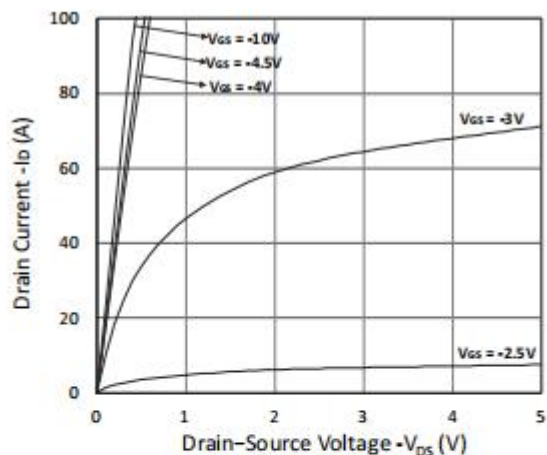


Figure 1. Output Characteristics

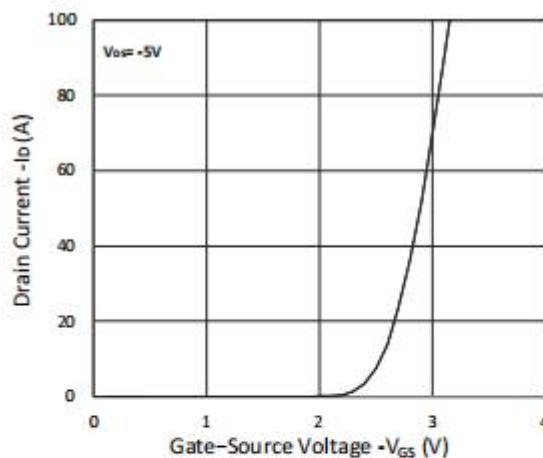


Figure 2. Transfer Characteristics

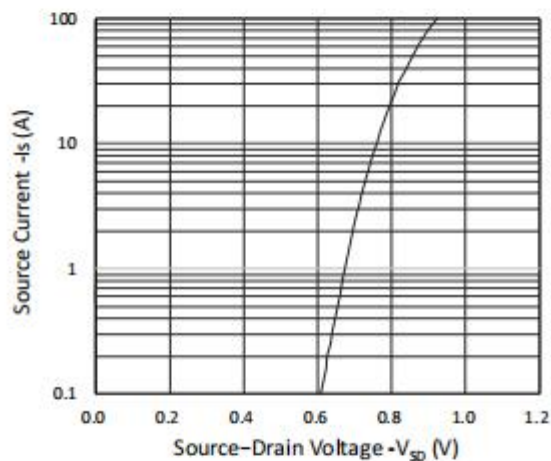
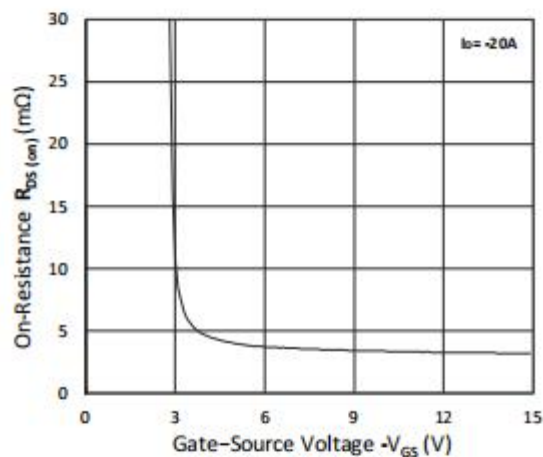
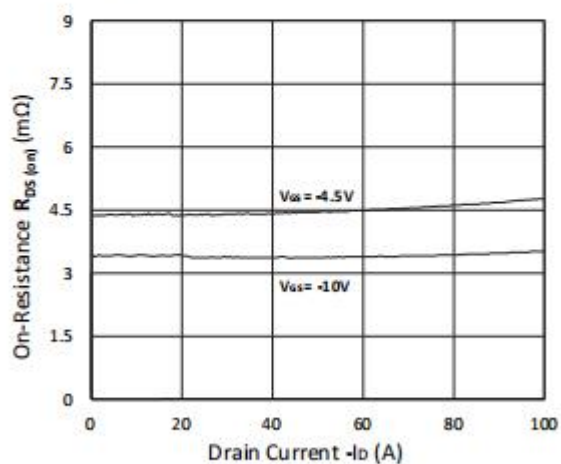
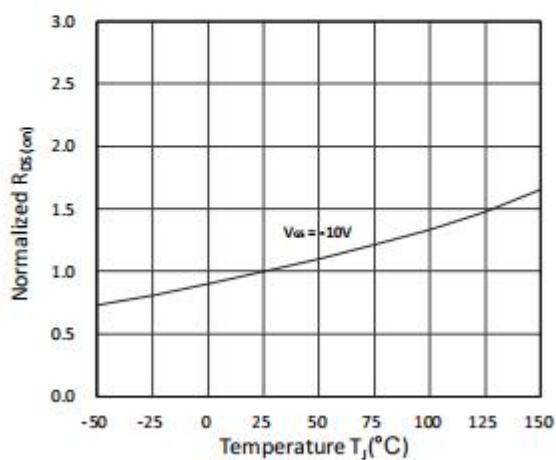


Figure 3. Forward Characteristics of Reverse

Figure 4. $R_{DS(on)}$ vs. V_{GS} Figure 5. $R_{DS(on)}$ vs. I_D Figure 6. Normalized $R_{DS(on)}$ vs. Temperature

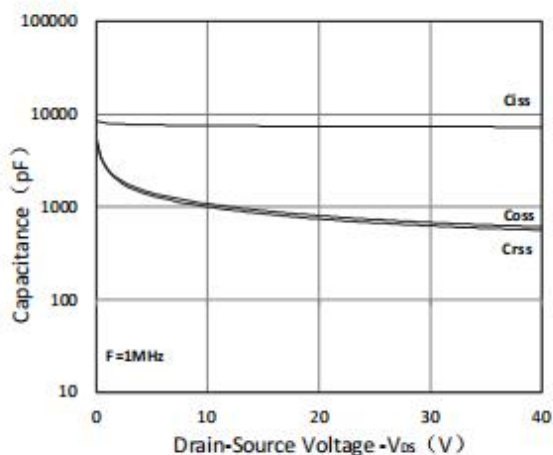


Figure 7. Capacitance Characteristics

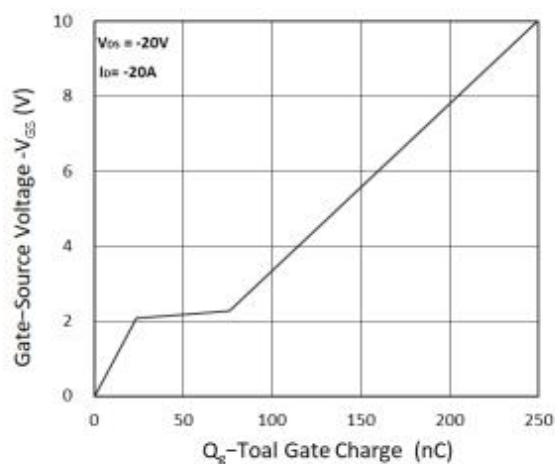


Figure 8. Gate Charge Characteristics

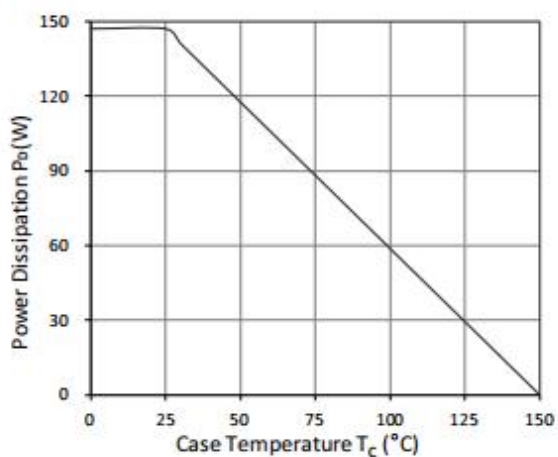


Figure 9. Power Dissipation

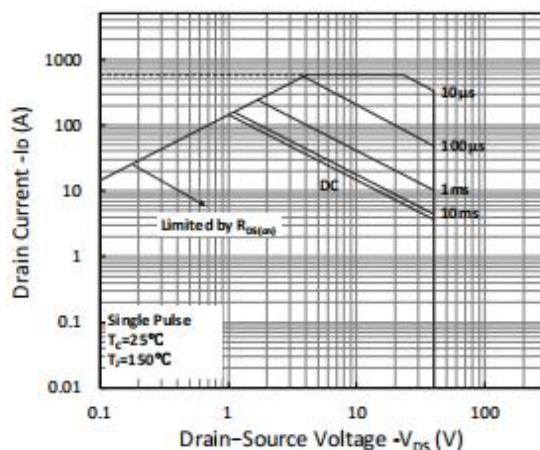


Figure 10. Safe Operating Area

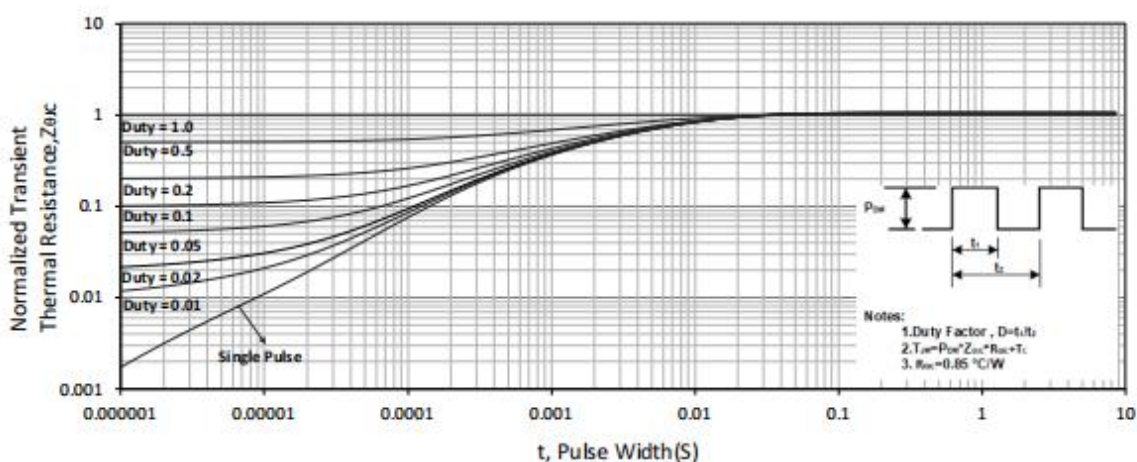
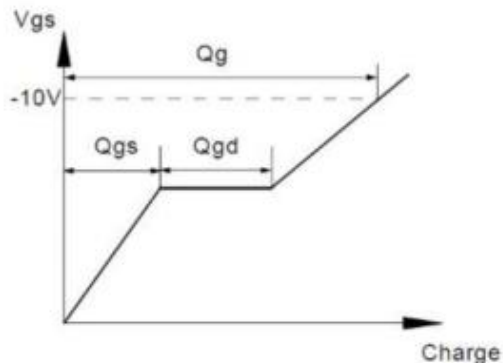
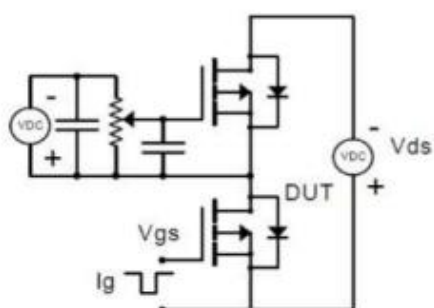


Figure 11. Normalized Maximum Transient Thermal Impedance

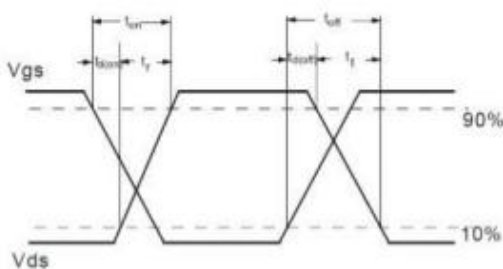
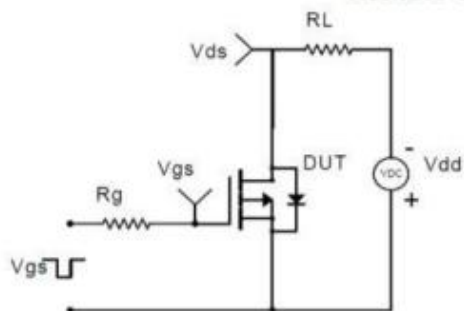


Test Circuit

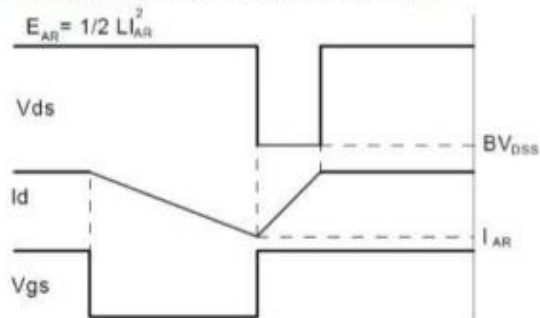
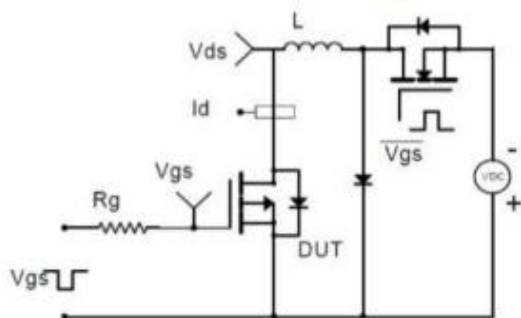
Gate Charge Test Circuit & Waveform



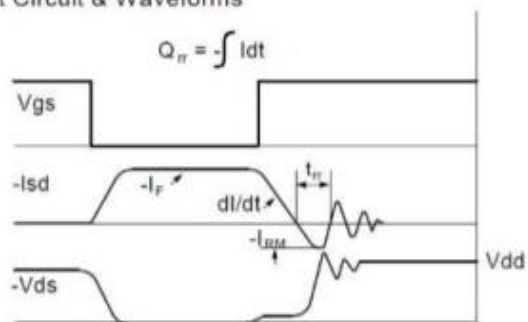
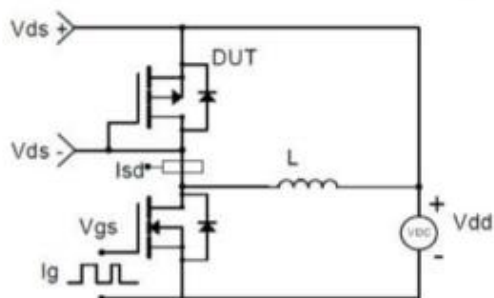
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

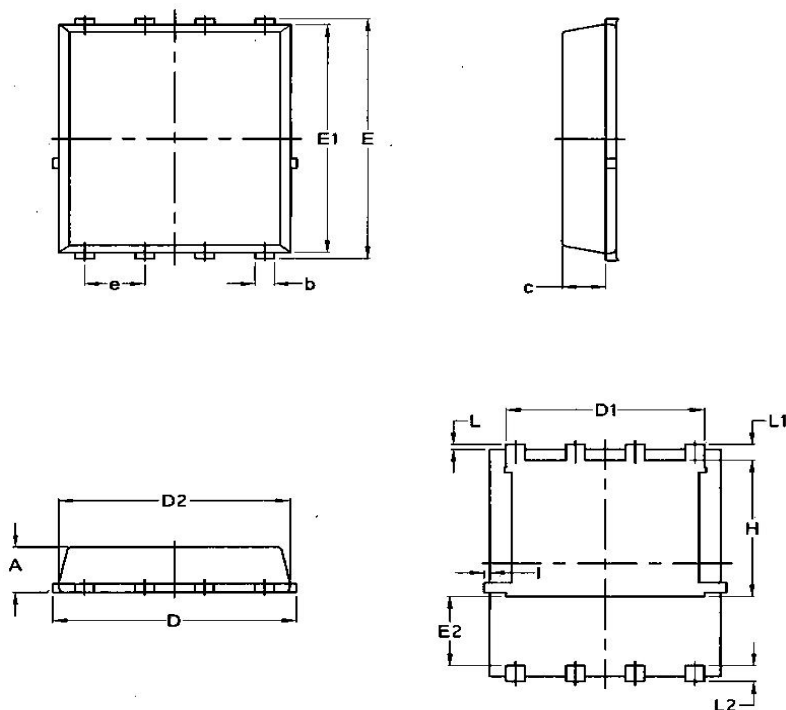


Diode Recovery Test Circuit & Waveforms





Package Dimensions PDFN5x6-8L



Symbol	Common			
	mm		Inch	
	Min	Max	Min	Max
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.0970	0.0324	0.082
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	/	0.18	/	0.0070



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