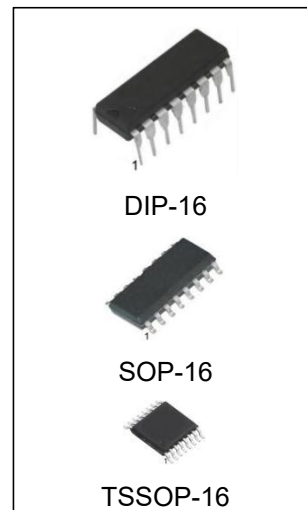


High-Performance Silicon-Gate CMOS

Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2.0 to 5.0 V
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 100 FETs or 25 Equivalent Gates



Package/Ordering Information

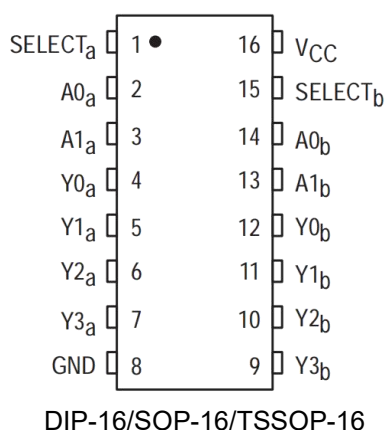
DEVICE	Package Type	MARKING	Packing	Packing Qty
74HC139N	DIP-16	74HC139	TUBE	1000pcs/Box
74HC139M/TR	SOP-16	74HC139	REEL	2500pcs/Reel
74HC139MT/TR	TSSOP-16	HC139	REEL	2500pcs/Reel

General Description

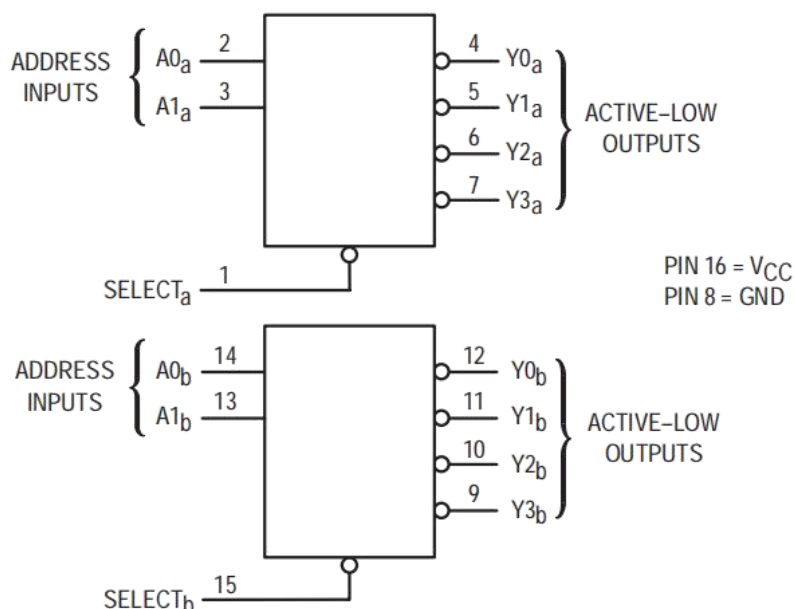
The 74HC139 is identical in pinout to the LS139. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of two independent 1-of-4 decoders, each of which decodes a two-bit Address to one-of-four active-low outputs. Active-low Selects are provided to facilitate the demultiplexing and cascading functions. The demultiplexing function is accomplished by using the Address inputs to select the desired device output, and utilizing the Select as a data input.

Pin Assignment



Logic Diagram



Function Table

Inputs			Outputs			
Select	A1	A0	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

X = don't care

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	– 1.5 to V _{CC} + 1.5	V
V _{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V _{CC} + 0.5	V
I _{in}	DC Input Current, per Pin	20	mA
I _{out}	DC Output Current, per Pin	25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	50	mA
P _D	Power Dissipation in Still Air, Plastic DIP† SOP Package†	750 500	mW
T _{stg}	Storage Temperature	– 65 to + 150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOP Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: – 10 mW/°C from 65 to 125°C
SOP Package: – 7 mW/°C from 65 to 125°C

Recommended Operating Conditions

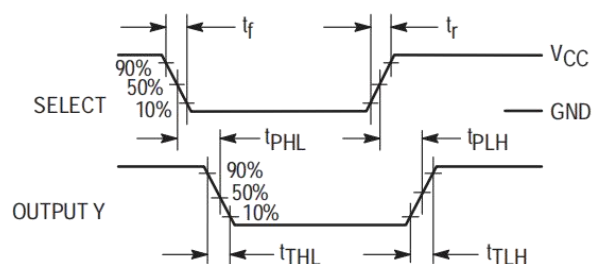
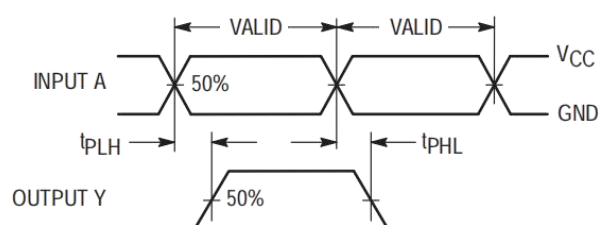
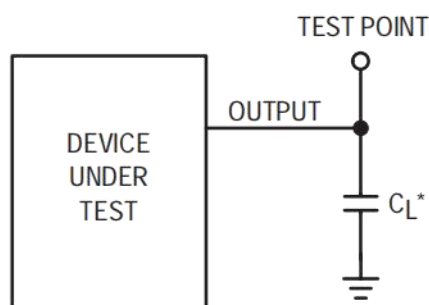
Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	5.0	V
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	-40	+ 85	°C
t _r , t _f	Input Rise and Fall Time(Figure 1) V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 5.0 V	0	1000 500 400	ns

Dc Electrical Characteristics (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				-40 to 25°C	85°C	125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} 20μA	2.0 4.5 5.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V _{IL}	Maximum Low-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} 20μA	2.0 4.5 5.0	0.5 1.35 1.8	0.5 1.35 1.8	0.5 1.35 1.8	V
V _{OH}	Minimum High-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} 20μA	2.0 4.5 5.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V _{in} = V _{IH} or V _{IL} I _{out} 4.0 mA	4.5	3.98	3.84	3.70	
		I _{out} 5.2 mA	5.0	5.48	5.34	5.20	
V _{OL}	Maximum Low-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} 20μA	2.0 4.5 5.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V _{in} = V _{IH} or V _{IL} I _{out} 4.0 mA	4.5	0.26	0.33	0.40	
		I _{out} 5.2 mA	5.0	0.26	0.33	0.40	
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	5.0	±0.1	±1.0	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0 μA	5.0	4	40	160	μA

Ac Electrical Characteristics (CL = 50 pF, Input tr = tf = 6.0 ns)

Symbol	Parameter	VCC V	Guaranteed Limit			Unit
			-40 to25℃	85℃	125℃	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Select to Output Y(Figures 1 and 3)	2.0	115	145	175	ns
		4.5	23	29	35	
		5.0	20	25	30	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input A to Output Y(Figures 2 and 3)	2.0	115	145	175	ns
		4.5	23	29	35	
		5.0	20	25	30	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output(Figures 1 and 3)	2.0	75	95	110	ns
		4.5	15	19	22	
		5.0	13	16	19	
C _{in}	Maximum Input Capacitance	—	10	10	10	pF
C _{PD}	Power Dissipation Capacitance (Per Decoder)*		Typical @ 25℃, VCC = 5.0 V			pF
			55			

Switching Waveforms

Figure 1.

Figure 2.


*Includes all probe and jig capacitance

Figure 3. Test Circuit

Pin Descriptions

ADDRESS INPUTS

A0a, A1a, A0b, A1b (Pins 2, 3, 14, 13)

Address inputs. These inputs, when the respective 1-of-4 decoder is enabled, determine which of its four active-low outputs is selected.

CONTROL INPUTS

Selecta, Selectb (Pins 1, 15)

Active-low select inputs. For a low level on this input, the outputs for that particular decoder follow the Address inputs. A high level on this input forces all outputs to a high level.

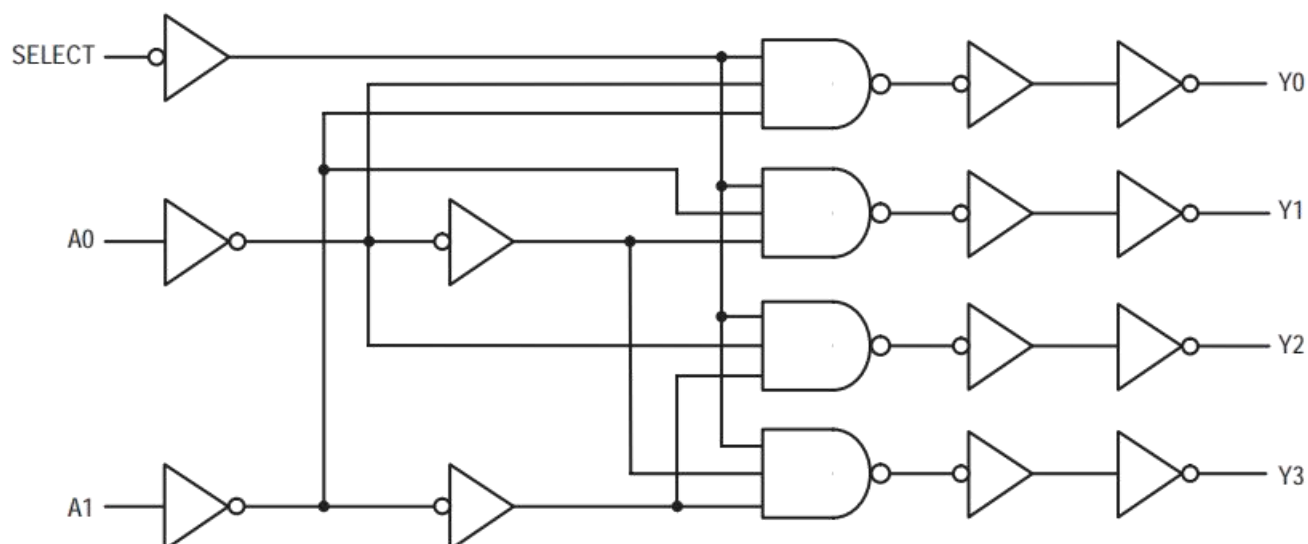
OUTPUTS

Y0a – Y3a, Y0b – Y3b (Pins 4 – 7, 12, 11, 10, 9)

Active-low outputs. These outputs assume a low level when addressed and the appropriate Select input is active. These outputs remain high when not addressed or the appropriate Select input is inactive.

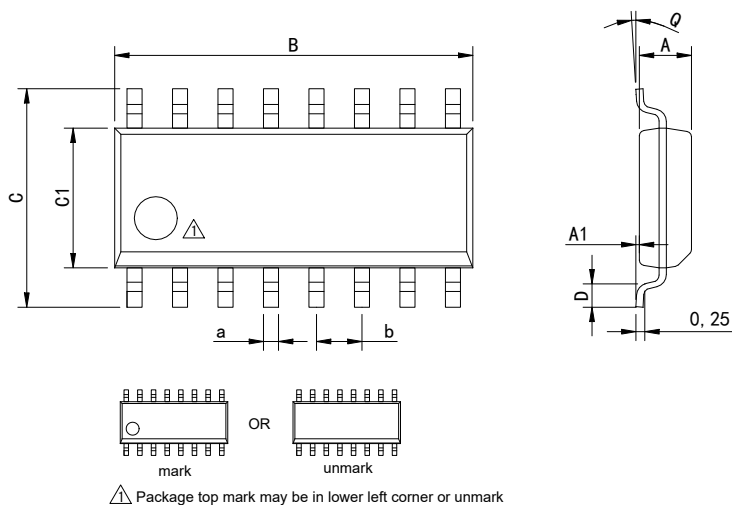
EXPANDED LOGIC DIAGRAM

(1/2 OF DEVICE)



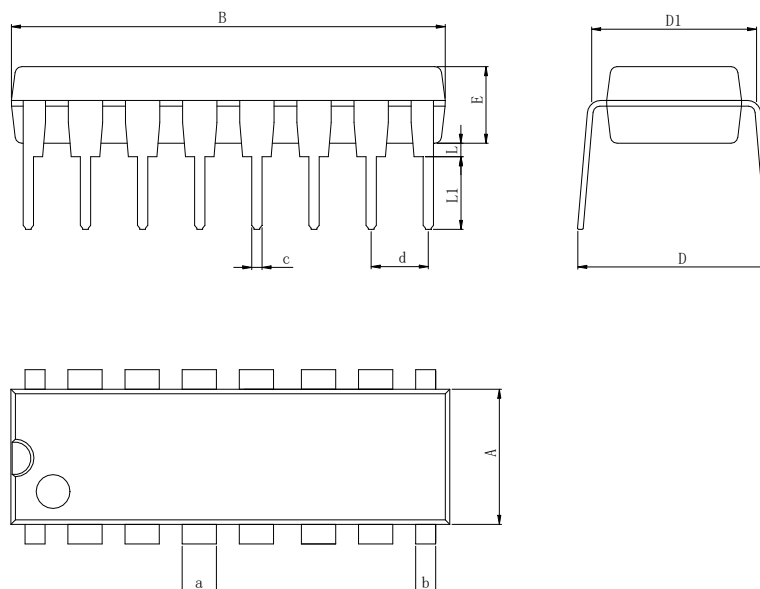
Physical Dimensions

SOP-16



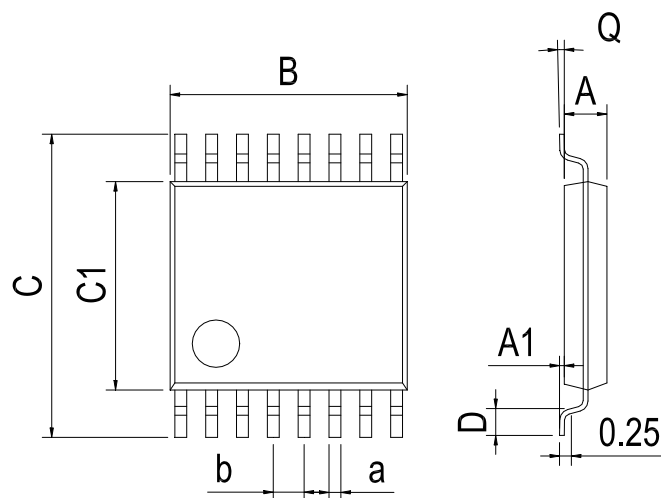
Dimensions In Millimeters(SOP-16)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	1.35	0.05	9.80	5.80	3.80	0.40	0°	0.35	1.27 BSC
Max:	1.55	0.20	10.0	6.20	4.00	0.80	8°	0.45	

DIP-16



Dimensions In Millimeters(DIP-16)											
Symbol:	A	B	D	D1	E	L	L1	a	b	c	d
Min:	6.10	18.94	8.10	7.42	3.10	0.50	3.00	1.50	0.85	0.40	2.54 BSC
Max:	6.68	19.56	10.9	7.82	3.55	0.70	3.60	1.55	0.90	0.50	

TSSOP-16



Dimensions In Millimeters(TSSOP-16)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	0.85	0.05	4.90	6.20	4.30	0.40	0°	0.20	0.65 BSC
Max:	0.95	0.20	5.10	6.60	4.50	0.80	8°	0.25	

Revision History

REVISION NUMBER	DATE	REVISION	PAGE
V1.0	2016-3	New	1-10
V1.1	2023-9	Modify the package dimension diagram TSSOP-16、Updated DIP-16 dimension	7、 8
V1.2	2024-11	Update Lead Temperature	3
V1.3	2025-9	Update important statements、 Update sop-16 Dimension drawing	7、 10

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