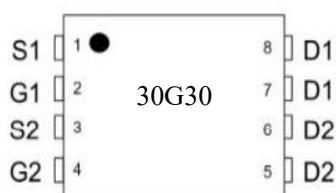


**Features**

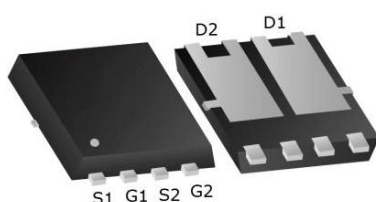
- Super Low Gate Charge
- Green Device Available
- Excellent Cdv/dt effect decline
- Advanced high cell density Trench technology
- 100% EAS Guaranteed

Bvdss**30V****-30V****Rdson****9.5mΩ****16mΩ****ID****30A****-30A****Application****RoHS**

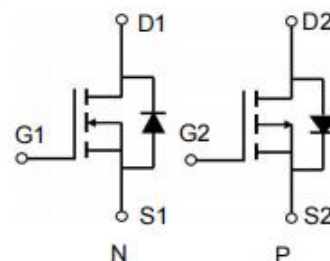
- Power management in half bridge and inverters
- Load Switch
- DC-DC Converter

Package

Marking and pin assignment



PDFN5x6-8L top view



Schematic diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Quantity
30G30	HL30G30F	PDFN5x6-8L	5000

Absolute Maximum Ratings

Parameter	Symbol	Value		Unit
		N-Channel	P-Channel	
Drain-Source Voltage	V_{DS}	30	-30	V
Gate-Source Voltage	V_{GS}	± 20	± 20	V
Continuous Drain Current, $V_{GS}@10V^1$	$I_D@T_A=25^\circ C$	30	-30	A
	$I_D@T_A=100^\circ C$	15	-16	A
Pulsed Drain Current ²	I_{DM}	46	-40	A
Single Pulsed Avalanche Energy ³	EAS	28	66	mJ
Avalanche Current	I_{AS}	-	-	A
Total Power Dissipation ⁴	$P_D@T_c=25^\circ C$	15	21.3	W
Operating Junction Temperature Range	T_J	-55 ~ 150		$^\circ C$
Storage Temperature Range	T_{STG}	-55 ~ 150		$^\circ C$



Thermal Resistance Ratings

Parameter	Symbol	Value	Unit
Thermal Resistance Junction-Ambient ¹	$R_{\theta JA}$	48	°C/W
Thermal Resistance Junction-Case ¹	$R_{\theta JC}$	5	°C/W

Ordering Information

Ordering Number	Package	Pin Assignment			Packing
Halogen Free		G	D	S	
HL30G30F	PDFN5x6-8L	2,4	5,6,7,8	1,3	Tape Reel

N-Channel Electrical Characteristics ($T_J=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	30	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=30V, V_{GS}=0V$	-	-	1	μA
Gate to Body Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$	-	-	± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=250\mu A$	1	1.5	2.5	V
Static Drain-Source On-Resistance ³	$R_{DS(on)}$	$V_{GS}=10V, I_D=10A$	-	9.5	13	m Ω
		$V_{GS}=4.5V, I_D=5A$	-	16	22.5	
Input Capacitance	C_{iss}	$V_{DS}=15V, V_{GS}=0V, f=1MHz$	-	633	-	pF
Output Capacitance	C_{oss}		-	120	-	
Reverse Transfer Capacitance	C_{rss}		-	99	-	
Total Gate Charge	Q_g	$V_{GS}=10V, V_{DS}=15V, I_D=10A$	-	15	-	nC
Gate-Source Charge	Q_{gs}		-	4.7	-	
Gate-Drain Charge	Q_{gd}		-	3.6	-	
Turn-On Delay Time	$T_{d(on)}$	$V_{GS}=10V, V_{DS}=30V,$ $R_G=3\Omega, I_D=18A$	-	5	-	ns
Rise Time	T_r		-	8	-	
Turn-Off Delay Time	$T_{d(off)}$		-	21	-	
Fall Time	T_f		-	7	-	
Diode Forward Voltage	V_{SD}	$I_S=18A, V_{GS}=0V$	-	-	1.2	V
Continuous Source Current	I_S	-	-	-	30	A
Source Diode Forward Current	I_{SM}	-	-	-	72	A
Body Diode Reverse Recovery Time	T_{rr}	$I_F=18A, di/dt=100A/\mu s$	-	7	-	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	5.9	-	nC

Notes:



1. The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper.
2. The data tested by pulsed , pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$
3. The EAS data shows Max. rating . The test condition is $V_{DD}=25\text{V}, V_{GS}=10\text{V}, L=0.1\text{mH}, I_{AS}=20\text{A}$
4. The power dissipation is limited by 150°C junction temperature.
5. The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

P-Channel Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{V}, I_D=-250\mu\text{A}$	-30	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-30\text{V}, V_{GS}=0\text{V}$	-	-	-1	μA
Gate to Body Leakage Current	I_{GSS}	$V_{DS}=0\text{V}, V_{GS}=\pm 20\text{V}$	-	-	± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=-250\mu\text{A}$	-1	-1.6	-2.5	V
Static Drain-Source On-Resistance ³	$R_{DS(on)}$	$V_{GS}=-10\text{V}, I_D=-10\text{A}$	-	16	25	m Ω
		$V_{GS}=-4.5\text{V}, I_D=-5\text{A}$	-	25	40	
Input Capacitance	C_{iss}	$V_{DS}=-15\text{V}, V_{GS}=0\text{V}, f=1\text{MHz}$	-	1240	-	pF
Output Capacitance	C_{oss}		-	151	-	
Reverse Transfer Capacitance	C_{rss}		-	138	-	
Total Gate Charge(-10V)	Q_g	$V_{GS}=-10\text{V}, V_{DS}=-15\text{V}, I_D=-6\text{A}$	-	24	-	nC
Gate-Source Charge	Q_{gs}		-	3.7	-	
Gate-Drain Charge	Q_{gd}		-	4.8	-	
Turn-On Delay Time	$T_{d(on)}$	$V_{GS}=-10\text{V}, V_{DD}=-15\text{V},$ $R_G=3\Omega, I_D=-10\text{A}$	-	11	-	ns
Rise Time	T_r		-	5.5	-	
Turn-Off Delay Time	$T_{d(off)}$		-	3.5	-	
Fall Time	T_f		-	4.6	-	
Diode Forward Voltage	V_{SD}	$V_{GS}=0\text{V}, I_S=-10\text{A}$	-	-	-1.2	V
Continuous Source Current	I_S	-	-	-	-30	A
Source Diode Forward Current	I_{SM}	-	-	-	-40	A

Notes:

1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.
2. EAS condition: $T_J=25^\circ\text{C}$, $V_{DD}=-15\text{V}$, $V_{GS}=-10\text{V}$, $R_G=25\Omega$, $L=0.1\text{mH}$, $I_{AS}=-27\text{A}$.
3. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.



N-Channel Typical Characteristics

Figure1: Output Characteristics

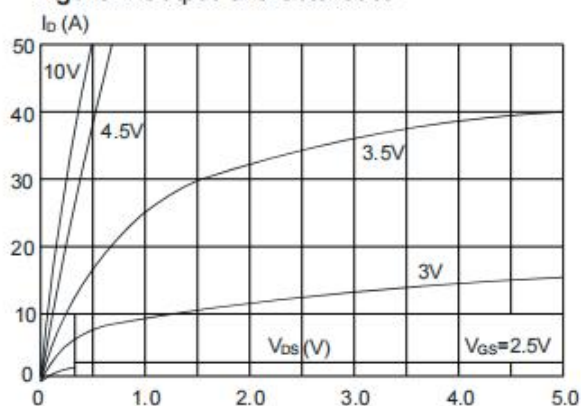


Figure 2: Typical Transfer Characteristics

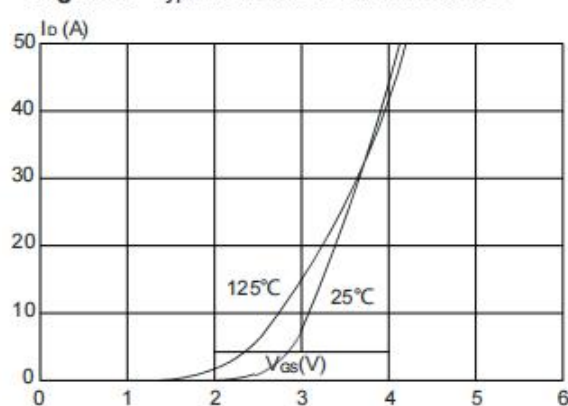


Figure 3: On-resistance vs. Drain Current

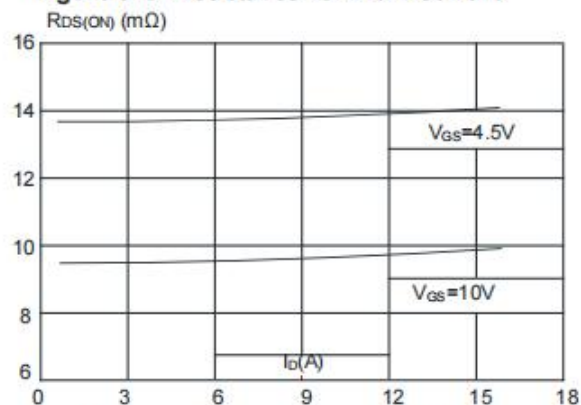


Figure 4: Body Diode Characteristics

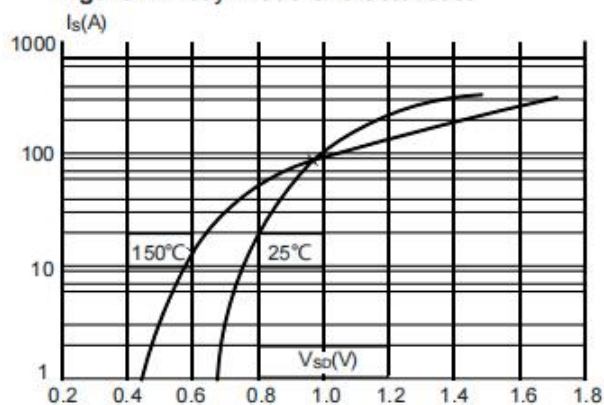


Figure 5: Gate Charge Characteristics

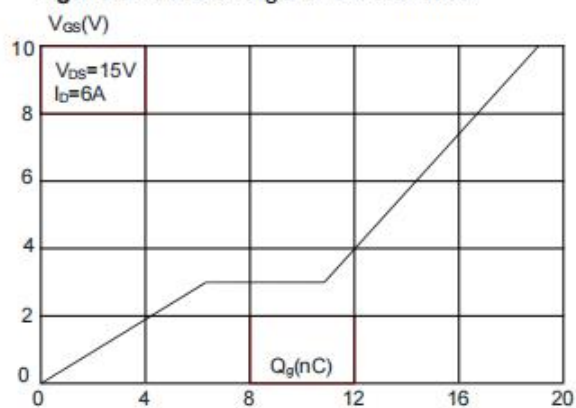
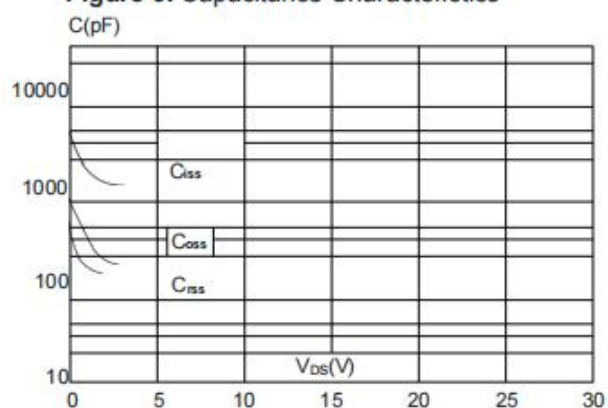
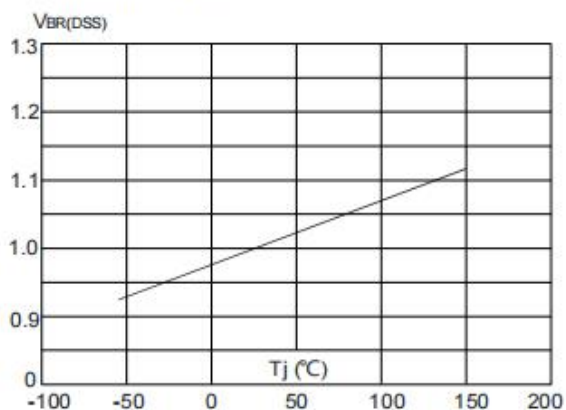
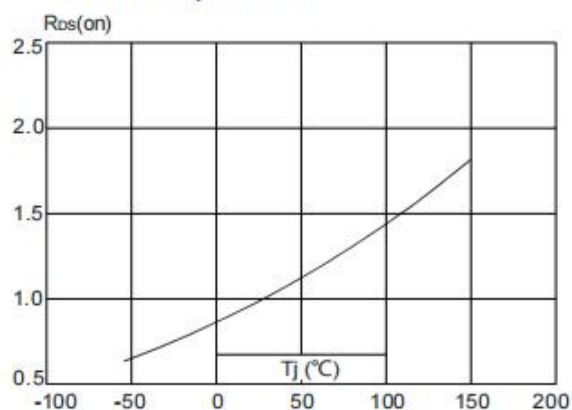
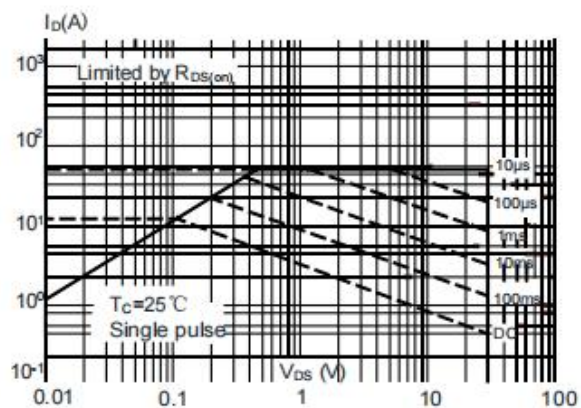
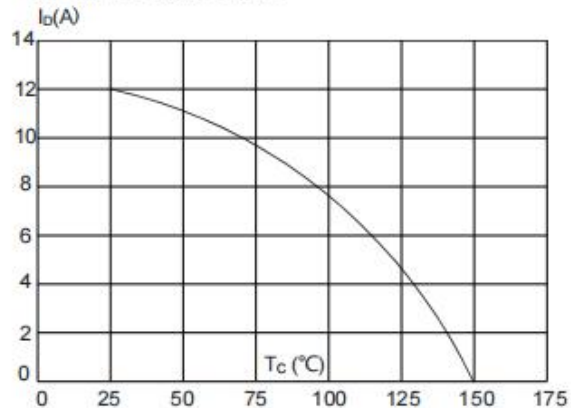
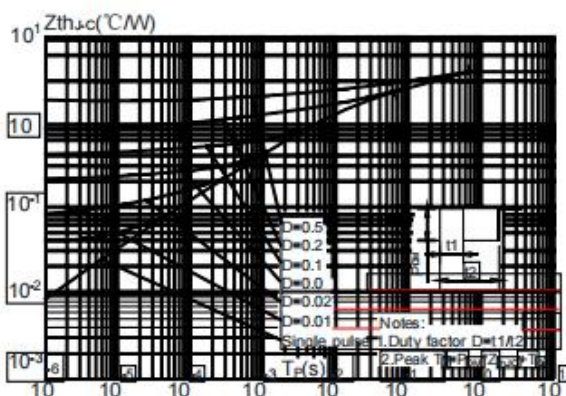


Figure 6: Capacitance Characteristics



**Figure 7:** Normalized Breakdown Voltage vs. Junction Temperature**Figure 8:** Normalized on Resistance vs. Junction Temperature**Figure 9:** Maximum Safe Operating Area**Figure 10:** Maximum Continuous Drain Current vs. Case Temperature**Figure.11:** Maximum Effective Transient Thermal Impedance, Junction-to-Case



P-Channel Typical Characteristics

Figure 1: Output Characteristics

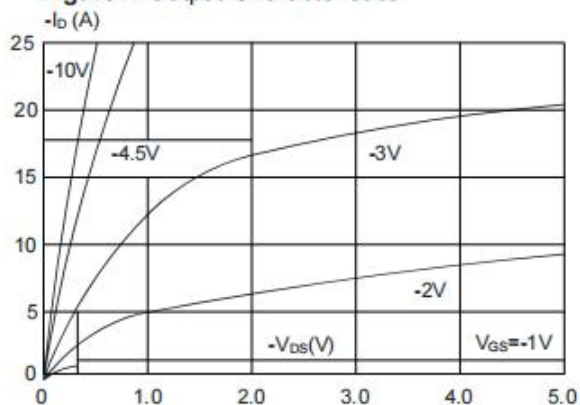


Figure 2: Typical Transfer Characteristics

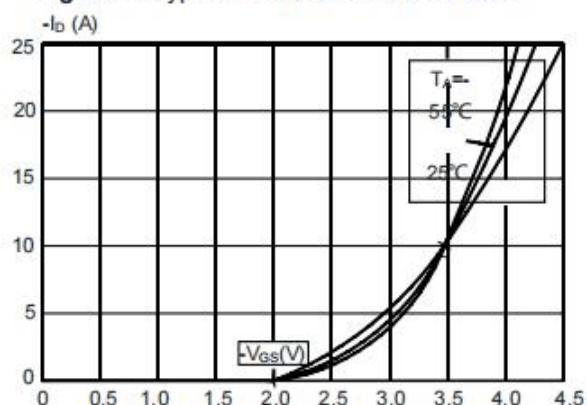


Figure 3: On-resistance vs. Drain Current

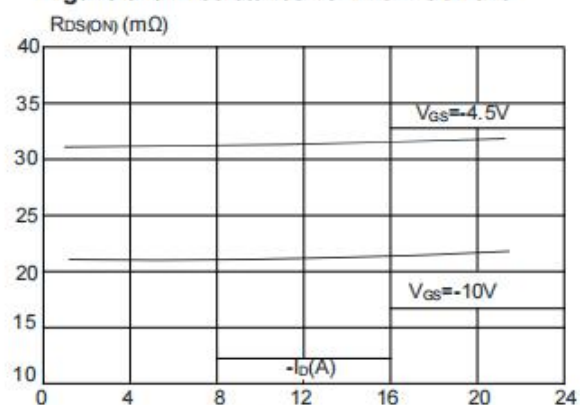


Figure 4: Body Diode Characteristics

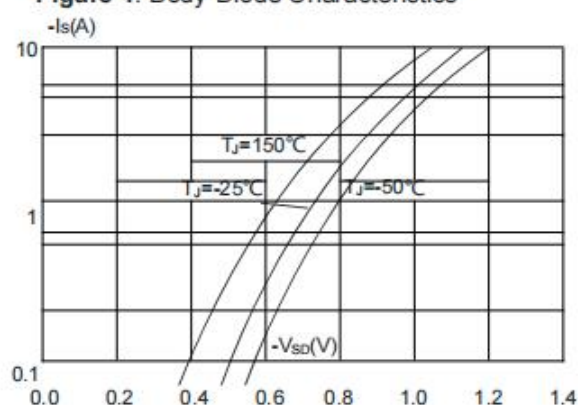


Figure 5: Gate Charge Characteristics

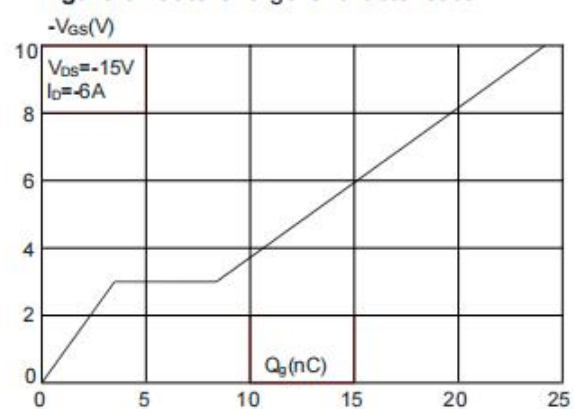
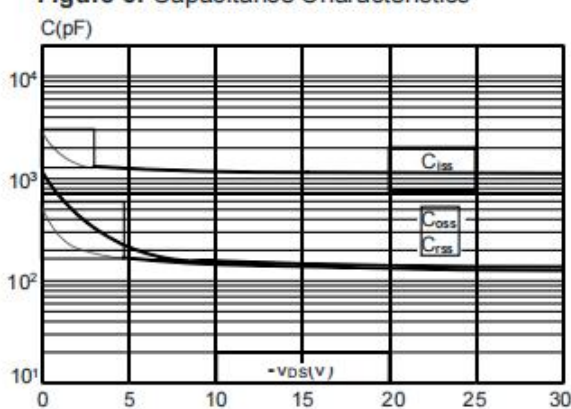
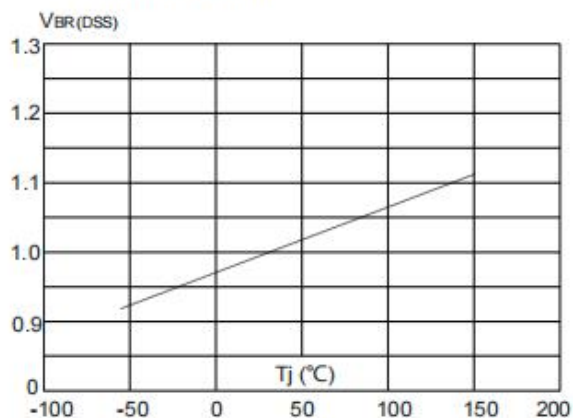
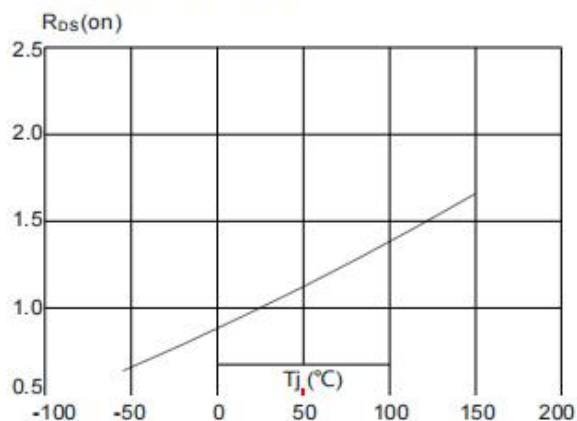
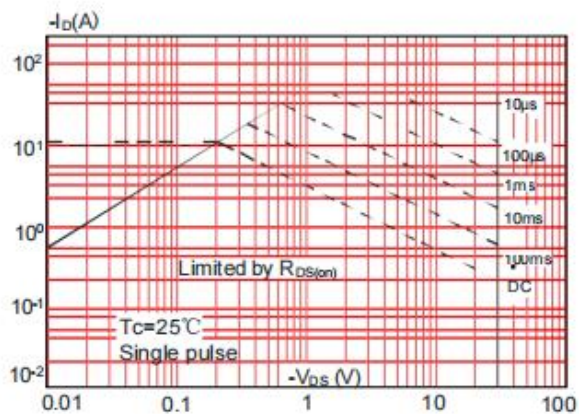
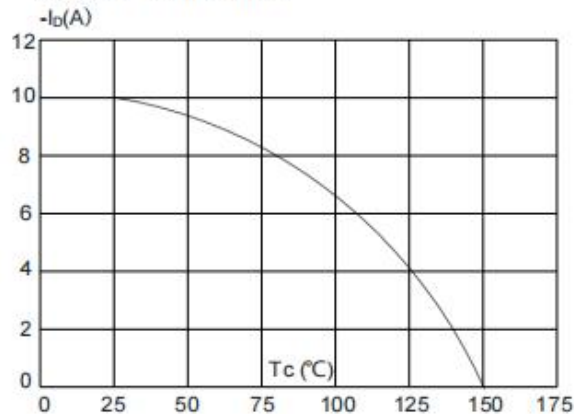
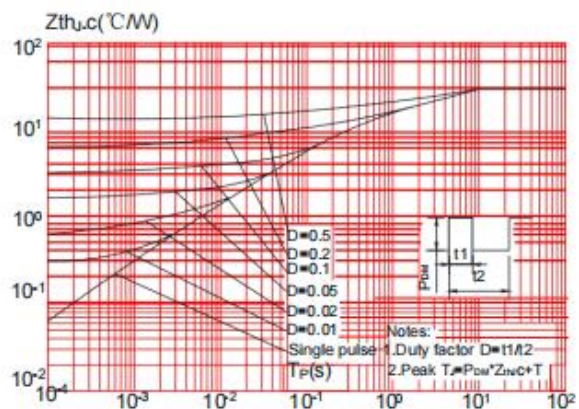


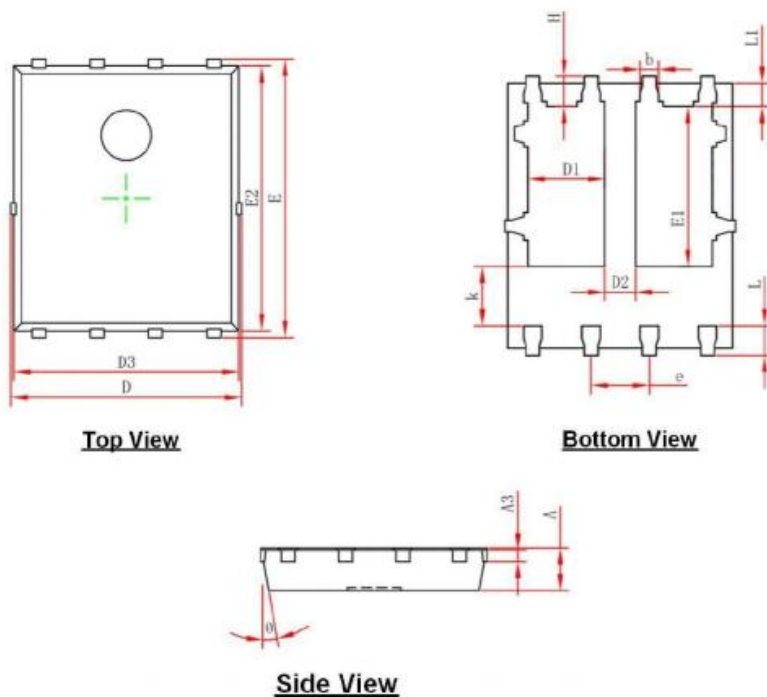
Figure 6: Capacitance Characteristics



**Figure 7:** Normalized Breakdown Voltage vs. Junction Temperature**Figure 8:** Normalized on Resistance vs. Junction Temperature**Figure 9:** Maximum Safe Operating Area**Figure 10:** Maximum Continuous Drain Current vs. Case Temperature**Figure 11:** Maximum Effective Transient Thermal Impedance, Junction-to-Case



Package Dimensions PDFN5x6-8L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.154REF.		0.006REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	1.470	1.870	0.058	0.074
D2	0.470	0.870	0.019	0.034
E1	3.375	3.575	0.133	0.141
D3	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
θ	10°	12°	10°	12°

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Chip revision change

Date	Revision	Remarks