



钜地半导体
Tudi Semiconductor

Product Specification

TUDI-PCF8563

I²C Real-Time Clock/Calendar Chip

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**semiconductor device
manufacturer**

- Design
- research and development
- production
- and sales



Features

- Operating voltage: 1.0 V to 5.5 V ($T_{amb}=25^{\circ}\text{C}$)
- 400 kHz I²C bus interface ($V_{DD}=1.8\text{V}$ to 5.5V)
- Programmable clock output frequency:
● 32.768KHz、1024Hz、32Hz、1Hz
- Internal Integrated Oscillator Capacitor
- Alarm and Timer Functions
- Internal Power Reset Function (POR)
- Open the leakage interrupt output pin
- The ²C bus reads from address-0A3H and writes to address-0A2H.
- Low sleep current: Typical value is 0.25 μA ($V_{DD}=3\text{V}$ at 25 $^{\circ}\text{C}$)

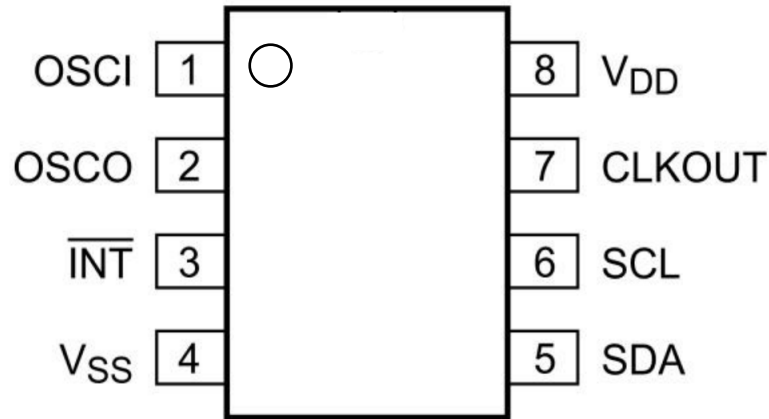


Figure 1. Pin Diagram

Description

The PCF8563 is a low-power CMOS real-time clock/calender chip that provides a programmable clock output, an interrupt output, and a power loss detector. All addresses and data are transmitted serially via the I²C bus interface with a maximum bus speed of 400 Kbit/s. After each data read/write operation, the built-in word address register automatically increments. It finds wide application in mobile phones and other devices. Battery-powered products such as portable instruments, fax machines, etc.

The primary packaging formats used are SOP8 and MSOP8.

Applications

- Mobile phones
- Portable instruments
- Electronic metering
- Battery-powered products

Pin description

number	symbol	function	number	symbol	function
1	OSCI	Oscillator Input	5	SDA	Local Serial Data Input/Output
2	OSCO	Oscillator output	6	SCL	Serial clock input
3	$\overline{\text{INT}}$	Interrupt (open-drain: valid at low level)	7	CLKOUT	Clock output (open drain)
4	Vss	Ground	8	VDD	Power supply voltage



Typical Application Diagram

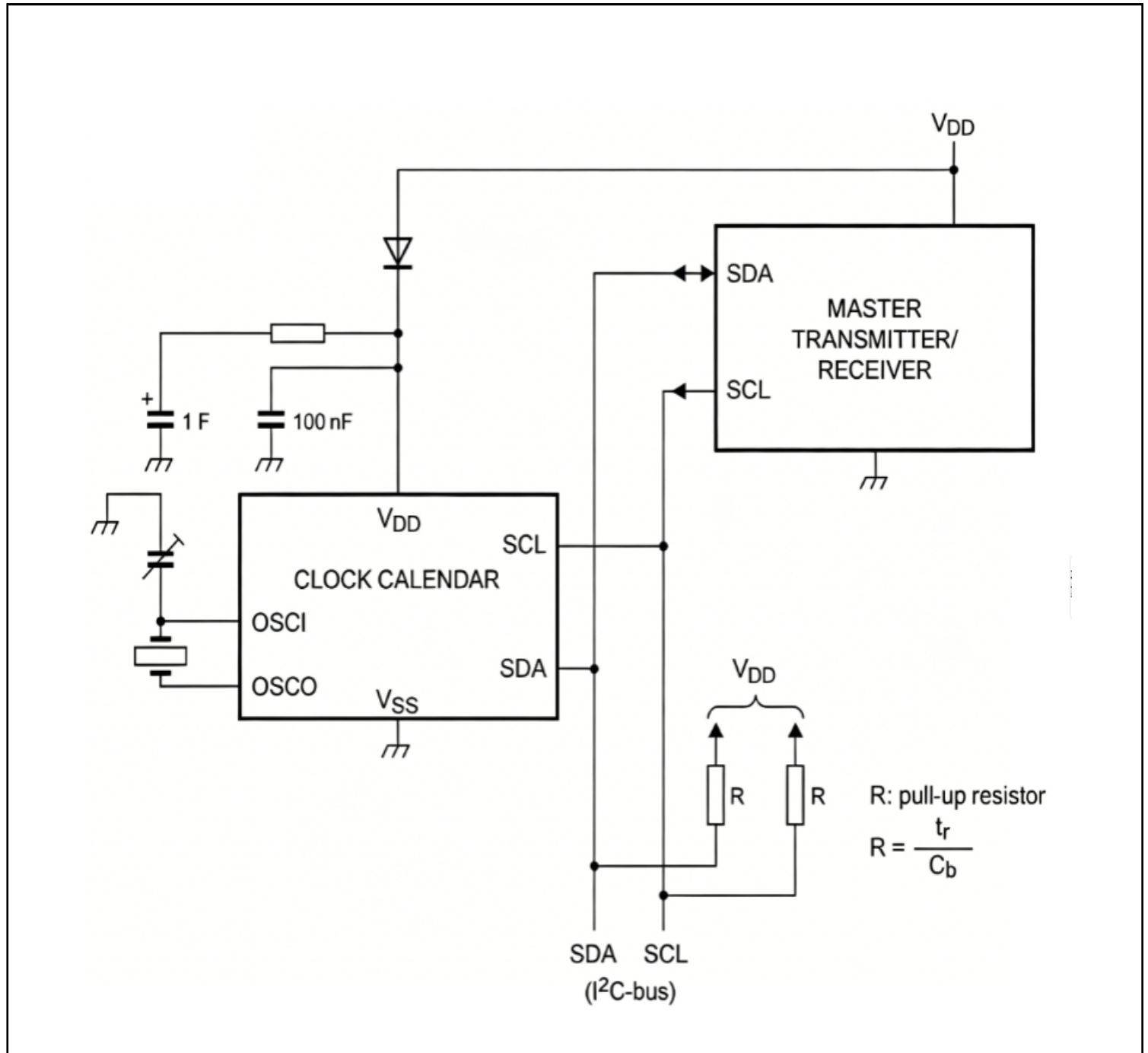


Figure 2: Typical Application Diagram



Internal Diode Protection Block Diagram

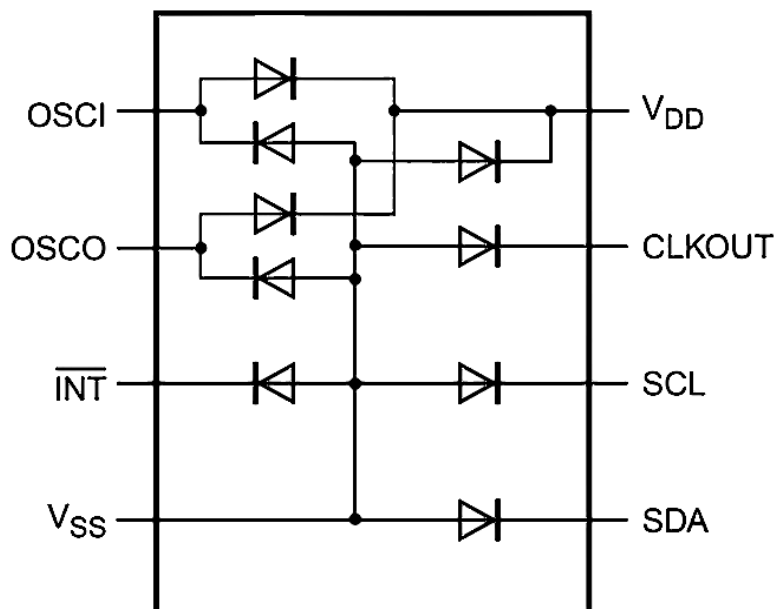


Figure 3: Block Diagram of the Internal Diode Protection Circuit

Maximum Limit Parameter

(Unless otherwise specified, $T_{amb} = +25^{\circ}\text{C}$)

Parameter	Symbol	Condition	Least value	Crest value	Unit
Supply voltage	V_{DD}	-	-0.5	+6.5	V
Source current	I_{DD}	-	-50	+50	mA
Input voltage	V_I	SCL, SDA, OSCI Pins	-0.5	+6.5	V
Output voltage	V_O	$\overline{INT}$, CLKOUT Pins	-0.5	+6.5	V
Input current	I_I	Any input pin	-10	+10	mA
Output	I_O	Any output pin	-10	+10	mA
Total Power Dissipation	P_D	-	-	300	mW
Working temperature	T_{amb}	Chip Operating Environment	-40	85	$^{\circ}\text{C}$
Storage Temperature	T_{stg}	-	-65	150	$^{\circ}\text{C}$
Electrostatic discharge voltage	V_{ESD}	HBM	-4000	+4000	V

Note: Exceeding the above limit values may cause permanent damage to the chip.



Static Characteristic

(Unless otherwise specified, $T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{DD} = 1.8$ to 5.5 V , $V_{SS} = 0\text{ V}$; $F_{osc} = 32.768\text{ kHz}$; quartz chip $R_s = 40\text{ K}\Omega$, $C_L = 8\text{ pF}$)

Symbol	Parameter	Condition		Least value	Typ	Crest value	Unit
Source							
V _{DD}	Working voltage	T _{amb} =+25℃	I2C bus invalid	1.0	—	5.5	V
		f _{SCL} =400KHz	I2C bus is active	1.8	—	5.5	V
	Data Maintenance Voltage	T _{amb} =+25℃		V _{LOW}	—	5.5	V
I _{DD1}	Working Current 1	f _{SCL} =400KHz	V _{DD} =5V	—	—	800	uA
		f _{SCL} =100KHz	V _{DD} =5V	—	—	200	uA
I _{DD2}	Working Current 2: CLOCKOUT failure (FE=0)	f _{SCL} =0Hz T _{amb} =+25℃	V _{DD} =5V	—	275	550	nA
			V _{DD} =3V	—	250	500	nA
			V _{DD} =2V	—	225	450	nA
		f _{SCL} =0Hz T _{amb} =-40 ~ +85℃	V _{DD} =5V	—	500	750	nA
			V _{DD} =3V	—	400	650	nA
			V _{DD} =2V	—	400	600	nA
			I _{DD3}	Working Current 3: CLOCKOUT active (FE=1)	f _{SCL} =0Hz F _{CLOCKOUT} =32KHz T _{amb} =+25℃	V _{DD} =5V	—
V _{DD} =3V	—	550				1000	nA
V _{DD} =2V	—	425				800	nA
f _{SCL} =0Hz F _{CLOCKOUT} =32KHz T _{amb} =-40 ~ +85℃	V _{DD} =5V	—			950	1700	nA
	V _{DD} =3V	—			650	1100	nA
	V _{DD} =2V	—			500	900	nA
Import							
V _{IL}	Enter low-level voltage	—		V _{SS}	—	0.3V _{DD}	V
V _{IH}	Put high level voltage	—		0.7V _{DD}	—	V _{DD}	V
I _{LI}	Input leakage current	VI = VDD or VSS		-1	0	+1	uA
C _I	Input capacitance	—		—	—	7	pF
Output							
I _{OL}	SDA Output Drain Current	V _{DD} =5V, V _{OL} =0.4V		3	—	—	mA
I _{OL}	$\overline{\text{INT}}$ Output Drain Current			1	—	—	mA
I _{OL}	CLKOUT Output Drive Current			1	—	—	mA
I _{LO}	Output leakage current	VO = VDD or VSS		-1	0	+1	uA
Voltage detector							
V _{LOW}	Power Loss Detection Value	T _{amb} =+25℃		—	1.0	1.2	V



Note:

- (1) The oscillator starts reliably upon power-up: $V_{DD(\text{minimum value; upon power-up})} = V_{DD(\text{minimum value})} + 0.3 \text{ V}$;
- (2) Timer source clock = 1/60 Hz; SCL and SDA = V_{DD} .

Dynamic Characteristics

(Unless otherwise specified, $T_{\text{amb}} = -40$ to $+85^\circ\text{C}$, $V_{DD} = 1.8$ to 5.5 V , $V_{SS} = 0 \text{ V}$; $F_{\text{osc}} = 32.768 \text{ kHz}$; quartz chip $R_S = 40 \text{ K}\Omega$, $C_L = 8 \text{ pF}$)

Symbol	Parameter	Condition	Least value	Typ	Crest value	Unit
Agitator						
C_{OSCO}	OSCO parasitic capacitance	—	15	25	35	pF
Δf_{OSC}	Oscillator Stability	$\Delta V_{DD} = 200 \text{ mV}$, $T_{\text{amb}} = +25^\circ\text{C}$	—	0.2	—	ppm
Quartz crystal parameters ($F_{\text{osc}} = 32.768 \text{ kHz}$)						
R_S	Series resistor	—	—	—	40	$\text{K}\Omega$
C_L	Load capacitor	—	—	10	—	pF
C_T	OSCI Adjustable Capacitor	—	5	—	25	pF
CLKOUT output						
δ_{CLKOUT}	CLKOUT Output Duty Cycle	—	— ⁽¹⁾	50	—	%
I²C Bus Timing Characteristics⁽²⁾						
f_{SCL}	SCL clock frequency	—	— ⁽³⁾	—	400	KHz
$T_{\text{HD;STA}}$	Activation Condition Duration	—	0.6	—	—	us
$T_{\text{SU;STA}}$	Time of repeated startup	—	0.6	—	—	us
T_{LOW}	SCL Clock Low-Level Duration	—	1.3	—	—	us
T_{HIGH}	SCL Clock High Level Duration	—	0.6	—	—	us
T_R	Rising edge duration of SCL and SDA	—	—	—	0.3	us
T_F	Time of the decline edges for SCL and SDA	—	—	—	0.3	us
T_{BUF}	Stop and Start Bus Idle Time	—	1.3	—	—	us
C_b	Bus load capacitor	—	—	—	400	pF
$T_{\text{SU;DAT}}$	Data Generation Time	—	100	—	—	ns
$T_{\text{HD;DAT}}$	Data Retention Time	—	0	—	—	ns
$T_{\text{SU;STO}}$	Stop Condition Occurrence Time	—	4.0	—	—	ns
T_{SW}	Acceptable bus spike width	—	—	—	50	ns

Note:

- (1) Unless otherwise specified, $f_{\text{CLKOUT}} = 32.768 \text{ kHz}$;
- (2) All timing values are valid within the operating voltage range (T_{amb} condition), and the values of V_{IL} and V_{IH} when the reference input voltage varies between V_{SS} and V_{DD} .
- (3) The access time of the I^2C bus under both start conditions or one start and one stop condition must be less than one second.

Functional Description

The PCF8563 features 16 8-bit registers with automatically incrementing addresses, a 32.768 kHz oscillator with an integrated capacitor, a divider providing source clocks for the Real-Time Clock (RTC) and calendar functions, a programmable clock output, a timer, an alarm module, a low-voltage detector, and a 400 kHz I²C bus interface.

All 16 registers are designed as addressable 8-bit parallel registers, though not all bits are utilized. The first two registers (memory addresses 00h and 01h) serve as control/status registers; memory addresses 02h – 08h are used for clock function counters (from second to year counters); internal Memory address 09h – 0Ch is used for the alarm register (to define alarm conditions); memory address 0Dh controls the output frequency of CLKOUT; memory address Addresses 0Eh and 0Fh are used for the timer control register and timer count register, respectively. The registers for seconds, minutes, hours, days, months, years, minute alarms, hour alarms, and daily alarms use BCD encoding; the day and week alarm registers do not use BCD encoding. When an RTC register is written to or read from, all counter contents are latched. This prevents erroneous reading or writing of the clock and calendar registers under transmission conditions.

Control/State Register 1

Bit	Symbol	Price	Description
7,6,5	0	0	Default value setting logic:0
4	TI_TP	TI_TP=0	When TF is active, __ INT is active(depending on the TIE state)
		TI_TP=1	The $\overline{\text{INT}}$ pulse is valid;refer to Table3 (depending on the TIE state).
3	AF	00-1	When an alarm occurs,AF is set to logic 1 and TF is set to logic 1 upon timer countdown completion;these values remain unchanged until software overwrites them,as the software cannot set both to logic 1 simultaneously. When both the timer and alarm interrupts are triggered,the interrupt source is determined by AF and TF.To clear one flag while preventing the other from being overwritten,use the logical AND operation;the values of flags AF and TF are specified in Reference Table4
2	TF	00-1	
1	AIE	AIE=0	Alarming interruption failed
		AIE=1	The alarm interruption is valid.
0	TIE	TIE=0	Timer interrupt is invalid
		TIE=1	Timer interrupt is enabled

Note: If both AF and AIE are valid, __ INT remains valid.

Table 1: Control and Status Registers – 2-Bit Description (Address 01h)



Control/State Register 2

Bit	Symbol	Price	Description
7	TEST1	TEST1=0	Normal Mode
		TEST1=1	EXT_CLK Test Mode
5	STOP	STOP=0	Chip clock operation
		STOP=1	All chip dividers are set to logic 0 asynchronously, and the chip clock stops operating. CLKOUT available at 32.768 kHz
3	TESTC	TESTC=0	Power reset function failed (set to logic 0 in normal mode)
		TESTC=1	Power reset function is effective
6,4,2,1,0	0	0	Default value setting logic:0

Table 2: Control/State Register 1-Bit Description (Address 00h)

Source Clock(Hz)	$\overline{\text{INT}}$ Cycle	
	n=1	N>1
4096	1/8192	1/4096
64	1/128	1-64
1	1-64	1-64
1-60	1-64	1-64

Table 3: $\overline{\text{INT}}$ Operation (Bit TI_TP=1)

Note:

(1) TF and INT Are Both Valid;

(2) n is the value of the countdown timer; when n = 0, the timer stops working.

Time and Data Register

Bit	Symbol	Price	Description
7	VL	0	Ensure accurate clock/calender data
		1	Cannot guarantee accurate clock/calender data
6-0	Second	00~59	Represents the actual second value in BCD format. For example: 1011001 represents 59 seconds.

Table 4: Description of the Second/VL Register Bit (Address 02h)



Low-voltage detector and clock monitoring

The PCF8563 has an embedded low voltage detector. When V_{DD} drops below V_{LOW} , the VL (Voltage Low, bit 7 the seconds register) is set to 1 to indicate that inaccurate clock/calendar information may be generated. The VL flag can only be cleared by software. When V_{DD} slowly drops (.g., battery-powered) to V_{LOW} , the VL flag is set, which may generate a Low interrupt.

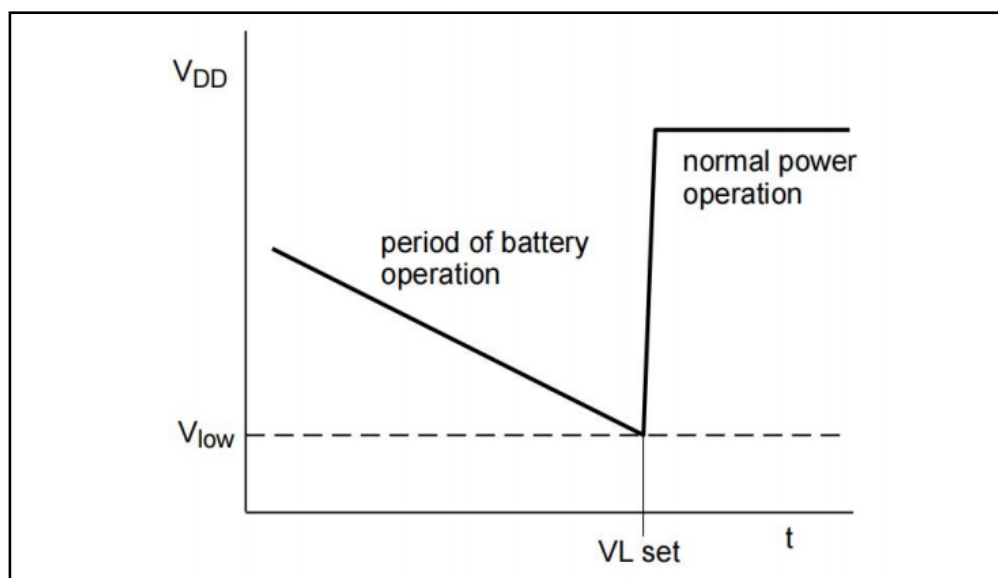


Figure 4 Low-Voltage Detector

Bit	Symbol	Price	Description
7	—	—	Of no avail
6-0	Minute	00 ~ 59	Represents the actual minute value in BCD format. For example: 1011001 represents 59 minutes.

Table 5: Description of the Minute Register Bits (Address 03h)

Bit	Symbol	Price	Description
7-6	—	—	Of no avail
5-0	Hour	00 ~ 23	Represents the actual minute value in the BCD format. For example: 100011 represents 23 hours.

Table 6: Description of Hour Register Bits (Address 04h)

Bit	Symbol	Price	Description
7-6	—	—	Of no avail
5-0	Sun	01 ~ 31	Represents the actual day value in BCD format. For example: 110001 represents day 31.

Note: If the current counter value is for a leap year, the PCF8563 automatically increments it by one for February, making it 29 days.

Table 7: Day Register Bit Description (Address 05h)



Bit	Symbol	Price	Description
7-3	—	—	Of no avail
2-0	Week	0 ~ 6	Actual day number; see the table below

Table 8: Week Register Bit Description (Address 06h)

Week	Bit		
	2	1	0
Sunday	0	0	0
Monday	0	0	1
Tuesday	0	1	0
Wednesday	0	1	1
Thursday	1	0	0
Friday	1	0	1
Saturday	1	1	0

Table 9: Week Allocation Table

Bit	Symbol	Price	Description
7	C	0	Show century value as X
		1	Show century value as X+1
6-5	—	—	Of no avail
4-0	Moon	01 ~ 12	Represents the actual month value in BCD format. For example: 10010 represents December.

Table 10: Month/S Century Register Bit Descriptions (Address 07h)

Bit	Symbol	Price	Description
7-0	Year	0-9	Represents the actual year value in BCD format. For example: 10011001 represents the year 99.

Note: If the value in the year register changes from 99 to 00, the century bit will change.

Table 11: Year Register Bit Description (Address 08h)



Register Structure

Address	Registry Name	Bit							
		7	6	5	4	3	2	1	0
Control/State Register									
00h	Control/State Register 1	TEST1	0	STOP	0	TESTC	0	0	0
01h	Control/State Register 2	0	0	0	TI_IP	AF	TE	AIE	TIE
Time and Data Register									
02h	Second	VL	00 ~ 59 BCD encoding format						
03h	Minute	x	00 ~ 59 BCD encoding format						
04h	Hour	x	x	00 ~ 23 BCD encoding format					
05h	Sun	x	x	01 ~ 31 BCD encoding format					
06h	Week	x	x	x	x	x	0 ~ 6		
07h	Month/S century	C	x	x	01–12 BCD encoding format				
08h	Year	00 ~ 99 BCD encoding format							
Alarm Register									
09h	Minute-level Alert	AE_M	00 ~ 59 BCD encoding format						
0Ah	Hourly Alert	AE_H	x	00 ~ 23 BCD encoding format					
0Bh	Daily Report	AE_D	x	01 ~ 31 BCD encoding format					
0Ch	Weekday Alert	AE_W	x	x	x	x	0 ~ 6		
CLKOUT Frequency Register									
0Dh	CLKOUT Frequency Register	FE	x	x	x	x	x	FD1	FD0
Timer Register									
0Eh	Timer Control Register	TE	x	x	x	x	x	TD1	TD0
0Fh	Timer Countdown Value Register	Timer Countdown Value							

Note: Bits marked "x" are invalid; bits marked "0" should be set to logical 0. To read data, the state can be either logical 0 or logical 1.

Table 12: Overview of Registers

Bit	Symbol	Price	Description
7	AE_M	0	The minute alarm is active.
		1	Minute alarm is invalid
6-0	Minute-level Alert	00 ~ 59	Represents the minute alarm value in BCD format. For example: 1011001 represents 59 minutes.

Table 13: Description of Minute Alarm Register Bits (Address 09h)



Alarm Register

Registers from 09h to 0Ch contain alarm information. When one or more alarm registers are written with valid minutes, hours, days, or weeks.

When the values match and the corresponding AE_X is set to logical 0, this information is compared with the current minute, hour, day, and day of the week. If the values match, AF is set to logical 1, and AF retains the configured value until cleared by the software.

After AF is cleared, AF can only be re-enabled when the time increment matches the alarm condition again. If the corresponding AE_X is set to logic 1, the alarm register will be ignored.

Bit	Symbol	Price	Description
7	AE_H	0	The hourly alarm is effective.
		1	The hourly alarm is invalid
6	—	—	Of no avail
5-0	Hourly Alert	00 ~ 23	Represents the hourly alarm value in BCD format. For example: 100011 represents 23:00.

Table 14: Description of Hour Alarm Register Bits (Address 0Ah)

Bit	Symbol	Price	Description
7	AE_D	0	The daily alarm is effective.
		1	Daily alarm is invalid
6	—	—	Of no avail
5-4	Daily Report	00 ~ 31	Represents the daily alarm value in BCD format, for example: 110001 represents 31 days

Table 15: Description of Daily Alarm Register Bits (Address 0Bh)

Bit	Symbol	Price	Description
7	AE_W	0	The weekly alarm is active.
		1	The weekly alarm is invalid.
6-3	—	—	Of no avail
2-0	Weekday Alert	0 ~ 6	Weekly alarm values, refer to Table 10

Table 16: Description of Week Alarm Register Bits (Address 0Ch)



CLKOUT Frequency Register

The CLKOUT pin outputs a programmable square wave, with its frequency determined by the CLKOUT frequency register (address 0Dh; see Reference Table 18). CLKOUT supports square waves at 32.768 kHz (default), 1024 Hz, 32 Hz, or 1 Hz. CLKOUT is an open-drain output pin that remains active when powered and exhibits high impedance when inactive.

Bit	Symbol	Price	Description
7	FE	0	The CLKOUT output is suppressed and set to high impedance.
		1	CLKOUT output is valid
6-2	—	—	Of no avail
1-0	FD[1:0]	CLKOUT Output Frequency	
		00	32.768KHz
		01	1024Hz
		10	32Hz
		11	1Hz

Table 17: Description of CLKOUT Frequency Register Bits (Address 0Dh)

Timer Register

The 8-bit timer countdown value register (address 0Fh) is controlled by the timer control register (address 0Eh), which sets the timer frequency (4096 Hz, 64 Hz, 1 Hz, or 1/60 Hz) and determines whether the timer is enabled or disabled. The timer starts with a software-defined 8-bit binary countdown value; at the end of each countdown cycle, it sets the flag TF (see Table 1), which can only be cleared via software.

The configured TF generates an interrupt at pin INT, producing one pulse per countdown cycle as the interrupt signal. TI_TP (see Table 1) controls the conditions for interrupt generation. When reading the timer, it returns the current countdown value.

To accurately read the countdown value, it is recommended to read it twice and verify the result; specifically, the frequency of the I²C bus clock (SCL) should be at least twice that of the selected timer clock frequency.

Bit	Symbol	Price	Description
7-0	Timer Countdown Value	00h-FFh	Countdown value "n" Countdown period = n / clock frequency

Table 18. Description of Timer Countdown Value Register Bits (Address 0Fh)

Bit	7	6	5	4	3	2	1	0
Timer Countdown Value	128	64	32	16	8	4	2	1

Table 19: Timer Countdown Values



Bit	Symbol	Price	Description
7	TE	0	Timer is invalid
		1	Timer is active
6-2	—	—	Of no avail
1-0	TD[1:0]	Timer Clock Frequency	
		00	4096Hz
		01	64Hz
		10	1Hz
		11	1/60Hz

Table 20: Description of Timer Control Register Bits (Address 0Eh)

EXT_CLK Test Mode

The test mode is used for online testing to establish test parameters and control RTC operations. The test mode is set via the TEST1 bit in Control/State Register 1, at which point the CLKOUT pin serves as the input pin. In test mode, the frequency signal applied to the CLKOUT pin replaces the chip's internal 64 Hz signal, generating a one second time increment for every 64 rising edges. The pulse width of the frequency signal input to the CLKOUT pin shall be no less than 300 ns, with a maximum period not exceeding 1000 ns. The chip's internal 64 Hz clock is divided into 1 Hz by a 2⁶ presplitter upon receiving the frequency signal at the CLKOUT pin. The presplitter can be set to a known state via the STOP parameter; setting STOP allows the presplitter to reset to 0 (STOP must be cleared before the presplitter resumes operation).

After entering the STOP state, when 32 rising edges are input to the CLKOUT pin, a 1-second time increment is generated for the first time. Thereafter, a 1-second time increment is generated every 64 rising edges.

Note: In EXT_CLK test mode, the clock does not synchronize with the chip's internal 64 Hz clock, and the presplitting state cannot be determined.

Operation Example

- (1) Enter Ext_CLK test mode (bit 7 of Control/Status Register 1, TESE1 = 1)
- (2) Set STOP (bit 5 of control/status register 1: STOP=1)
- (3) Clear Stop (bit 5 of Control/Status Register 1: STOP=0)
- (4) Set the time register (seconds, minutes, hours, days, weeks, months/centuries, and years) to the desired value
- (5) Provide 32 clock pulses to the CLKOUT pin
- (6) Observe the first change in the time register
- (7) Provide 64 clock pulses to the CLKOUT pin
- (8) To observe the second change in the time register, repeat steps 7 and 8 when you need to read the additional increment from the time register.



RESET

PCF8563 includes an internal reset circuit that activates when the oscillator stops operating. In the reset state, the I²C bus is initialized, including the address pointer, and all registers are set according to Table 21. Communication on the I²C bus is unavailable during the reset period.

Address	Registry Name	Bit							
		7	6	5	4	3	2	1	0
00h	Control/State Register 1	0	x	0	x	1	x	x	x
01h	Control/State Register 2	x	x	x	0	0	0	0	0
02h	Second /VL	1	x	x	x	x	x	x	x
03h	Minute	x	x	x	x	x	x	x	x
04h	Hour	x	x	x	x	x	x	x	x
05h	Sun	x	x	x	x	x	x	x	x
06h	Week	x	x	x	x	x	x	x	x
07h	Month/S century	x	x	x	x	x	x	x	x
08h	Year	x	x	x	x	x	x	x	x
09h	Minute-level Alert	1	x	x	x	x	x	x	x
0Ah	Hourly Alert	1	x	x	x	x	x	x	x
0Bh	Daily Report	1	x	x	x	x	x	x	x
0Ch	Weekday Alert	1	x	x	x	x	x	x	x
0Dh	Clock Frequency Control	1	x	x	x	x	x	0	0
0Eh	Timer Control	0	x	x	x	x	x	1	1
0Fh	Timer Countdown Value	x	x	x	x	x	x	x	x

Note: Registers marked with x are not defined when powered on and remain unchanged upon reset.

Table 21: Register Reset Values

Power Reset (POR) Failure Mode

The duration of POR is directly related to the oscillator's startup time. An embedded circuit with extended startup capability can disable POR, thereby enhancing device testing speed. Setting this mode requires the signal waveforms at I²C bus pins SDA and SCL as shown in the figure below, with all time values being the minimum required values.

Once failure mode is activated, the chip immediately stops operating and transitions to EXT_CLK test mode via the I²C bus. To clear failure mode, set the TESTC bit to logic 0; reactivating failure mode requires setting TESTC to logic 1 again. In normal operation, setting TESTC to logic 0 is meaningless unless intended to prevent entry into POR failure mode.

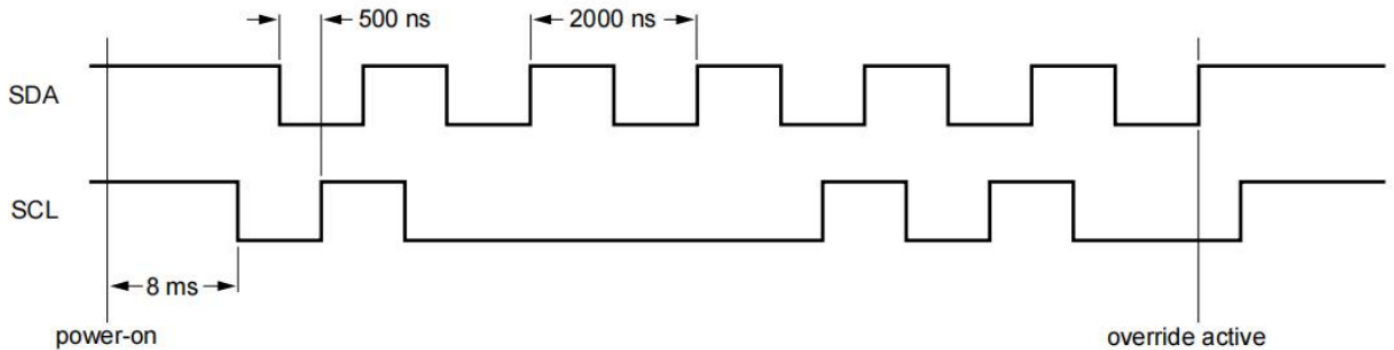


Figure 5: Time Sequence Diagram of POR Failure

Serial Interface

The serial interface of PCF8563 is the I²C bus

I²C Bus Characteristics

The I²C bus uses two lines to transmit data between the chip and modules: the Serial Data Line (SDA) and the Serial Clock Line (SCL). Both lines must be connected to the positive power supply via a pull-up resistor, and data can only be transmitted when the bus is not busy.

The system configuration is shown in the figure below: the signal-generating device is the transmitter, the signal-receiving device is the receiver, the control signal device is the master device, and the devices controlled by it are slave devices.

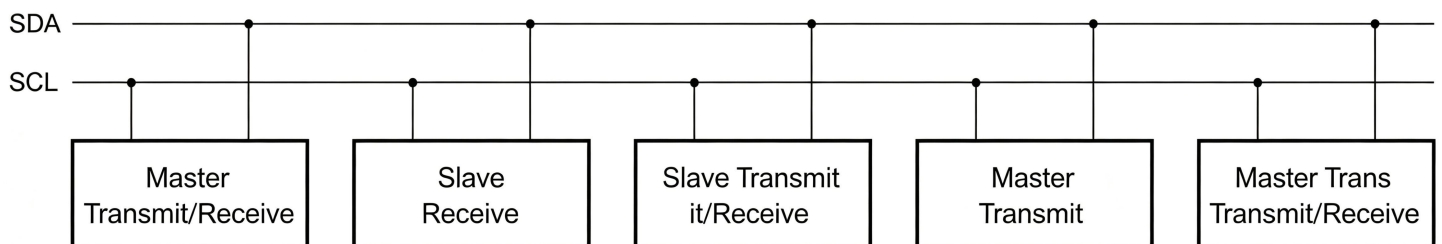


Figure 6 Configuration Diagram of the I²C Bus System

Start (START) and Stop (STOP) Conditions

As shown in the figure below, when the bus is not busy, both the data line and clock line remain high. The data line is at its falling edge while the clock line remains high—this state is the start condition (S); the data line is at its rising edge while the clock line remains high—this state is the stop condition (P).

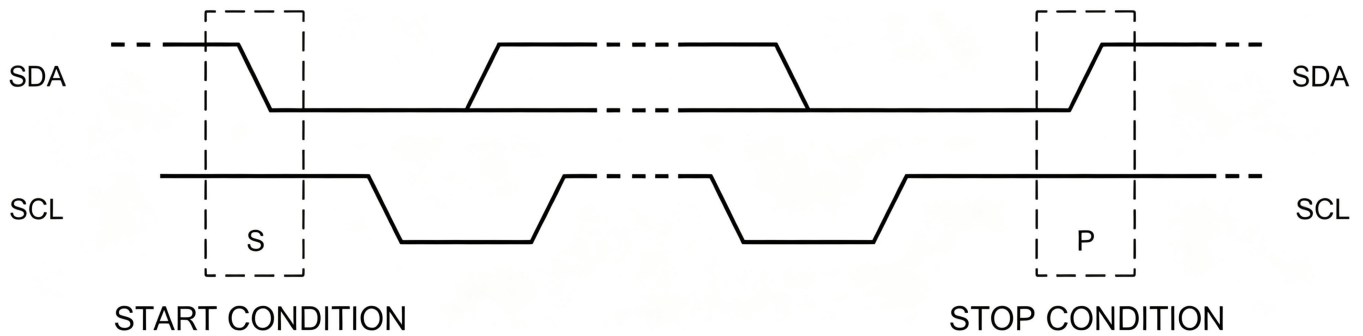


Figure 7: Starting and Stopping Conditions of the I²C Bus

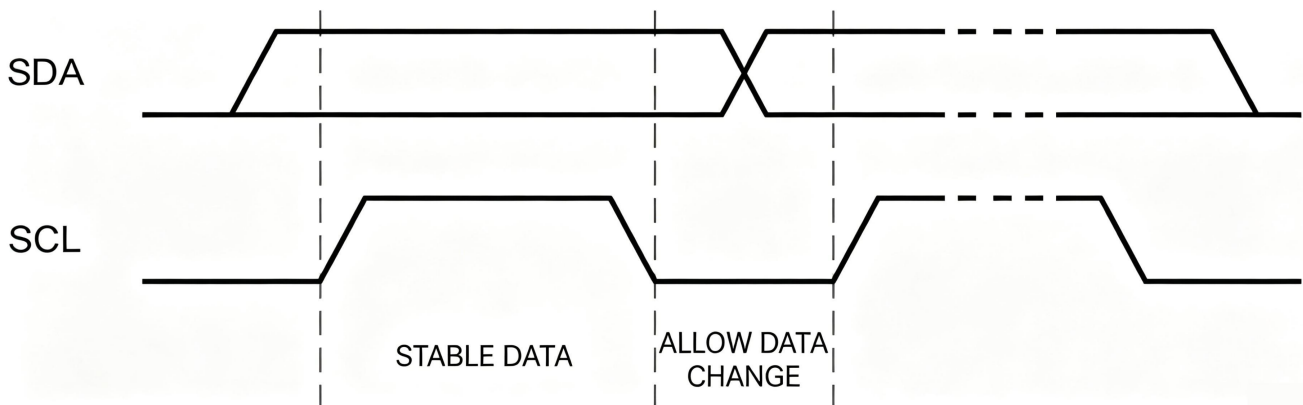


Figure 8: I²C Bus Bit Transmission

Bit Transfer

As shown in the figure below, each clock pulse transmits one data bit. The data on the data line (SDA) must remain unchanged during the high-level phase of the clock pulse; otherwise, it will be interpreted as a control signal.

Bit Zone

Between startup and stop conditions, the amount of data transmitted from the transmitter to the receiver is unlimited. A flag bit is added every 8 bytes; when this flag bit reaches a high level, the master device generates an additional flag clock pulse. For each byte received by the receiver, a flag bit must be generated immediately thereafter; similarly, for each byte received from the transmitter, the master receiver must also generate a flag bit promptly. When the flag clock pulse occurs, the SDA line must remain low (accounting for start and hold times). The transmitter should switch to a low level upon receiving the final byte from the slave device, prompting the receiver to generate the flag signal; this enables the master device to initiate the stop condition (see figure below).

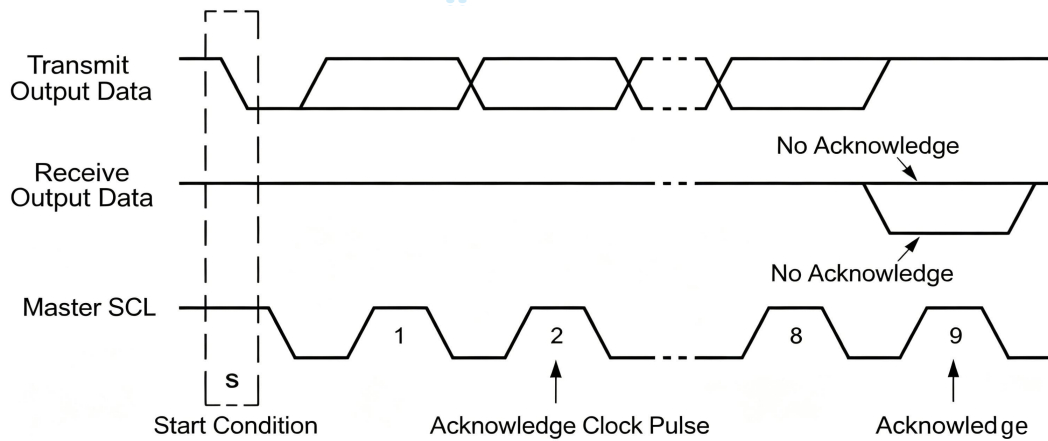


Figure 9 I²C Bus Flag Bits

I²C Bus Protocol

Before transmitting data via the I²C bus, the receiving device must first specify its address; once the I²C bus is activated, this address is transmitted along with the first byte. The PCF8563 can function as either a receiver or a transmitter, in which case the clock signal line (SCL) serves solely as an input line, while the data signal line (SDA) is a bidirectional line.

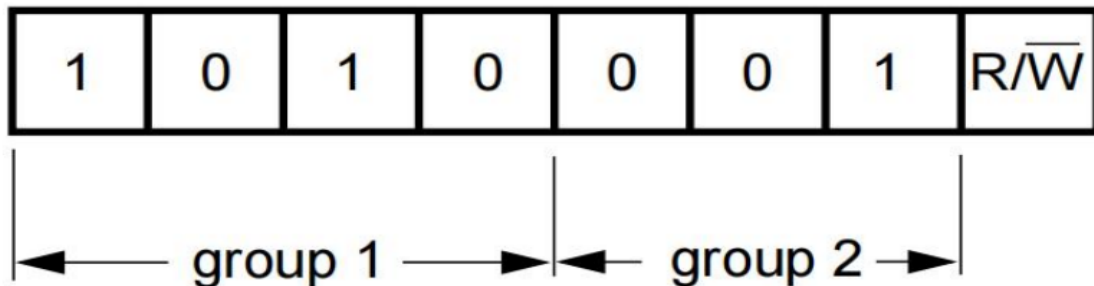


Figure 10 From Address

The configuration of the I²C bus during the clock/calendar chip's read/write cycles is illustrated in the following three diagrams. The word address (a four-bit value) specifies the register to be accessed next, with its high four bits being unused.

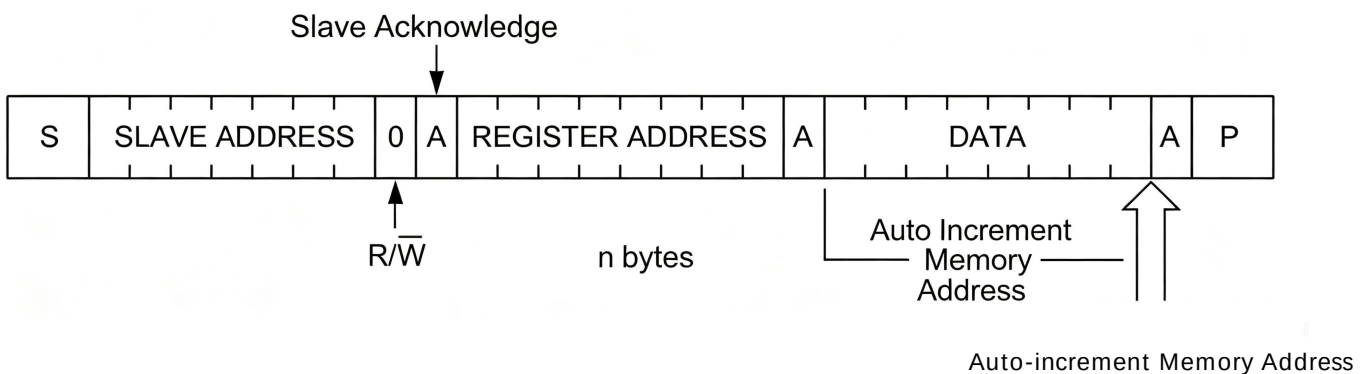


Figure 11 Main Transmitter to Slave Receiver (write Mode)

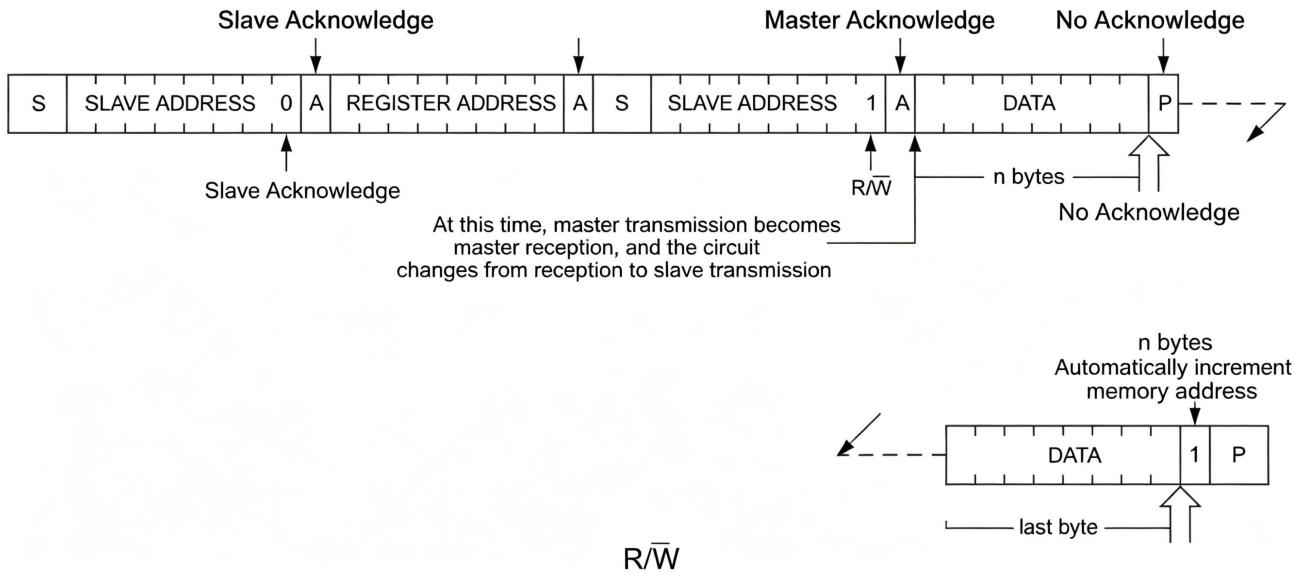


Figure 12: After Setting the Word Address, the Master Device Reads Data (write Address: Read Data)

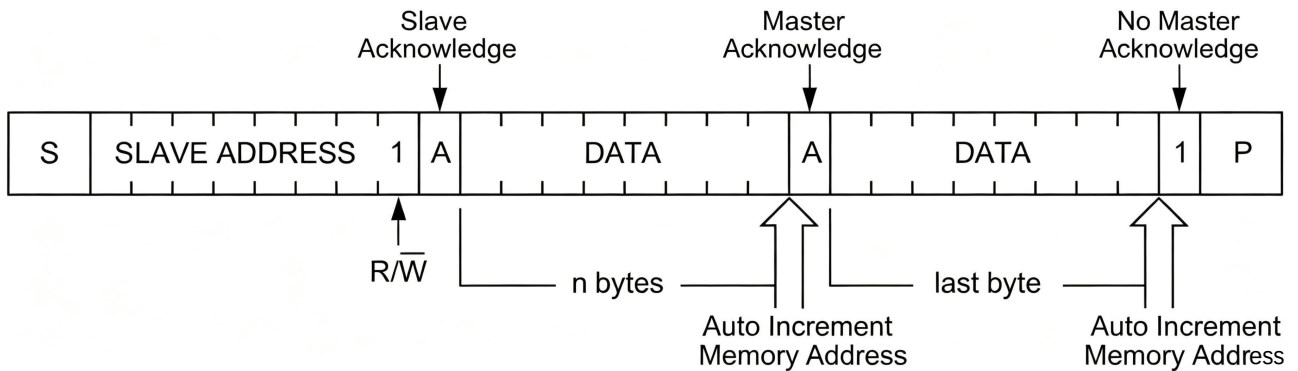
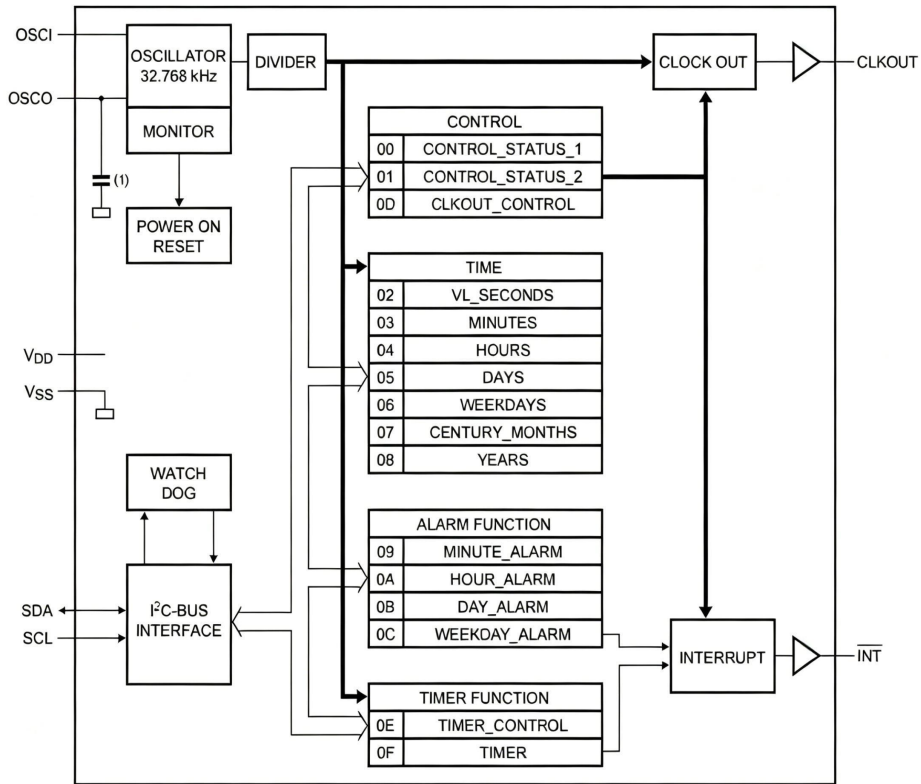


Figure 13 Data After the Main Device Reads the First Byte from the Slave Device (read Mode)



Internal Function Block Diagram



Order information

Order Number	Package	Package Quantity	Marking On The park	Temperature
PCF8563T/F4,118-TUDI	SOP8	Tape,Reel,4000	8563T	-40°C to +85°C



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