

P-Channel High Cell Density Trenched MOSFET

PRIMARY CHARACTERISTICS

BV_{DSS}	$R_{DS(ON)MAX}$	I_D
-20V	125m Ω @ $V_{GS} = -4.5V$	-3
	190m Ω @ $V_{GS} = -2.5V$	

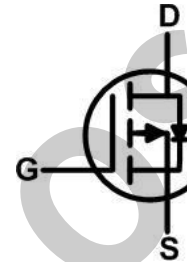
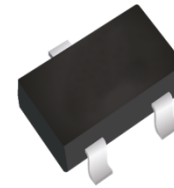
Features

- P-Channel Enhancement Mode MOSFET
- -20V / -3A, $R_{DS(on)} < 125m \Omega$ @ $V_{GS} = -4.5V$
- $R_{DS(on)} < 190m \Omega$ @ $V_{GS} = -2.5V$
- Super low gate charge
- Excellent CdV/dt effect decline
- High power and current handling capability
- RoHS compliant, Green device

Mechanical Data

- Package: SOT-23
- Surface mount package
- Pin configuration: see diagram
- Marking: see device marking

SOT-23



Applications

- Synchronous buck converter
- Load switch
- Power management
- Battery powered devices

Ordering Information

Orderable Part Number	Package Type	Device Marking	Form	Quantity (pcs)
DC2301H	SOT-23	-	7" Tape&Reel	3,000

Maximum Ratings (@ $T_A = 25^\circ C$, unless otherwise specified.)

Parameter	Symbol	Value	Unit
Drain - Source Voltage	V_{DS}	-20	V
Gate - Source Voltage	V_{GS}	± 12	V
Continuous Drain Current ($V_{GS} = 4.5V$) ⁽¹⁾	I_D	-3	A
		-1.4	A
Pulsed Drain Current ⁽²⁾	I_{DM}	-8	A
Power Dissipation	P_D	0.8	W
Junction & Storage Temperature Range	T_J, T_{STG}	-55 ~ +150	$^\circ C$

Thermal Characteristics

Parameter	Symbol	Typ.	Max.	Unit
Thermal Resistance, Junction-to-Ambient ⁽³⁾	$R_{\theta JA}$	-	156	$^\circ C/W$

Electrical Characteristics (@ $T_J = 25^\circ\text{C}$, unless otherwise specified.)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Off Characteristics ⁽⁴⁾						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	VGS=0V, ID=-250μA	-20	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	VDS=-20V, VGS = 0V,TJ=25°C	-	-	-1	μA
Gate-Source Leakage Current	I _{GSS}	VGS=±12V, VDS = 0V	-	-	100	nA
On Characteristics ⁽⁴⁾						
Gate Threshold Voltage	V _{GS(th)}	VDS=VGS, ID=-250μA	-0.4	-0.7	-1.0	V
Static Drain-Source On-Resistance	R _{DS(ON)}	VGS=-2.5V, ID=-1A	-	135	190	mΩ
		VGS=-4.5V, ID=-2A	-	60	125	mΩ
Diodes Forward Voltage	V _{SD}	IS=-2A, VGS=0V	-	-	-1.2	V
Dynamic Characteristics ⁽⁴⁾						
Input Capacitance	C _{ISS}	VDS=-10V, VGS=0V, f=1MHz	-	185	-	pF
Output Capacitance	C _{OSS}		-	35	-	pF
Reverse Transfer Capacitance	C _{RSS}		-	25	-	pF
Switching Characteristics ⁽⁵⁾						
Turn-On DelayTime	t _{d(on)}	VGS=-4.5V, VDD=-10V, ID=-2A, RGEN=3Ω	-	10	-	ns
Rise Time	t _r		-	30	-	ns
Turn-Off DelayTime	t _{d(off)}		-	63	-	ns
Fall Time	t _f		-	50	-	ns
Gate Charge Characteristics ⁽⁵⁾						
Total Gate Charge	Q _g	VDS=-10V,ID=-2A, VGS=-4.5V	-	2.2	-	nC
Gate-Source Charge	Q _{gs}		-	0.5	-	nC
Gate-Drain Charge	Q _{gd}		-	0.5	-	nC
Drain-Source Diode Characteristics ⁽⁵⁾						
Diode Forward Current	Is	TA = 25°C	-	-	-2.5	A
Maximum Pulsed Drain to Source Diode Forward Current	ISM	TA = 25°C	-	-	-8	A
Drain to Source Diode Forward Voltage	VSD	VGS=0V	-	-	-1.2	V
Notes:						
1. This current is chip limited, which is calculated based on Rthja.						
2. This current is calculated on single pulse with 10μs Single Pulse .						
3. Device mounted on FR-4 substrate PC board with 2oz copper in 1inch square cooling area.						
4. Short duration pulse test used to minimize self-heating effect.						
5. Defined by design, not subject to production.						

Typical Performance Characteristics

P- Channel Typical Characteristics

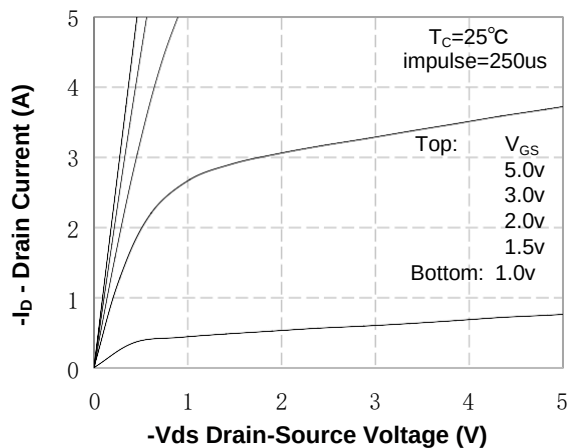


Figure 1. On-Region Characteristics

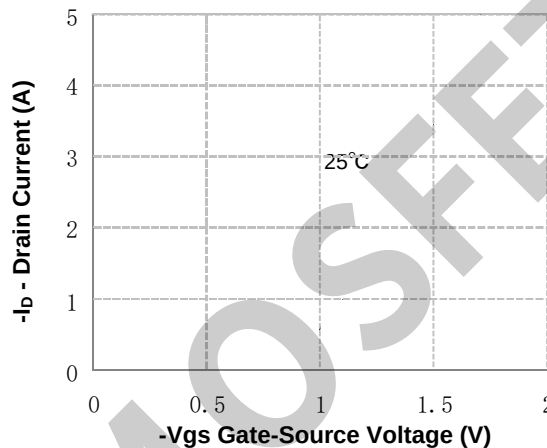


Figure 2. Transfer Characteristics

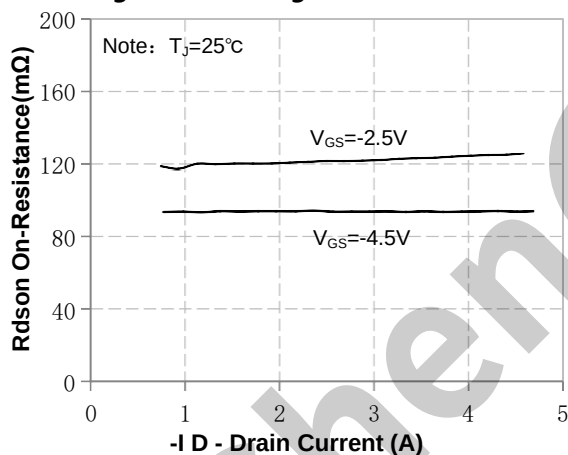


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

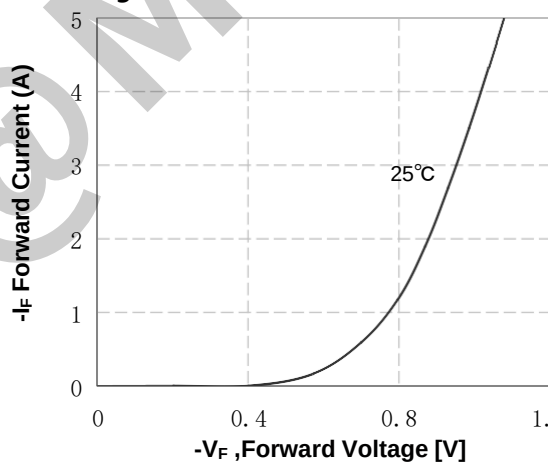


Figure 4. Body Diode Forward Voltage Variation with Source Current

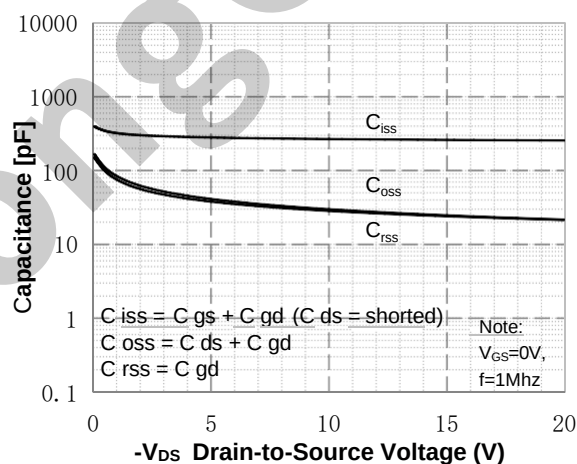


Figure 5. Capacitance Characteristics

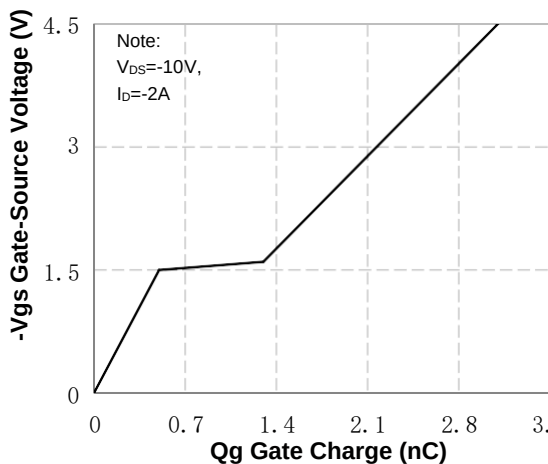


Figure 6. Gate Charge Characteristics

P- Channel Typical Characteristics

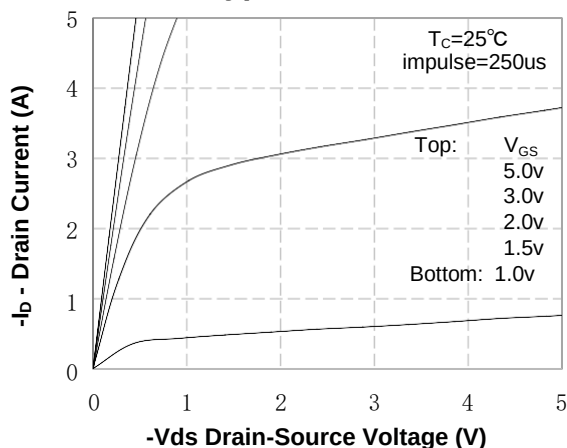


Figure 1. On-Region Characteristics

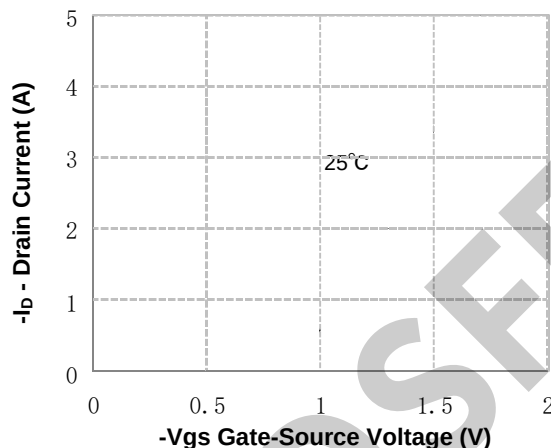


Figure 2. Transfer Characteristics

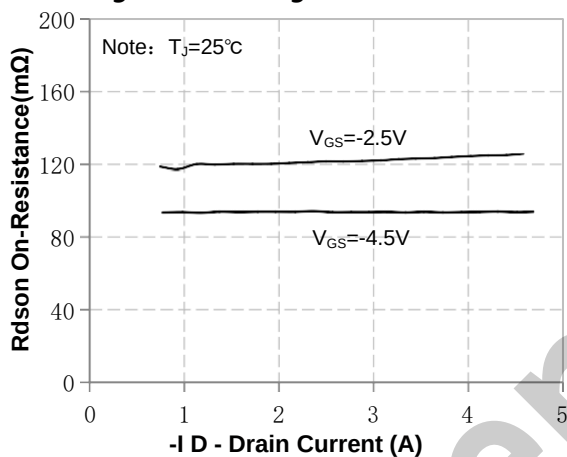


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

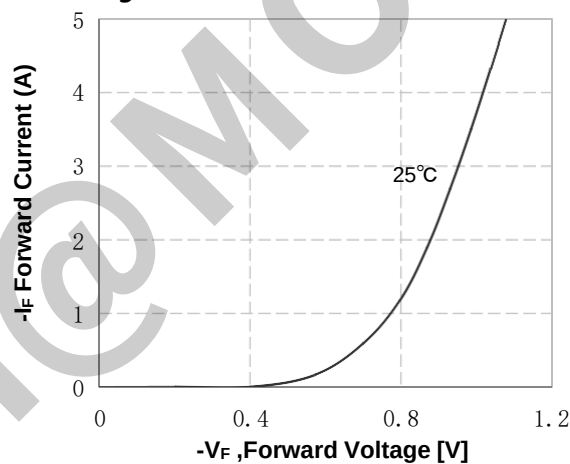


Figure 4. Body Diode Forward Voltage Variation with Source Current

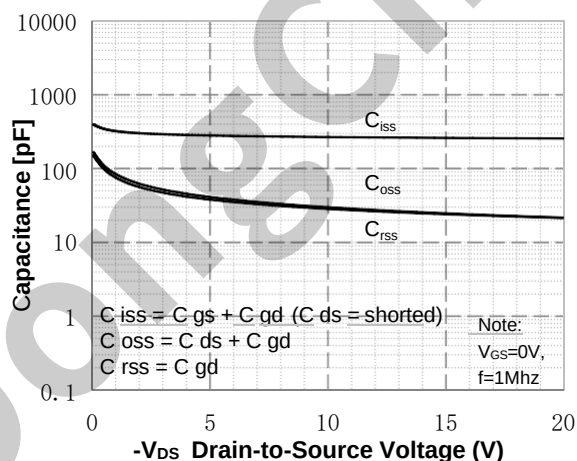


Figure 5. Capacitance Characteristics

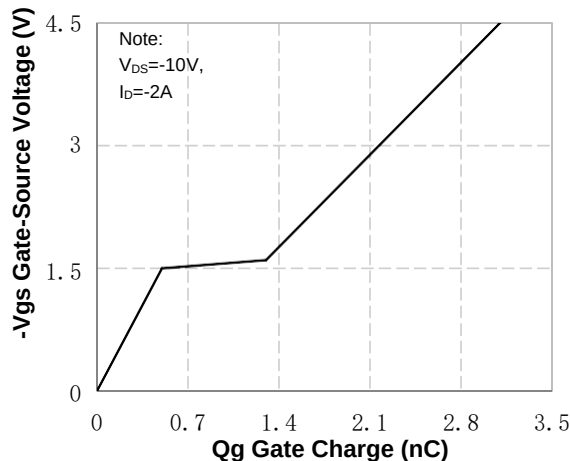
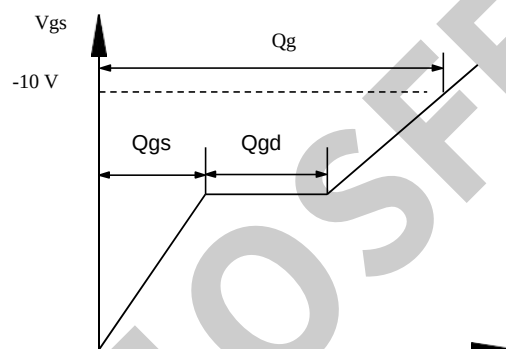
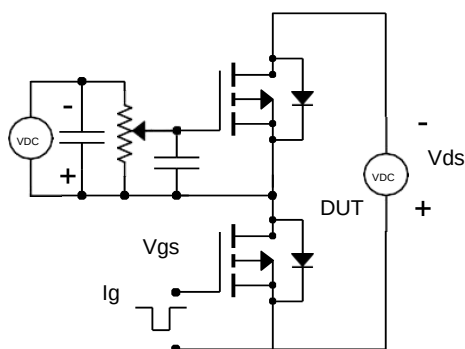


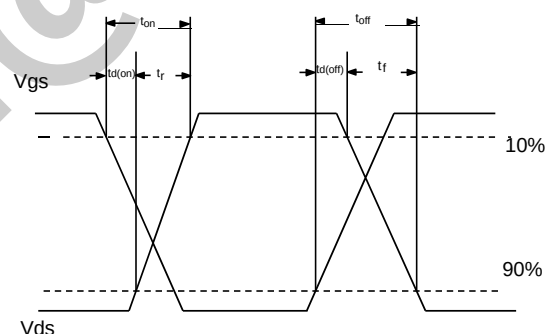
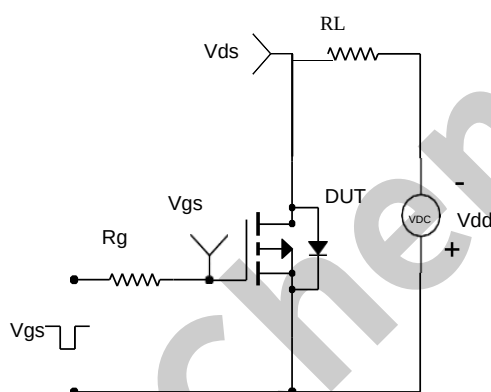
Figure 6. Gate Charge Characteristics

P- Channel

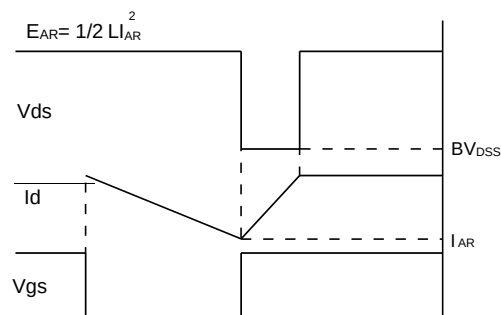
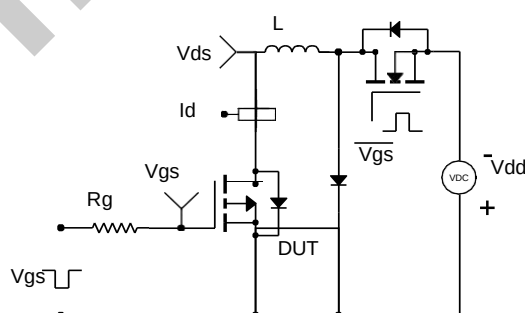
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms

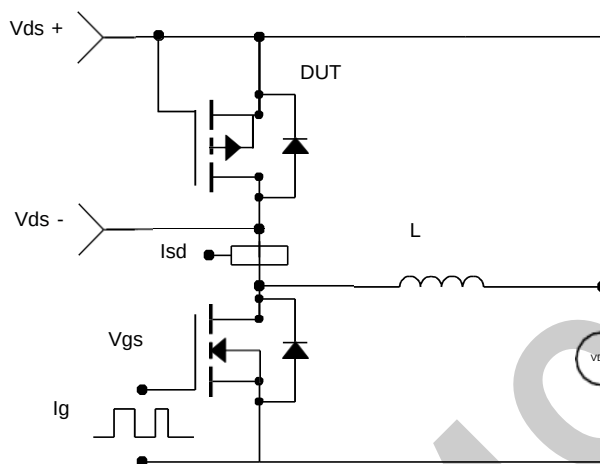


Unclamped Inductive Switching Test Circuit & Waveforms

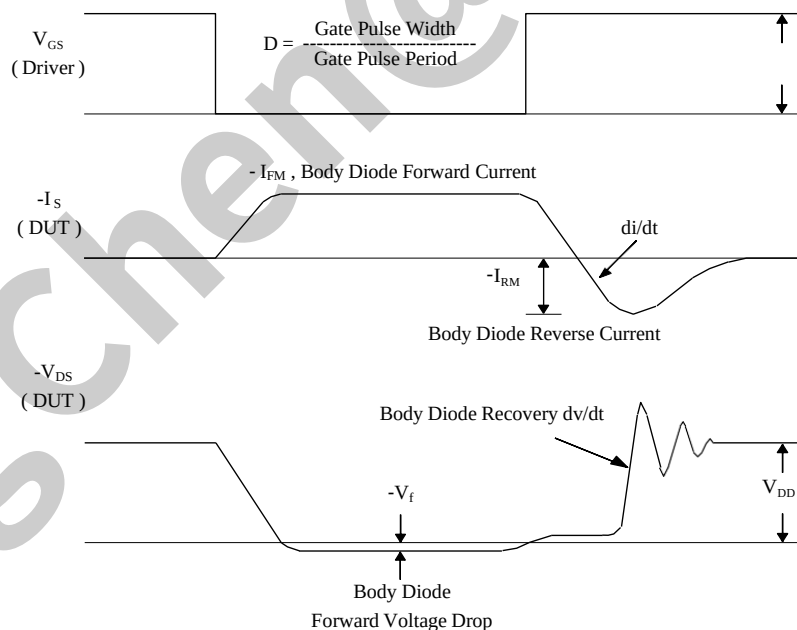


P- Channel

Peak Diode Recovery dv/dt Test Circuit & Waveforms

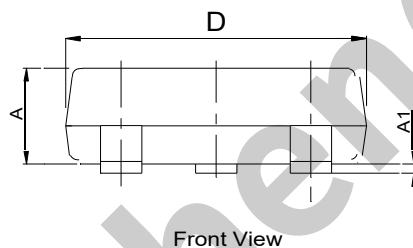
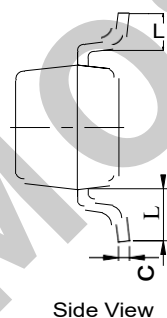
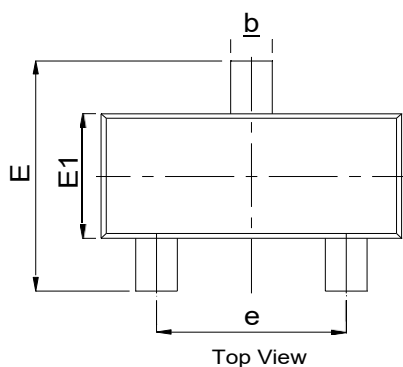


- dv/dt controlled by R_g
- I_{SD} controlled by pulse period



Outline Drawing

SOT-23

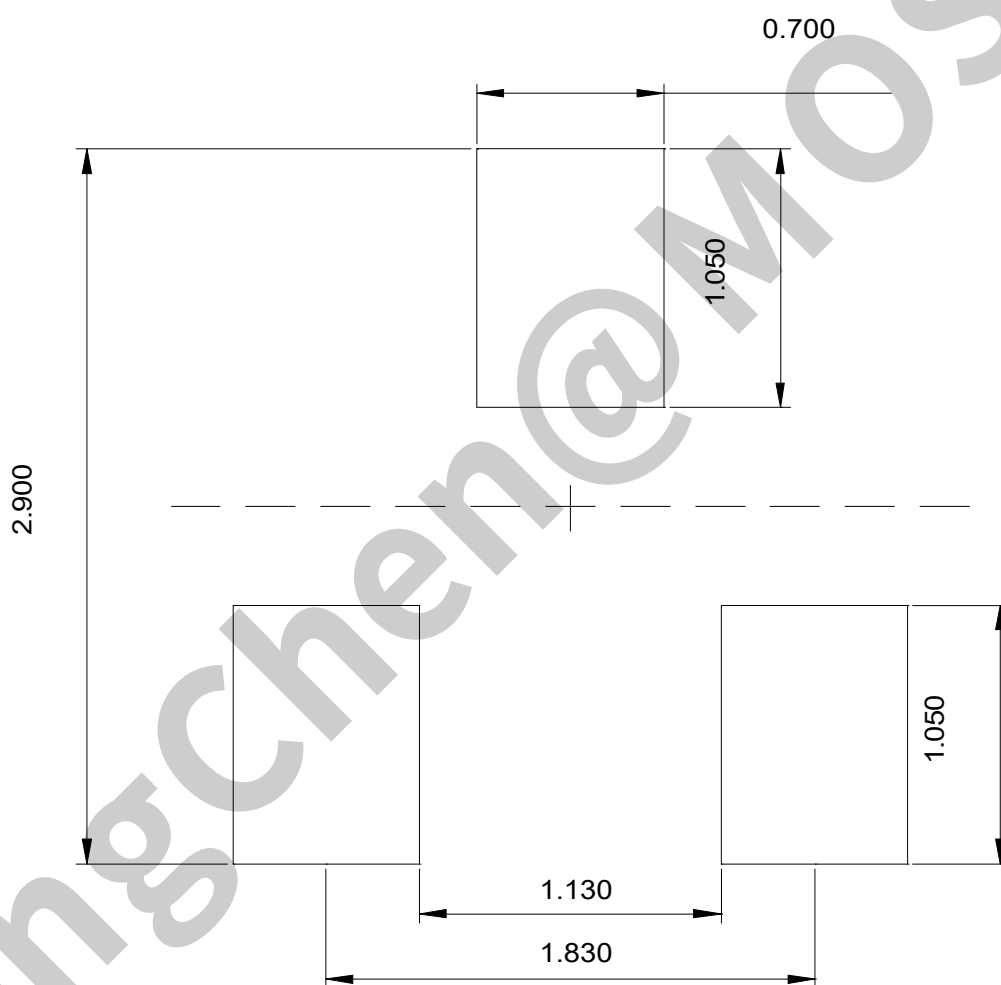


DIM.	MILLIMETER		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	-	0.10
D	2.80	2.90	3.00
E	2.30	2.40	2.50
E1	1.20	1.30	1.40
L	0.45	0.55	0.65
L1	0.20	-	0.55
b	0.30	0.40	0.50
c	-	0.10	0.15
e	-	1.90	-

Dimensions in inches and (millimeters)

Suggested Soldering Pad Layout

SOT-23



Dimensions in inches and (millimeters)

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