TLV2333IDR-HX Vos,0.02-pV/℃,17-μA,CMOS Operational Amplifiers Zero-Drift Series

Description

The TLV2333IDR-HX is a precision CMOS operational amplifier that delivers high-performance characteristics at a highly competitive price point. This device belongs to the zero-drift amplifier family and employs a proprietary auto-calibration technique to simultaneously achieve ultra-low input offset voltage (maximum 15 μV) and near-zero drift over time and temperature—all while consuming only 28 μA (maximum) of quiescent current. The TLV2333IDR-HX features rail-to-rail input and output capability, along with exceptionally flat 1/f noise performance, making it well-suited for a broad range of applications and significantly simplifying system integration.

These devices are optimized for low-voltage operation, supporting supply voltages as low as 1.8 V (±0.9 V) up to 5.5 V (±2.75 V).

The TLV2333IDR-HX (dual-channel version) is available in SOIC-8 packages. All versions are fully specified for operation across an extended industrial temperature range of –40 °C to +125 °C.

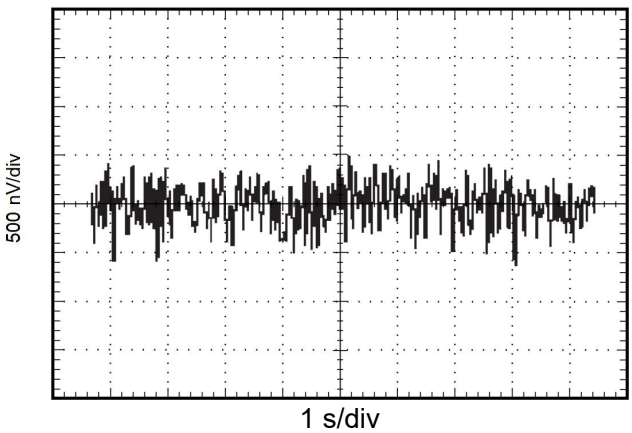
Features

- Unmatched Price Performance
- Low Offset Voltage: 2 μV
- Zero Drift: 0.02 μV/°C
- Low Noise: 1.1 μVPP, 0.1 Hz to 10 Hz
- Quiescent Current: 17 μA
- Supply Voltage: 1.8 V to 5.5 V
- Rail-to-Rail Input/Output
- Internal EMI Filtering
- microSize Packages: SOIC

Applications

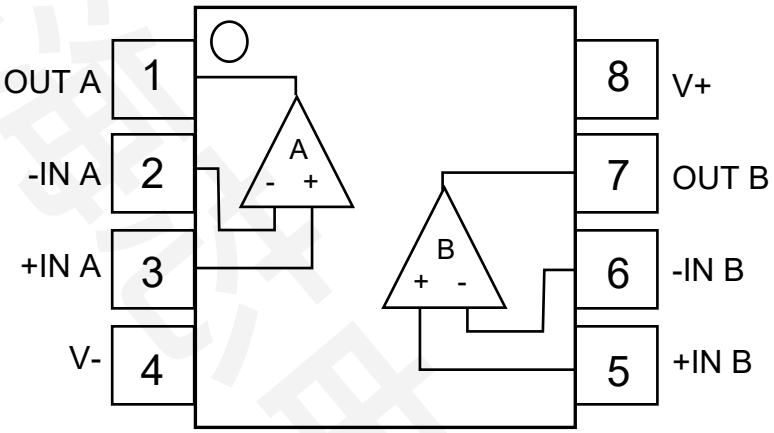
- Battery-Powered Instruments
- Temperature Measurements
- Transducer Applications
- Electronic Scales
- Medical Instrumentation
- Handheld Test Equipment
- Current Sense

0.1-Hz to 10-Hz Noise



Pin Configuration and Functions

8-Pin SOIC
Top View



Pin Functions: TLV2333IDR-HX

PIN		I/O	DESCRIPTION
NAME	NO. SOIC		
–IN A	2	I	Inverting input, channel A
+IN A	3	I	Noninverting input, channel A
–IN B	6	I	Inverting input, channel B
+IN B	5	I	Noninverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V–	4	__	Negative (lowest) power supply
V+	8	__	Positive (highest) power supply

Specifications

1. Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	V_S = (V+) – (V–)		7	V
Signal input pins(2)	Voltage	(V–) –0.3 0.3	(V+) +	V
	Current	–10 10		mA
Output short-circuit (3)		Continuous		
Temperature	Operating	–40	150	°C
	Junction		150	
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Input pins are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3 V beyond the supply rails must be current limited to 10 mA or less.

(3) Short-circuit to ground, one amplifier per package.

2. ESD Ratings

			VALUE	UNIT
V(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

3. Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Supply voltage	1.8		5.5	V
	Specified temperature range	–40		125	°C

4. Thermal Information: TLV2333IDR-HX

THERMAL METRIC(1)		TLV2333IDR-HX SOIC 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	124.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	73.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	64.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	18.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	63.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

5. Electrical Characteristics: V_S = 1.8 V to 5.5 V

at T_A = 25°C, R_L = 10 kΩ connected to mid-supply, and V_{CM} = V_{OUT} = mid-supply (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage(1)	V_S = 5 V		2	15	µV
dVOS/dT	VOS vs temperature	T_A = –40°C to +125°C		0.02		µV/°C
PSRR	VOS vs power supply	V_S = 1.8 V to 5.5 V		1	8	µV/V
	Long-term stability (2)			1(2)		µV
	Channel separation, dc			0.1		µV/V
INPUT BIAS CURRENT						
I_B	Input bias current			±70		pA
	Input bias current over temperature	T_A = –40°C to +125°C		±150		pA
I_{OS}	Input offset current			±140		pA
NOISE						
e_n	Input voltage noise density	f = 1 kHz		55		nV/√Hz
	Input voltage noise	f = 0.01 Hz to 1 Hz		0.3		µVPP
		f = 0.1 Hz to 10 Hz		1.1		
i_n	nput current noise	f = 10 Hz		100		fA/√Hz
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range		(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	(V–) – 0.1 V < V_{CM} < (V+) + 0.1 V	102		115	dB
INPUT CAPACITANCE						
	Differential			2		pF
	Common-mode			4		
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	(V–) + 0.1 V< V_O < (V+) – 0.1 V	102		130	dB
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product	C_L = 100 pF		350		kHz
SR	Slew rate	G = 1		0.16		V/µs
OUTPUT						
	Voltage output swing from rail	T_A = –40°C to +125°C		30	70	mV
I_{SC}	Short-circuit current			±5		mA
C_L	Capacitive load drive		See *Typical Characteristics*			
Z_O	Open-loop output impedance	f = 350 kHz, I_O = 0 mA		2		kΩ
POWER SUPPLY						
V_S	Specified voltage range		1.8		5.5	V
I_Q	Quiescent current per amplifier	I_O = 0 mA, T_A = –40°C to +125°C		17	28	µA
	Turn-on time	V_S = 5 V		100		µs
TEMPERATURE RANGE						
	Specified range		–40		125	°C
	Operating range		–40		150	°C
	Storage range		–65		150	°C

(1) Specified by design and characterization. Amplifiers are 100% production screened at 25°C to reduce defective units.

(2) 300-hour life test at 150°C demonstrated randomly distributed variation of approximately 1 µV.

6. ypical Characteristics

at T_A = 25°C, C_L = 0 pF, R_L = 10 ka connected to mid-supply, V_{CM} = V_{OUT} = mid-supply (unless otherwise noted)

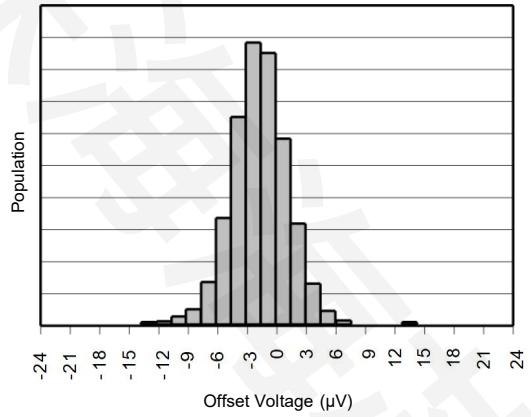


Figure 1. Offset Voltage Production Distribution

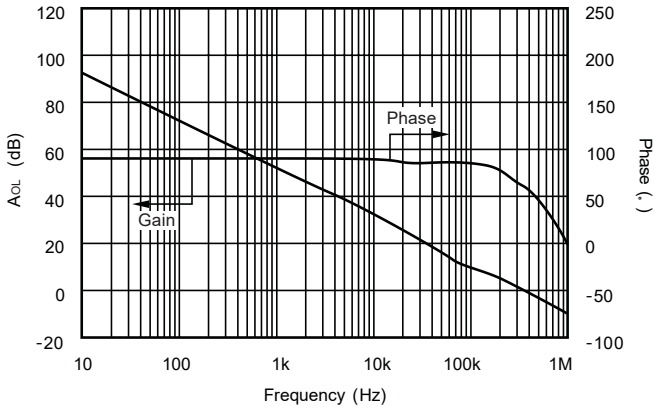


Figure 2. Open-Loop Gain vs Frequency

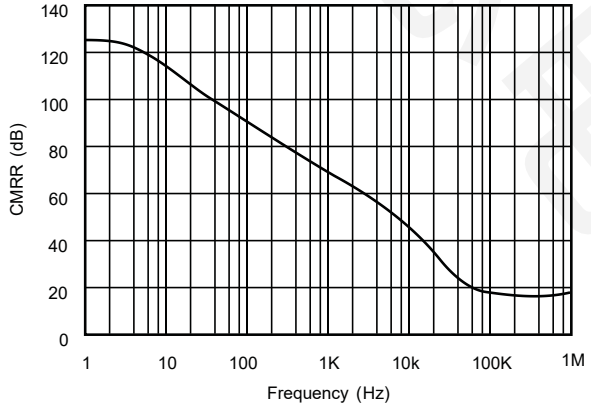


Figure 3. Common-Mode Rejection Ratio vs Frequency

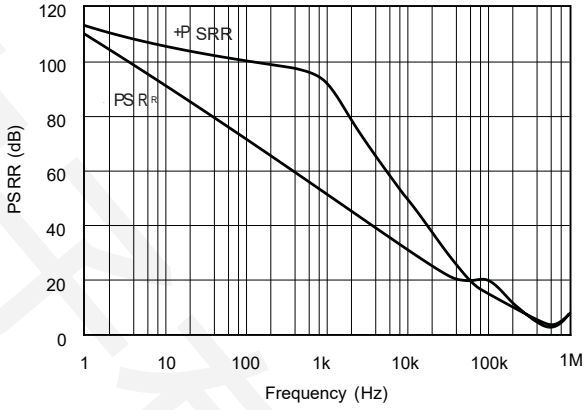


Figure 4. Power-Supply Rejection Ratio vs Frequency

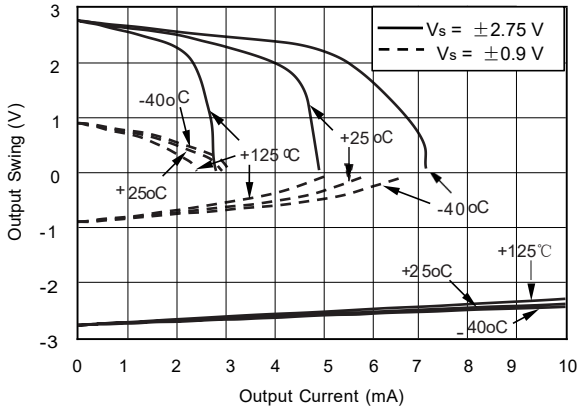


Figure 5. Output Voltage Swing vs Output Current

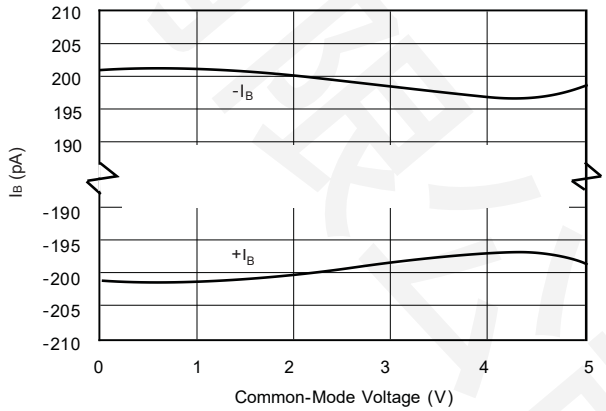


Figure 6. Input Bias Current vs Common-Mode Voltage

Typical Characteristics (continued)

at T_A = 25°C, C_L = 0 pF, R_L = 10 kΩ connected to mid-supply, V_{CM} = V_{OUT} = mid-supply (unless otherwise noted)

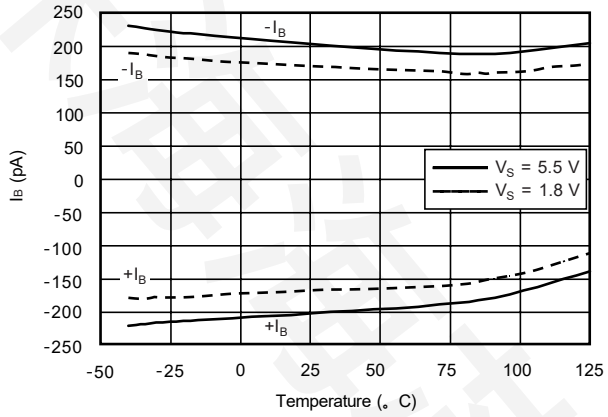


Figure 7. Input Bias Current vs Temperature

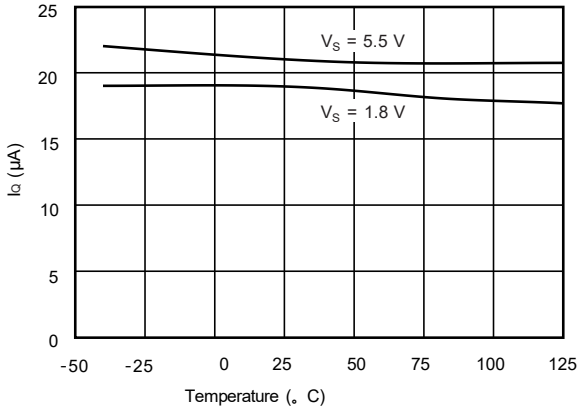


Figure 8. Quiescent Current vs Temperature

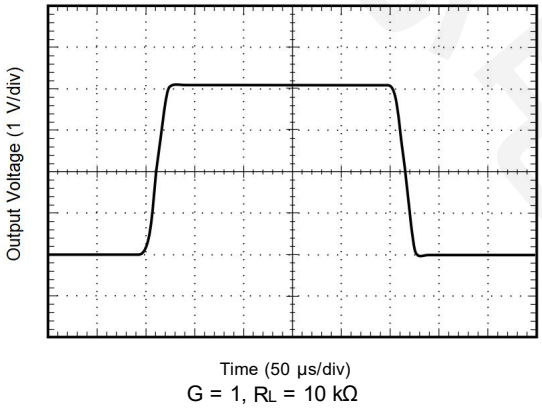


Figure 9. Large-Signal Step Response

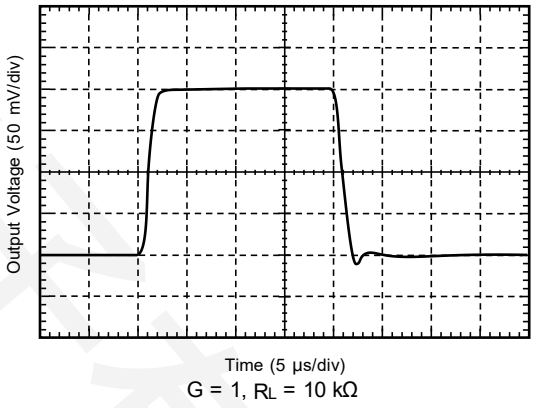


Figure 10. Small-Signal Step Response

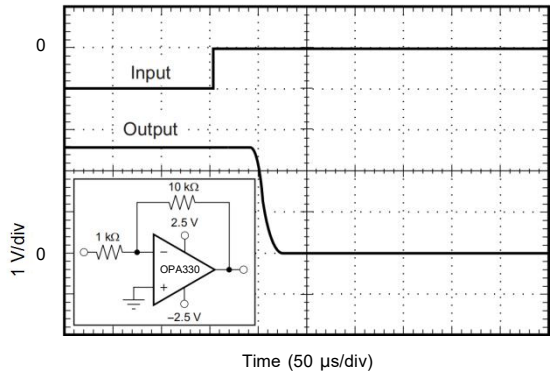


Figure 11. Positive Overvoltage Recovery

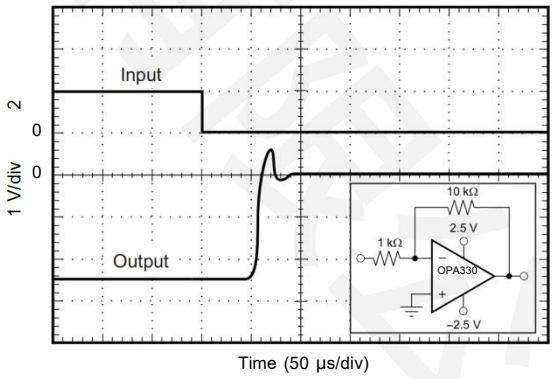


Figure 12. Negative Overvoltage Recovery

Typical Characteristics (continued)

at T_A = 25°C, C_L = 0 pF, R_L = 10 ka connected to mid-supply, V_{CM} = V_{OUT} = mid-supply (unless otherwise noted)

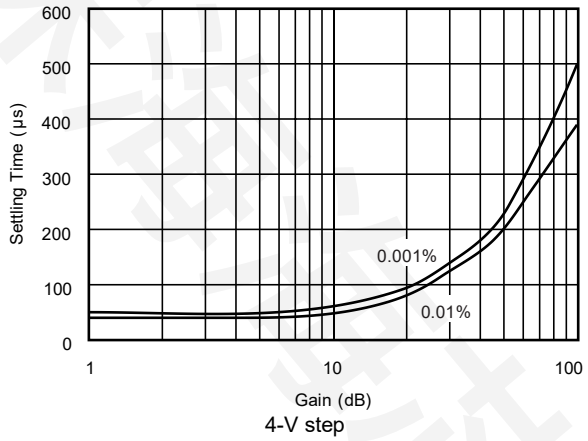


Figure 13. Settling Time vs Closed-Loop Gain

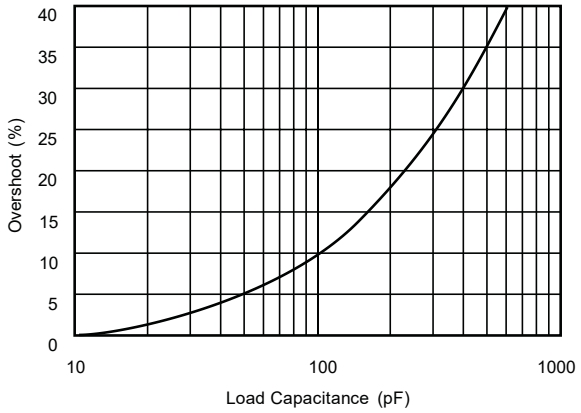


Figure 14. Small-Signal Overshoot vs Load Capacitance

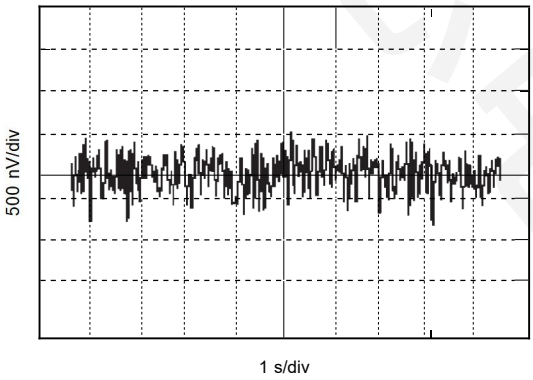


Figure 15. 0.1-Hz to 10-Hz Noise

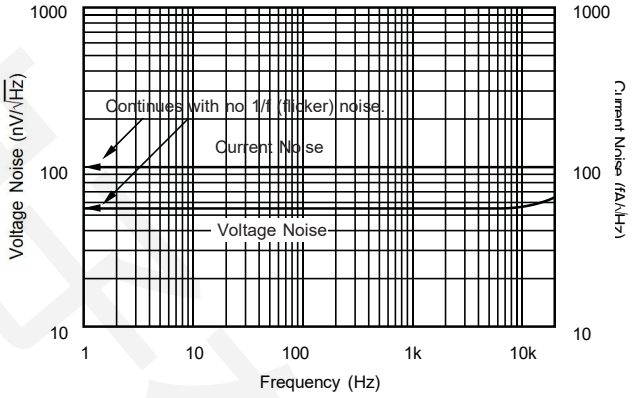


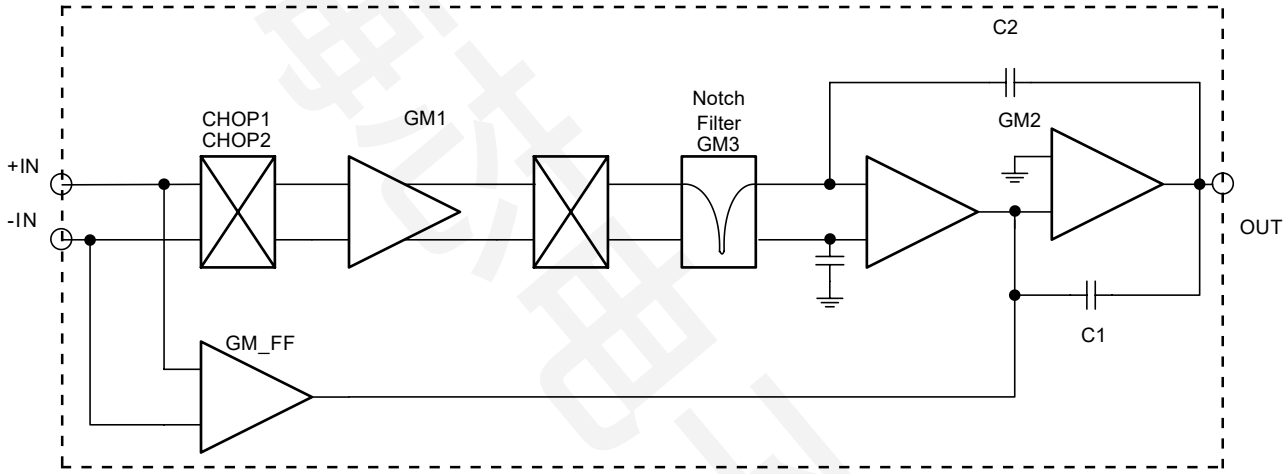
Figure 16. Current and Voltage Noise Spectral Density vs Frequency

Detailed Description

1. Overview

The TLV2333IDR-HX of low-cost operational amplifiers are unity-gain stable and free from unexpected output phase reversal. These devices use a proprietary auto-calibration technique to provide low offset voltage and very low drift over time and temperature. The TLV2333IDR-HX also offers rail-to-rail input and output and near-flat 1/f noise. These features make this series of op amps ideal for many applications and much easier to design into a wide variety of systems.

2. Functional Block Diagram



3. Feature Description

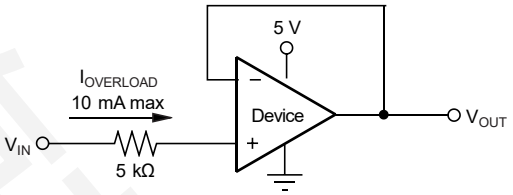
The TLV2333IDR-HX are unity-gain stable, precision operational amplifiers free from unexpected output phase reversal. The use of proprietary zero-drift circuitry gives the benefit of low input offset voltage over time and temperature, as well as lowering the 1/f noise component. As a result of the high PSRR,these devices work well in applications that run directly from battery power without regulation.

Feature Description (continued)

3.2 Input Voltage

The TLV2333IDR-HX input common-mode voltage range extends 0.1 V beyond the supply rails.

Typically, input bias current is approximately 200 pA; however, input voltages that exceed the power supplies can cause excessive current to flow into or out of the input pins. Momentary voltages greater than the power supply can be tolerated if the input current is limited to 10 mA. This limitation is easily accomplished with an input resistor, as shown in Figure 17.



NOTE: A current-limiting resistor required if the input voltage exceeds the supply rails by ≥ 0.3 V.

Figure 17. Input Current Protection

3.3 Internal Offset Correction

The TLV2333IDR-HX op amps use an auto-calibration technique with a time-continuous, 125- kHz op amp in the signal path. This amplifier is zero-corrected every 8 µs using a proprietary technique. Upon power-up, the amplifier requires approximately 100 µs to achieve specified V_{OS} accuracy. This design has no aliasing or flicker noise.

3.4 Achieving Output Swing to the Op Amp Negative Rail

Some applications require output voltage swings from 0 V to a positive full-scale voltage (such as 2.5 V) with excellent accuracy. With most single-supply op amps, problems arise when the output signal approaches 0 V, near the lower output swing limit of a single-supply op amp. A good single-supply op amp can swing close to single-supply ground, but does not reach ground. The output of the TLV2333IDR-HX can be made to swing to ground, or slightly below, on a single-supply power source. This swing to ground requires the use of another resistor and an additional, more negative, power supply than the op amp negative supply. Connect a pull-down resistor between the output and the additional negative supply to pull the output down below the value that the output can otherwise achieve, as shown in Figure 18.

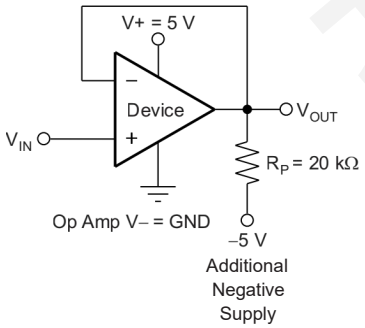


Figure 18. For V_{OUT} Range to Ground

Feature Description (continued)

The TLV2333IDR-HX have an output stage that allows the output voltage to be pulled to its negative supply rail, or slightly below, using the technique previously described. This technique only works with some types of output stages. The TLV2333IDR-HX are characterized to perform with this technique; the recommended resistor value is approximately 20 kΩ. Note that this configuration increases the current consumption by several hundreds of microamps. Accuracy is excellent down to 0 V and as low as –2 mV. Limiting and nonlinearity occur below –2 mV, but excellent accuracy returns when the output is again driven above –2 mV. Lowering the resistance of the pull-down resistor allows the op amp to swing even further below the negative rail. Resistances as low as 10 kΩ can be used to achieve excellent accuracy down to –10 mV.

8.3.5 Input Differential Voltage

The most common cause of an overdriven condition occurs when the op amp is outside of the linear range of operation. When the output of the op amp is driven to one of the supply rails, the feedback loop requirements cannot be satisfied and a differential input voltage develops across the input pins. This differential input voltage results in activation of parasitic diodes inside the front-end input chopping switches that combine with 10-kΩ electromagnetic interference (EMI) filter resistors to create the equivalent circuit shown in Figure 19. Notice that the input bias current remains within specification within the linear region.

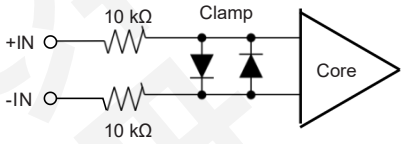


Figure 19. Equivalent Input Circuit

8.3.6 EMI Susceptibility and Input Filtering

Operational amplifiers vary in their susceptibility to EMI. If conducted EMI enters the operational amplifier, the dc offset observed at the amplifier output may shift from its nominal value when EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. Although all operational amplifier pin functions can be affected by EMI, the input pins are likely to be the most susceptible.

Layout

1. Layout Guidelines

1.1. General Layout Guidelines

Attention to good layout practice is always recommended. Keep traces short and, when possible, use a printed circuit board (PCB) ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1-μF capacitor closely across the supply pins. Apply these guidelines throughout the analog circuit to improve performance and to provide benefits such as reducing the electromagnetic interference(EMI) susceptibility.

For lowest offset voltage and precision performance, circuit layout and mechanical conditions must be optimized. Avoid temperature gradients that create thermoelectric (Seebeck) effects in the thermocouple junctions formed from connecting dissimilar conductors. These thermally-generated potentials can be made to cancel by assuring they are equal on both input terminals. Other layout and design considerations include:

- Use low thermoelectric-coefficient conditions (avoid dissimilar metals).
- Thermally isolate components from power supplies or other heat sources.
- Shield op amp and input circuitry from air currents, such as cooling fans.

Following these guidelines reduces the likelihood of junctions being at different temperatures, which can cause thermoelectric voltages of 0.1 μV/°C or higher, depending on materials used.

System Examples

Figure 20 shows the basic configuration for a bridge amplifier.

A low-side current shunt monitor is shown in Figure 21.

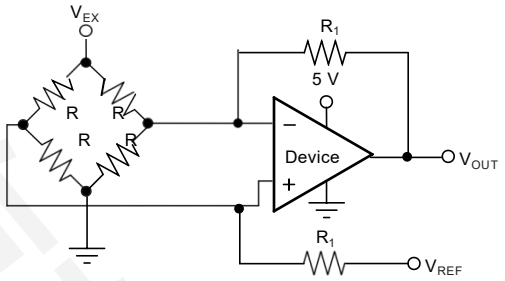
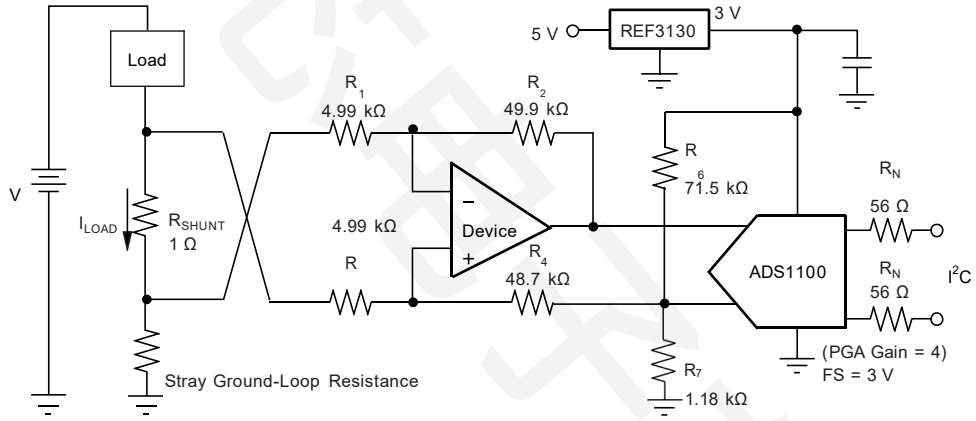


Figure 20. Single Op Amp Bridge Amplifier



NOTE: 1% resistors provide adequate common-mode rejection at small ground-loop errors.

Figure 21. Low-Side Current Monitor

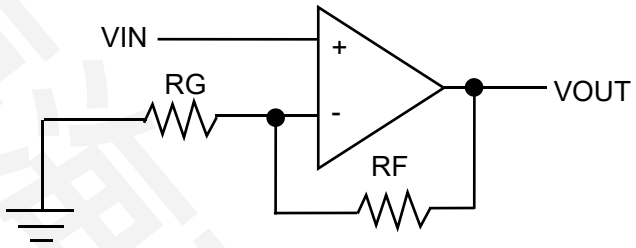
R_N are operational resistors used to isolate the ADS1100 from the noise of the digital I^2C bus. Because the ADS1100 is a 16-bit converter, a precise reference is essential for maximum accuracy.If absolute accuracy is not required, and the 5-V power supply is sufficiently stable, the REF3130 can be omitted.

CAUTION

Supply voltages larger than 7 V can permanently damage the device (see the *Absolute Maximum Ratings* table).

Place 0.1-μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement.

Layout Example



(Schematic Representation)

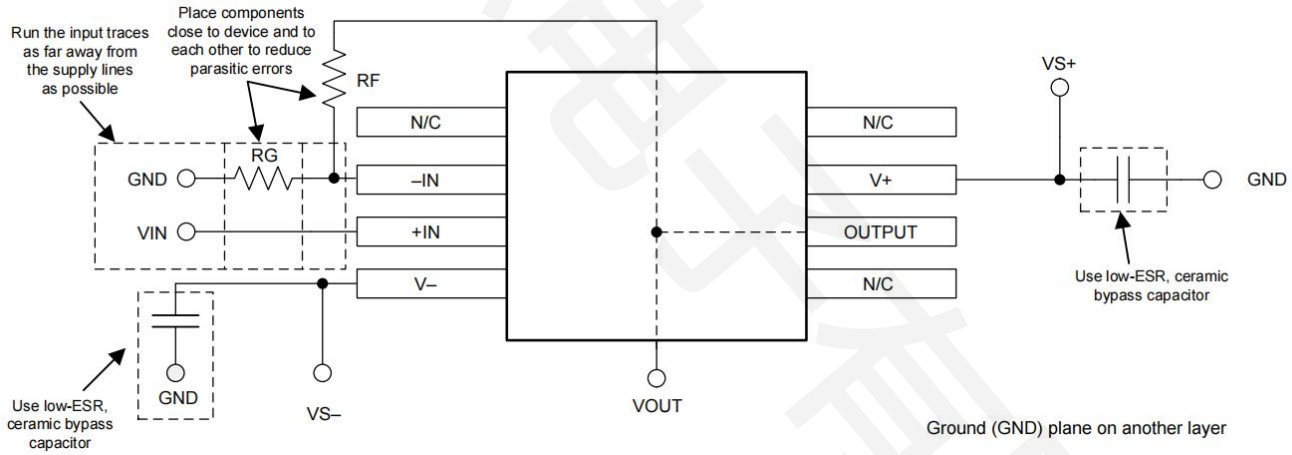


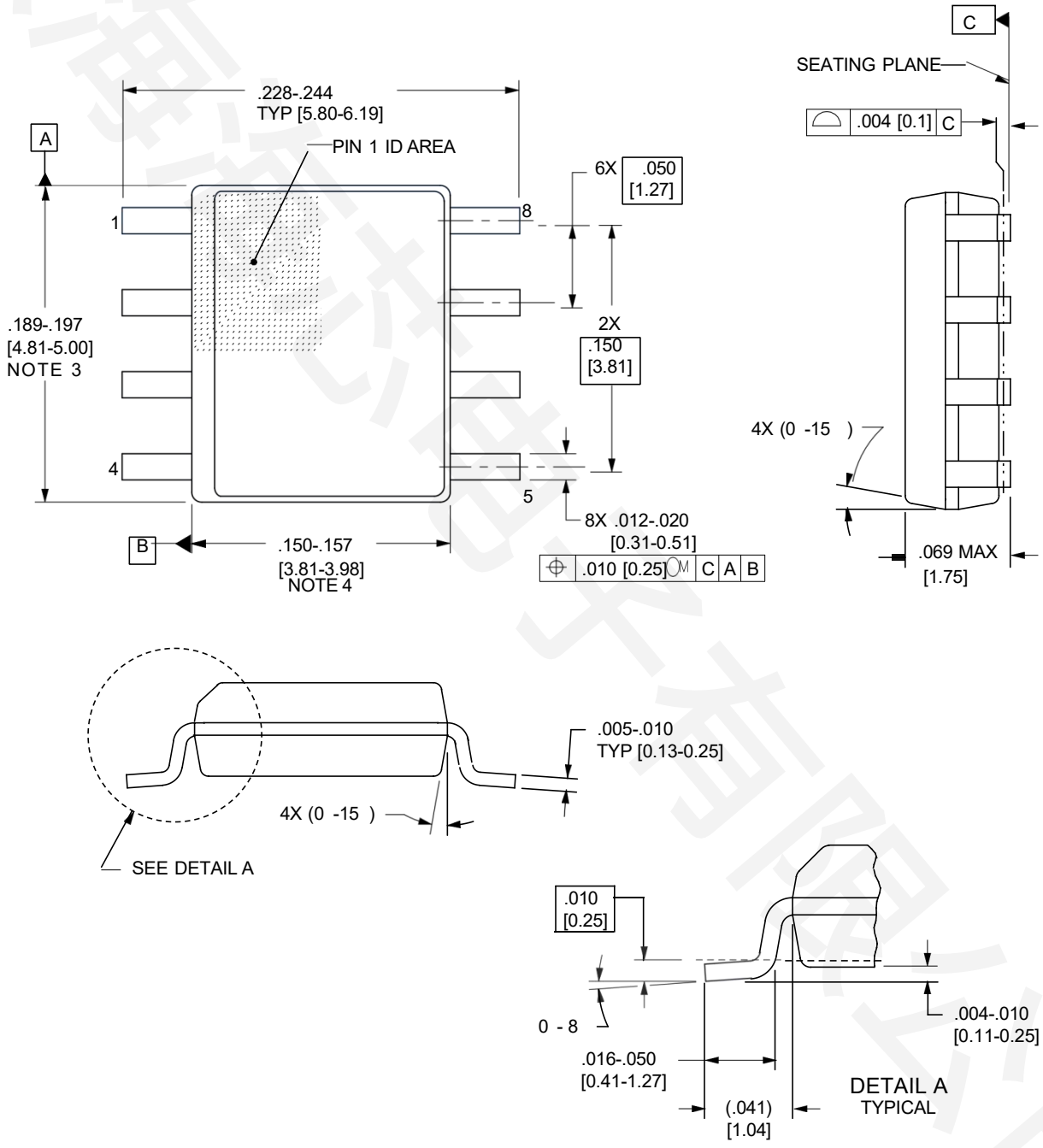
Figure 22. Layout Example

Electrostatic Discharge Caution

These devices have limited built-in ESD protection.The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

PACKAGE OUTLINE

SOIC-8



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.