

1. Description

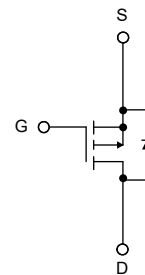
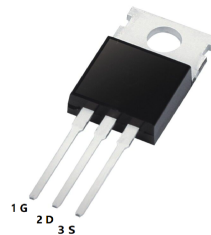
This P-Channel enhancement mode power MOSFET is produced using planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength.

2. Features

- $V_{DS(V)} = -60V$
- $I_D = -47A$
- $R_{DS(ON)} = 26m\Omega (V_{GS} = -10V)$
- Low Gate Charge (Typ. 84 nC)
- Low C_{rss} (Typ. 320 pF)
- 100% Avalanche Tested
- 175°C Maximum Junction Temperature Rating

3. Pinning information

Pin	Symbol	Description
1	G	GATE
2	D	SOURCE
3	S	DRAIN



4. Absolute Maximum Ratings $T_c = 25^\circ C$

Parameter		Symbol	Rating	Units
Drain Source Voltage		V_{DSS}	-60	V
Drain Current - Continuous	$T_c = 25^\circ C$	I_D	-47	A
- Continuous	$T_c = 100^\circ C$		-33.2	A
- Pulsed	(Note 1)	I_{DM}	-188	A
Gate-Source Voltage		V_{GSS}	± 25	V
Single Pulsed Avalanche Energy	(Note 2)	E_{AS}	820	mJ
Avalanche Current	(Note 1)	I_{AR}	-47	A
Repetitive Avalanche Energy	(Note 1)	E_{AR}	16	mJ
Peak Diode Recovery dv/dt	(Note 3)	dv/dt	-7	V/ns



Power Dissipation ($T_C=25^{\circ}\text{C}$)	P_D	160	W
- Derate above 25°C		1.06	W/ $^{\circ}\text{C}$
Temperature Range	T_J, T_{STG}	-55 to 175	$^{\circ}\text{C}$
Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	T_L	300	$^{\circ}\text{C}$

5. Thermal Characteristics

Parameter	Symbol	Rating	Units
Thermal Resistance, Junction-to-Case, Max.	$R_{\theta JC}$	0.94	$^{\circ}\text{C/W}$
Thermal Resistance, Case-to-Sink, Typ.	$R_{\theta CS}$	0.5	$^{\circ}\text{C/W}$
Thermal Resistance, Junction-to-Ambient, Max.	$R_{\theta JA}$	62.5	$^{\circ}\text{C/W}$



6. Electrical Characteristic ($T_c=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain to Source Breakdown Voltage	BV_{DSS}	$I_D=-250\mu\text{A}$, $V_{GS}=0\text{V}$	-60			V
Breakdown Voltage Temperature Coefficient	$\frac{\Delta BV_{DSS}}{\Delta T_J}$	$I_D=-250\mu\text{A}$ Referenced to 25°C		-0.06		V/ $^\circ\text{C}$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-60\text{V}$, $V_{GS}=0\text{V}$			-1	μA
		$V_{DS}=-48\text{V}$, $T_c=150^\circ\text{C}$			-10	μA
Gate-Body Leakage Current, Forward	I_{GSSF}	$V_{GS}=-25\text{V}$, $V_{DS}=0\text{V}$			-100	nA
Gate-Body Leakage Current, Reverse	I_{GSSR}	$V_{GS}=25\text{V}$, $V_{DS}=0\text{V}$			100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$, $I_D=-250\mu\text{A}$	-1.1	-1.8	-2.5	V
Static Drain to Source On Resistance	$R_{DS(ON)}$	$V_{GS}=-10\text{V}$, $I_D=-23.5\text{A}$		21	26	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=-30\text{V}$, $I_D=-23.5\text{A}$ (Note 4)		21		S
Input Capacitance	C_{iss}	$V_{DS}=-25\text{V}$, $V_{GS}=0\text{V}$, $f=1\text{MHz}$		2800	3600	pF
Output Capacitance	C_{oss}			1300	1700	pF
Reverse Transfer Capacitance	C_{rss}			320	420	pF
Turn-On Delay Time	$t_{D(on)}$	$V_{DD}=-30\text{V}$, $I_D=-23.5\text{A}$ $R_G=25\Omega$ (Note 4,5)		50	110	ns
Rise Time	t_r			450	910	ns
Turn-Off Delay Time	$t_{D(off)}$			100	210	ns
Fall Time	t_f			195	400	ns
Total Gate Charge	Q_g	$V_{DS}=-48\text{V}$, $I_D=-47\text{A}$ $V_{GS}=-10\text{V}$ (Note 4,5)		84	110	nC
Gate-Source Charge	Q_{gs}			18		nC
Gate-Drain Charge	Q_{gd}			44		nC
Maximum Continuous Drain to Source Diode Forward Current	I_S				-47	A
Maximum Pulsed Drain to Source Diode Forward Current	I_{SM}				-188	A



Drain-Source Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_S=-47A$			-4	V
Reverse Recovery Time	t_{rr}	$V_{GS}=0V, I_S=-47A$		130		ns
Reverse Recovery Charge	Q_{rr}	$dI_F/dt=100A/\mu s$ (Note 4)		0.55		μC

Notes:

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted.
Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$.

5. Essentially independent of operating temperature.



7.1 Typical characteristic

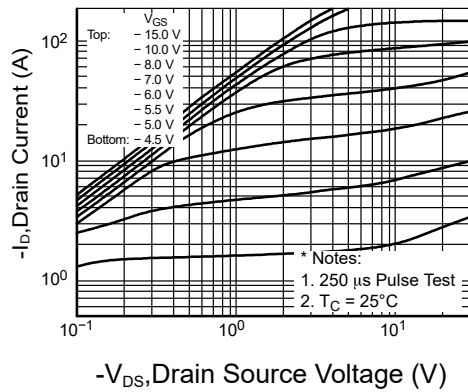


Figure 1: Output Characteristics

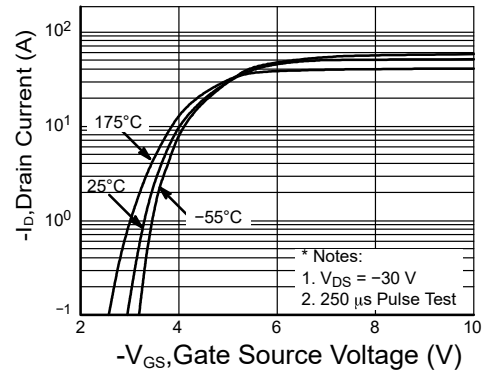


Figure 2: Transfer Characteristics

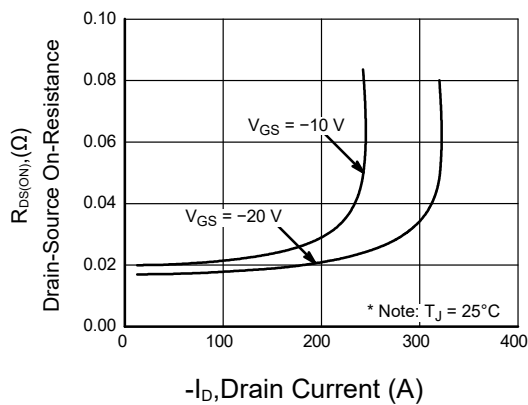


Figure 3: On-Resistance Variation vs. Drain Current and Gate Voltage

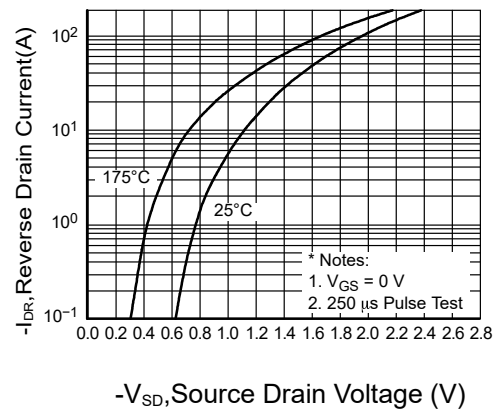


Figure 4: Body Diode Forward Voltage Variation vs. Source Current and Temperature

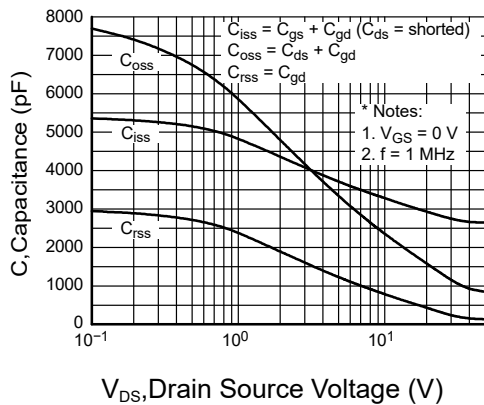


Figure 5: Capacitance Characteristics

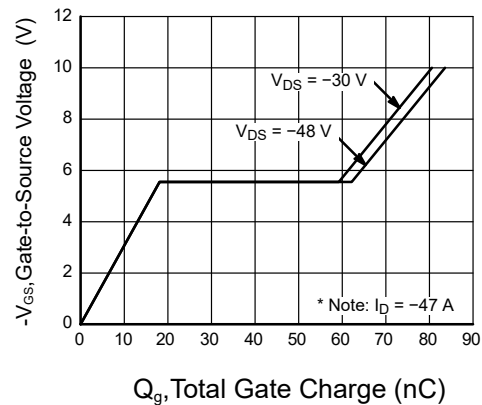


Figure 6: Gate Charge Characteristics



7.2 Typical characteristic

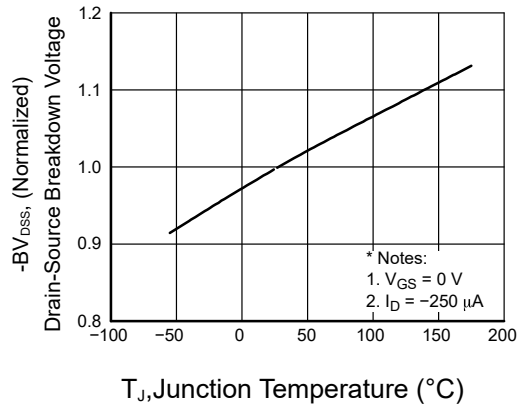


Figure 7: Breakdown Voltage Variation vs. Temperature

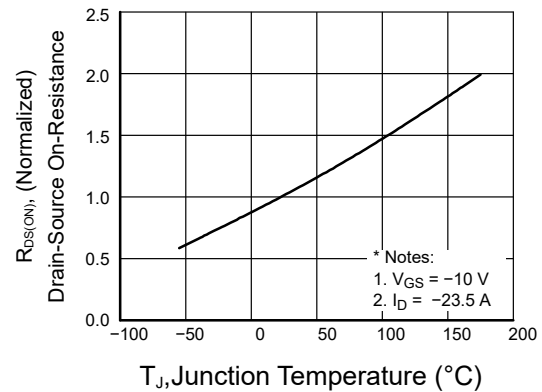


Figure 8: On-Resistance Variation vs. Temperature

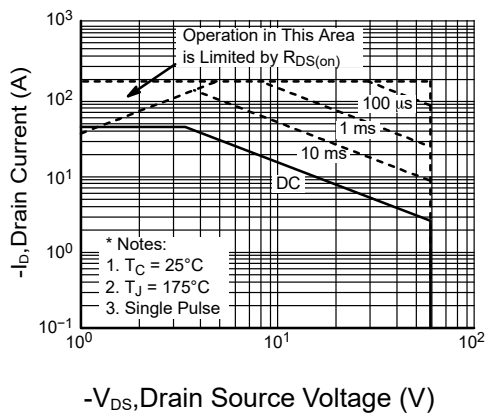


Figure 9: Maximum Drain Current vs. Ambient Temperature

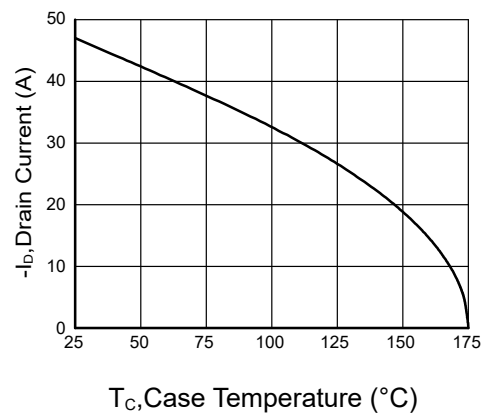


Figure 10: Maximum Drain Current vs. Case Temperature

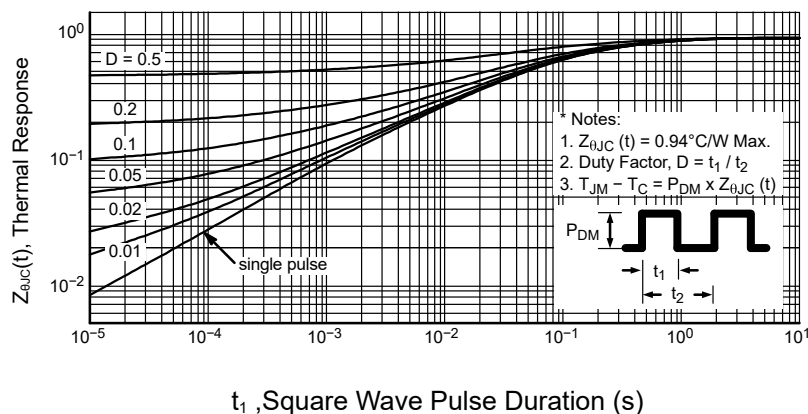


Figure 11: Transient Thermal Response Curve



7.3 Typical characteristic

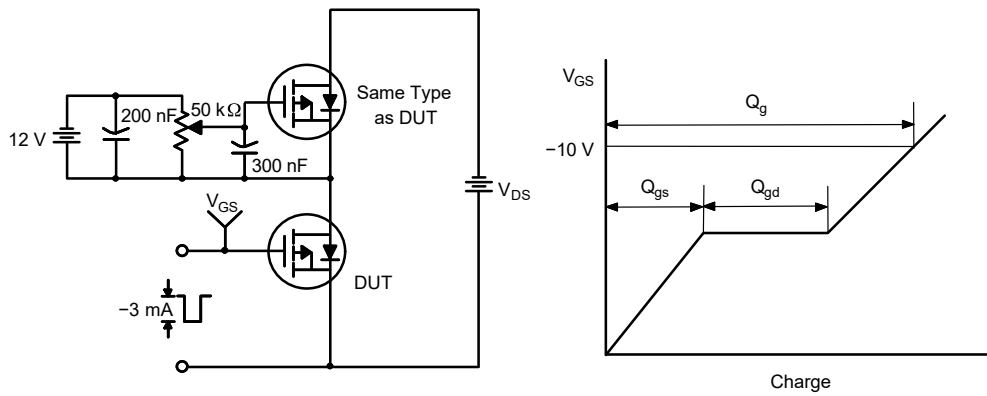


Figure 12: Gate Charge Test Circuit & Waveform

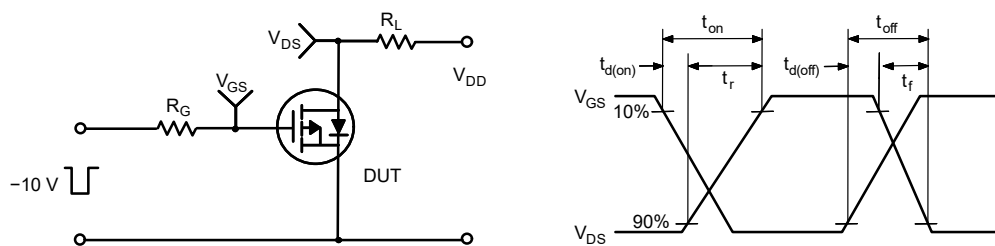


Figure 13: Resistive Switching Test Circuit & Waveforms

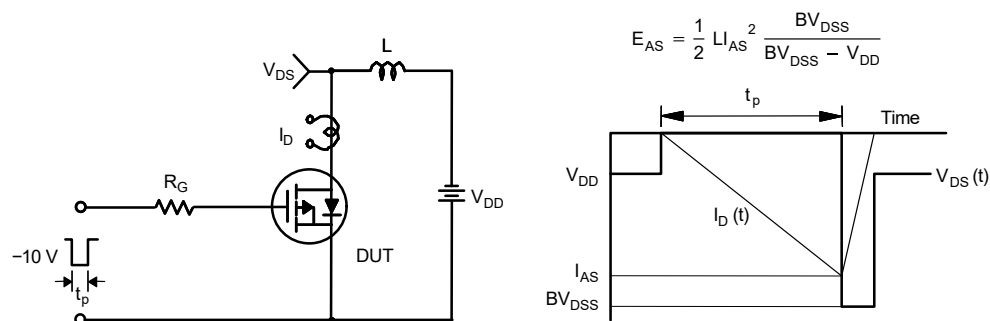


Figure 14: Unclamped Inductive Switching Test Circuit & Waveforms



7.4 Typical characteristic

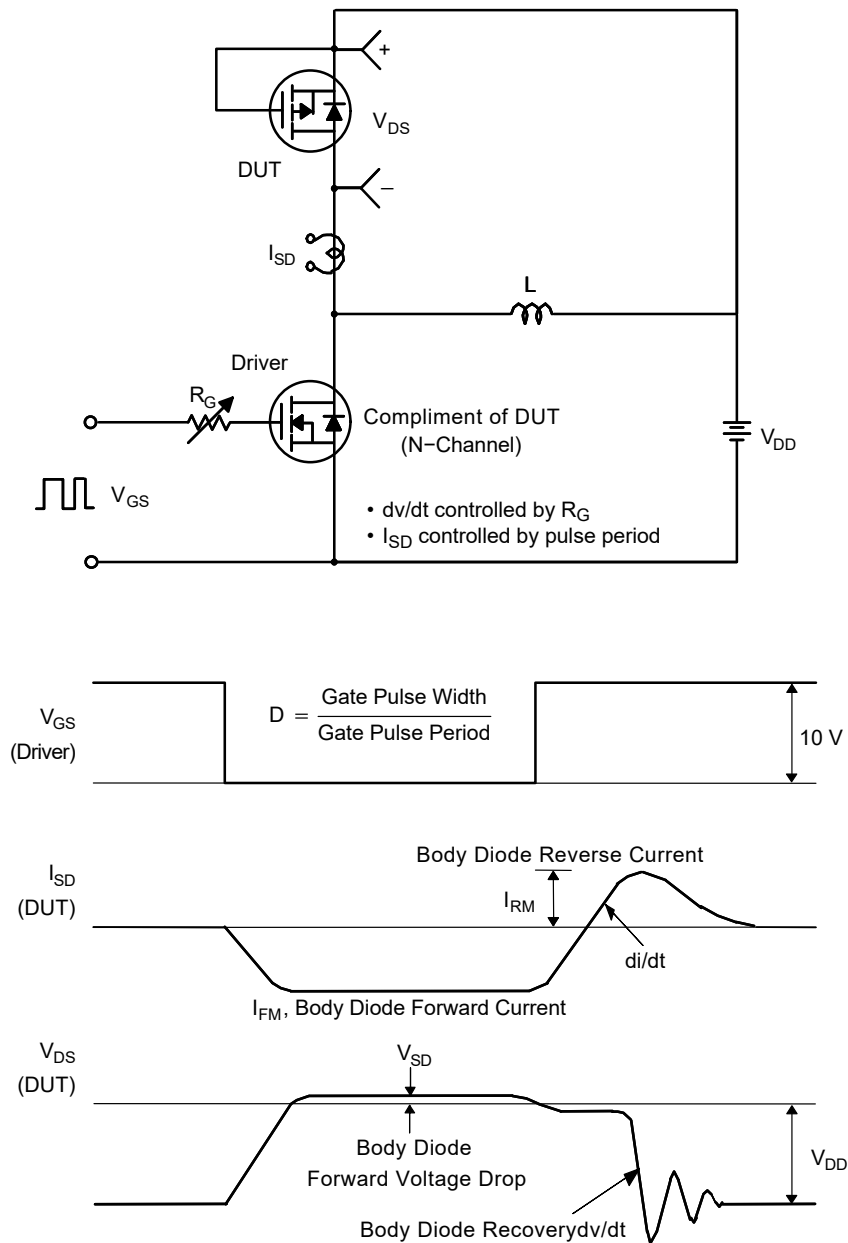
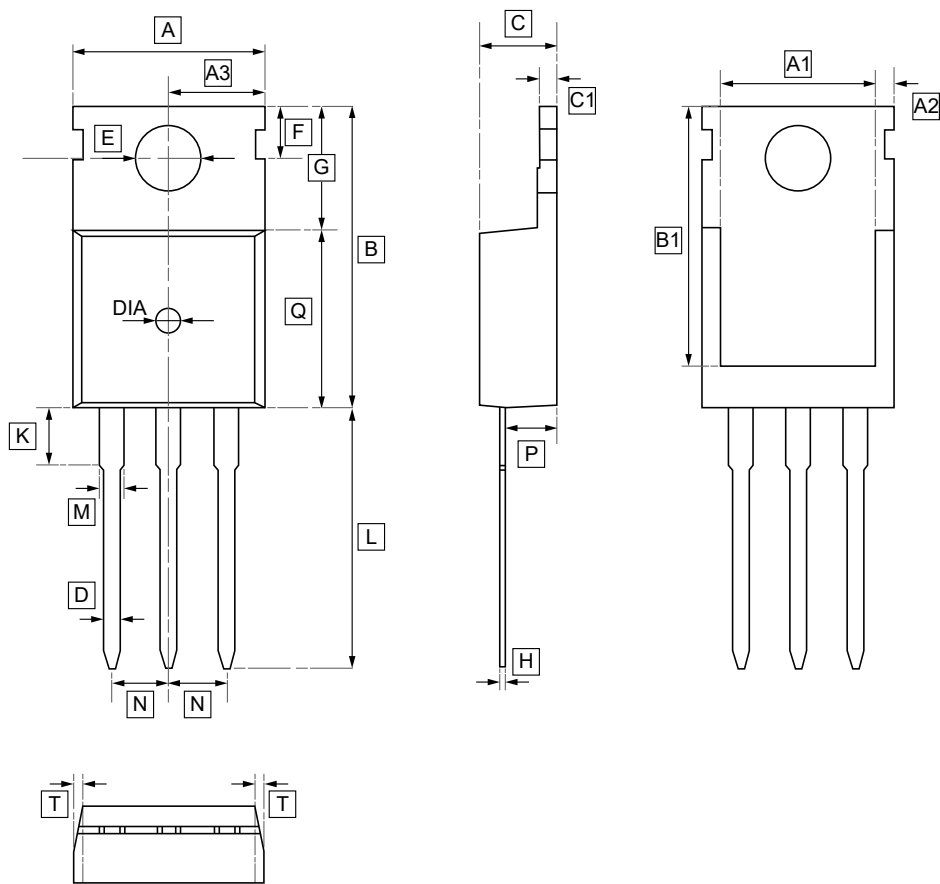


Figure 15: Peak Diode Recovery dv/dt Test Circuit & Waveforms



8.1 TO-220 Package Outline Dimensions



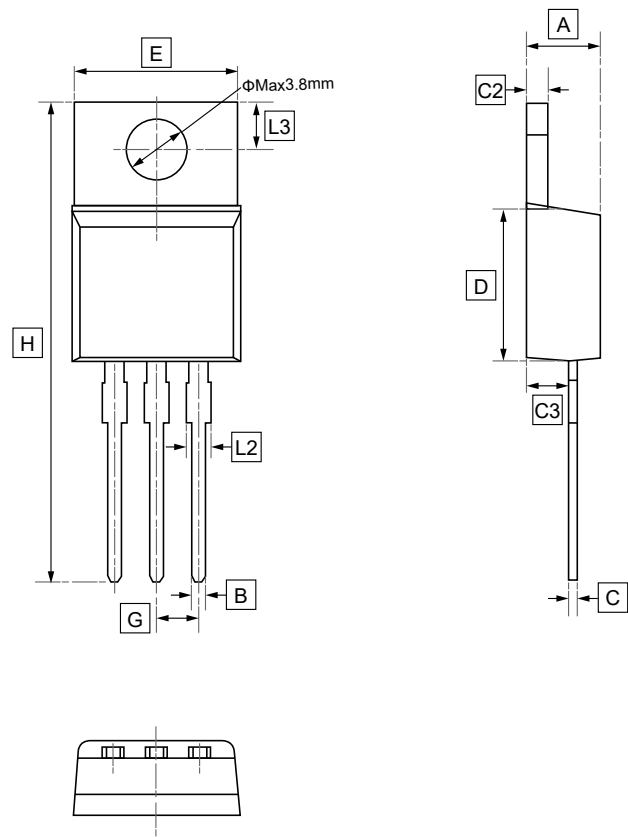
DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	A3	B	B1	C	C1	D	E	F	G
Min	9.7	8.44	1.05	4.8	15.4	12.9	4.28	1.1	0.6	3.4	2.65	5.2
Max	10.3	8.84	1.25	5.2	16.2	13.5	4.68	1.5	1.0	3.8	3.25	5.8

Symbol	H	K	L	L1	M	N	P	Q	T	DIA
Min	0.4	2.9	12.8	2.7	1.15	2.49	2.1	8.7	W:0.35	⌀1.5
Max	0.6	3.3	13.6	3.3	1.35	2.59	2.7	9.3		(deep 0.2)



8.2 TO-220 Package Outline Dimensions

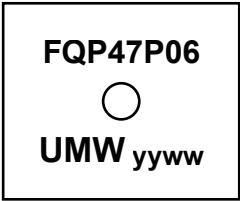


DIMENSIONS (mm are the original dimensions)

Symbol	A	B	C	C2	C3	D	E	G	H	L2	L3
Min	4.30	0.60	0.28	1.17	2.30	8.80	9.80	2.44	28.55	1.10	2.59
Max	4.70	1.00	0.48	1.37	2.70	9.20	10.20	2.64	29.15	1.50	2.89



9.Ordering Information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW FQP47P06	TO-220	1000	Tube and box



10.Disclaimer

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