

1.Features

- $V_{DS(V)}=100V$
- $I_D=192A$
- $R_{DS(ON)}<4.2m\Omega(V_{GS}=10V)$

2.2Benefits

- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness

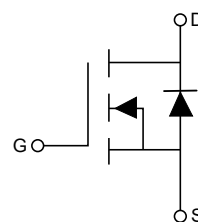
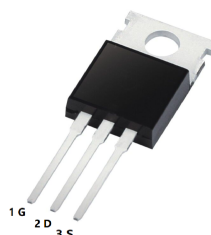
2.1Benefits

- Lead-Free, RoHS Compliant, Halogen-Free
- Enhanced body diode dV/dt and dI/dt Capability

3.Pinning information

Pin	Symbol	Description
1	G	GATE
2	D	DRAIN
3	S	SOURCE

TO-220



4.Absolute Maximum Ratings

Parameter		Symbol	Rating	Units
Continuous Drain Current, $V_{GS}=10V$	$T_C=25^{\circ}C$	I_D	192	A
Continuous Drain Current, $V_{GS}=10V$	$T_C=100^{\circ}C$		136	A
Pulsed Drain Current ①		I_{DM}	690	A
Maximum Power Dissipation	$T_C=25^{\circ}C$	P_D	441	W
Linear Derating Factor			2.9	W/ $^{\circ}C$
Gate-to-Source Voltage		V_{GS}	± 20	V
Storage Temperature Range		T_J, T_{STG}	-55 to 175	$^{\circ}C$
Soldering Temperature, for 10 seconds (1.6mm from case)			300	$^{\circ}C$
Mounting Torque, 6-32 or M3 Screw			10 lbf·in (1.1 N·m)	



Single Pulse Avalanche Energy ②	$E_{AS(Thermally\ limited)}$	567	mJ
Single Pulse Avalanche Energy ⑨	$E_{AS(Thermally\ limited)}$	1005	mJ
Single Pulse Avalanche Energy Tested Value ⑩	$E_{AS(tested)}$	240	mJ
Avalanche Current ①	I_{AR}	See Fig 14, 14,	A
Repetitive Avalanche Energy ①	E_{AR}	23a, 23b	mJ

5. Thermal resistance rating

Parameter	Symbol	Typ	Max	Units
Junction-to-Case ⑦	$R_{\theta JC}$		0.34	°C/W
Case-to-Sink, Flat Greased Surface	$R_{\theta CS}$	0.5		°C/W
Junction-to-Ambient	$R_{\theta JA}$		62	°C/W
Junction-to-Ambient (PCB Mount) ⑧	$R_{\theta JA}$		40	°C/W



6. Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	100			V
Breakdown Voltage Temp. Coefficient	$\Delta V_{(BR)DSS}/\Delta T_J$	$I_D=5\text{mA}$, Reference to 25°C ①		0.1		V/ $^\circ\text{C}$
Static Drain-to-Source On-Resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=115\text{A}$		3.5	4.2	m Ω
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	2		4	V
Drain-to-Source Leakage Current	I_{DSS}	$V_{DS}=100\text{V}$, $V_{GS}=0\text{V}$			20	μA
		$V_{DS}=80\text{V}$, $V_{GS}=0\text{V}$, $T_J=125^\circ\text{C}$			250	μA
Gate-to-Source Forward Leakage	I_{GSS}	$V_{GS}=20\text{V}$			100	nA
Gate-to-Source Reverse Leakage		$V_{GS}=-20\text{V}$			-100	nA
Gate Resistance	R_g			2.2		Ω
Forward Transconductance	g_{FS}	$V_{DS}=10\text{V}$, $I_D=115\text{A}$	278			S
Total Gate Charge	Q_g	$I_D=115\text{A}$, $V_{DS}=50\text{V}$, $V_{GS}=10\text{V}$		170	255	nC
Gate-to-Source Charge	Q_{gs}			46		nC
Gate-to-Drain Charge	Q_{gd}			45		nC
Total Gate Charge Sync. (Q_g-Q_{gd})	Q_{sync}			125		nC
Turn-On Delay Time	$t_{D(on)}$	$V_{DD}=65\text{V}$, $I_D=115\text{A}$ $R_G=2.7\Omega$, $V_{GS}=10\text{V}$ ④		17		ns
Rise Time	t_r			97		ns
Turn-Off Delay Time	$t_{D(off)}$			110		ns
Fall Time	t_f			100		ns
Input Capacitance	C_{iss}	$V_{GS}=0\text{V}$, $V_{DS}=50\text{V}$ $f=1\text{MHz}$, See Fig.TBD		9500		pF
Output Capacitance	C_{oss}			660		pF
Reverse Transfer Capacitance	C_{rss}			310		pF
Effective Output Capacitance (Energy Related)	$C_{oss\text{eff.}}(ER)$	$V_{GS}=0\text{V}$, $V_{DS}=0\text{V}$ to 80V ⑥		725		pF
Output Capacitance (Time Related)	$C_{oss\text{eff.}}(TR)$	$V_{GS}=0\text{V}$, $V_{DS}=0\text{V}$ to 80V ⑤		950		pF



Diode Characteristics						
Continuous Source Current (Body Diode)	I_S	MOSFET symbol showing the integral reverse p-n junction diode.			192	A
Pulsed Source Current (Body Diode) ①	I_{SM}				690	A
Diode Forward Voltage	V_{SD}	$T_J=25^\circ\text{C}, I_S=115\text{A}, V_{GS}=0\text{V}$ ④			1.3	V
Peak Diode Recovery dv/dt ③	dv/dt	$T_J=175^\circ\text{C}, I_S=115\text{A}, V_{GS}=100\text{V}$		18		V/ns
Reverse Recovery Time	t_{rr}	$T_J=25^\circ\text{C}, V_{DD}=85\text{V}$		47		ns
		$T_J=125^\circ\text{C}, I_F=115\text{A}$		55		ns
Reverse Recovery Charge	Q_{rr}	$T_J=25^\circ\text{C}, di/dt=100\text{A}/\mu\text{s}$ ④		90		nC
		$T_J=125^\circ\text{C}$		125		nC
Reverse Recovery Current	I_{RRM}	$T_J=25^\circ\text{C}$		3.5		A

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Limited by T_{Jmax} , starting $T_J = 25^\circ\text{C}$, $L = 86\mu\text{H}$, $R_G = 50\Omega$, $I_{AS} = 115\text{A}$, $V_{GS} = 10\text{V}$.
- ③ $I_{SD} \leq 115\text{A}$, $di/dt \leq 1400\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 175^\circ\text{C}$.
- ④ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ⑤ C_{oss} eff. (TR) is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑥ C_{oss} eff. (ER) is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑦ R_θ is measured at T_J approximately 90°C .
- ⑧ Limited by T_{Jmax} starting $T_J = 25^\circ\text{C}$, $L = 1\text{mH}$, $R_G = 50\Omega$, $I_{AS} = 45\text{A}$, $V_{GS} = 10\text{V}$.
- ⑨ This value determined from sample failure population, starting $T_J = 25^\circ\text{C}$, $L = 86\mu\text{H}$, $R_G = 50\Omega$, $I_{AS} = 115\text{A}$, $V_{GS} = 10\text{V}$.



7.1 Typical Characteristics

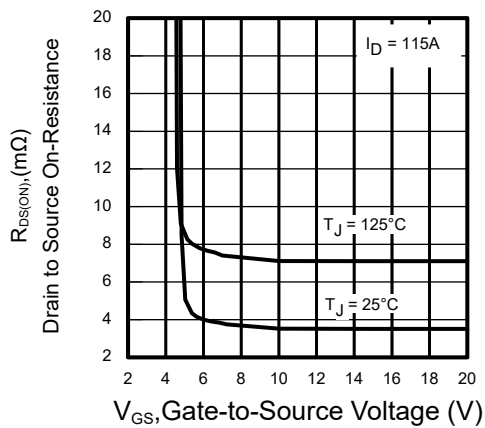


Figure 1: Typical On-Resistance vs. Gate Voltage

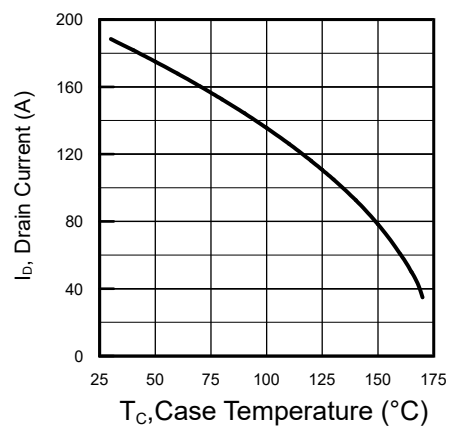


Figure 2: Maximum Drain Current vs. Case Temperature

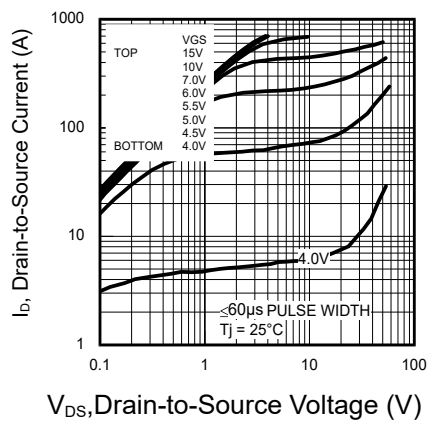


Figure 3: Typical Output Characteristics

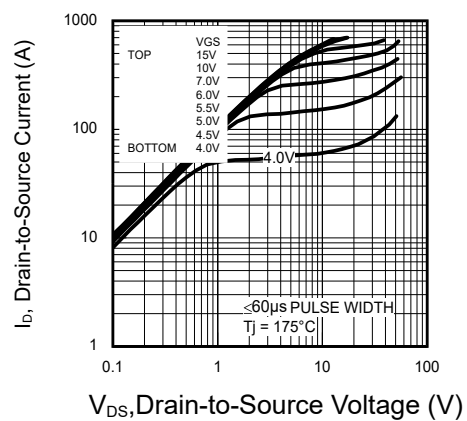


Figure 4: Typical Output Characteristics

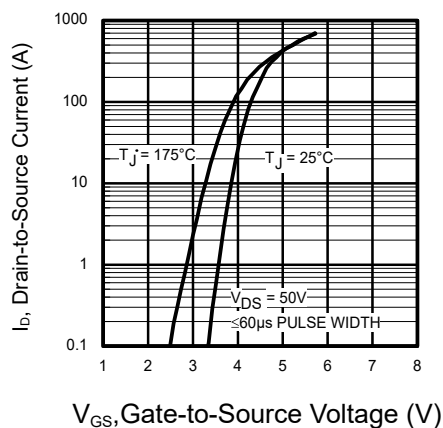


Figure 5: Typical Transfer Characteristics

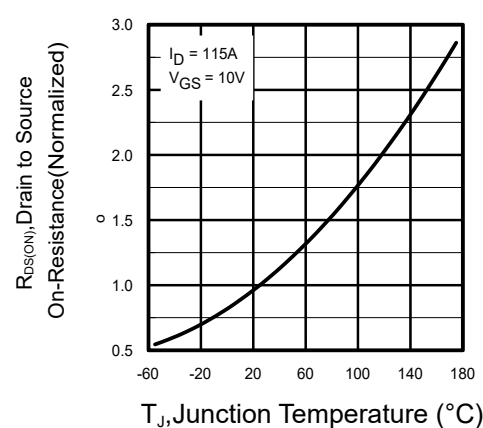
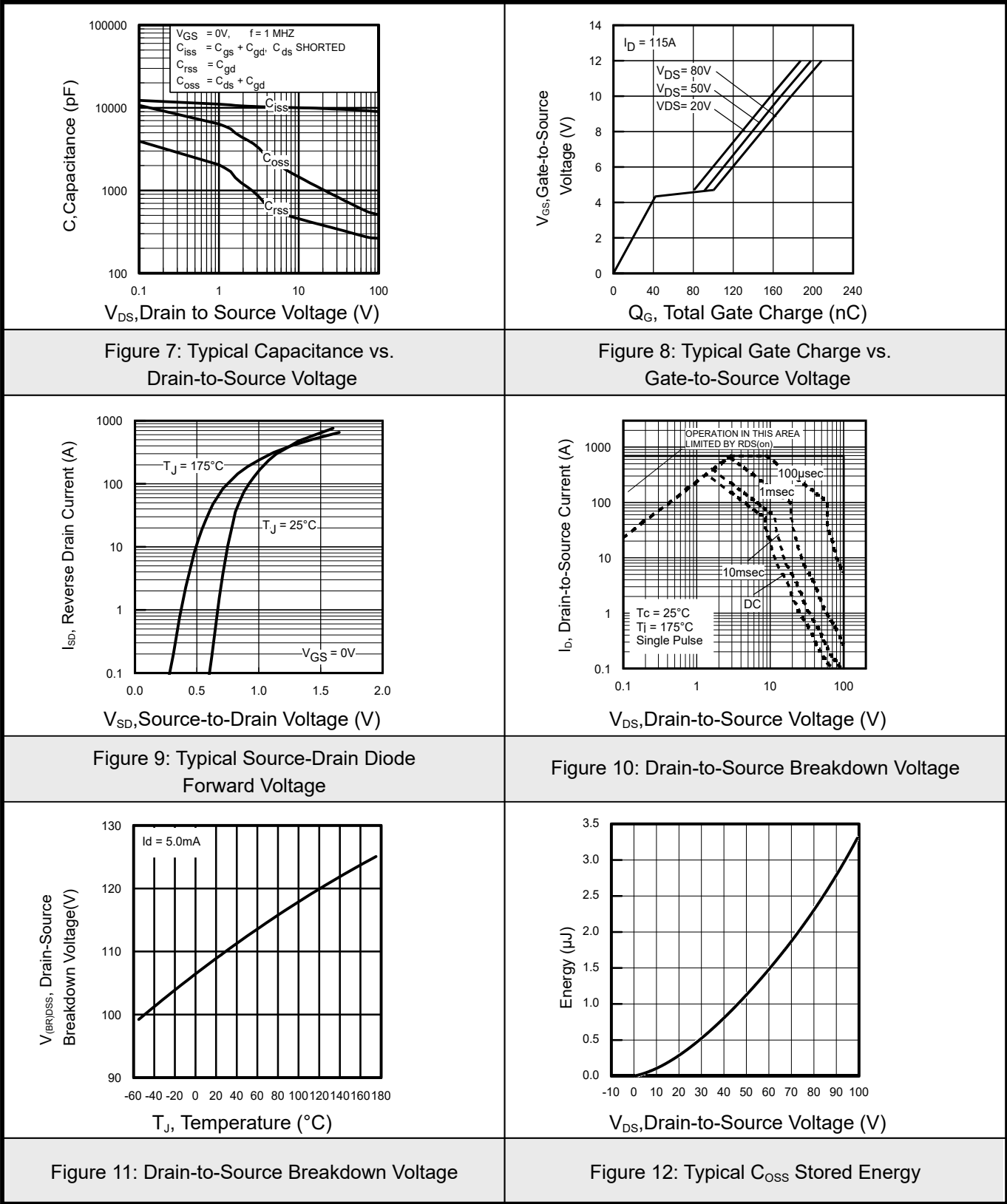


Figure 6: Normalized On-Resistance vs. Temperature



7.2 Typical Characteristics





7.3 Typical Characteristics

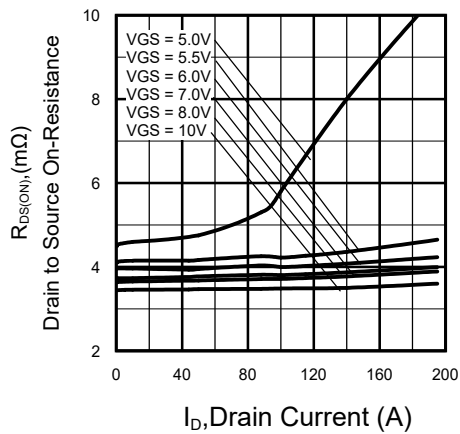


Figure 13: Typical On-Resistance vs. Drain Current

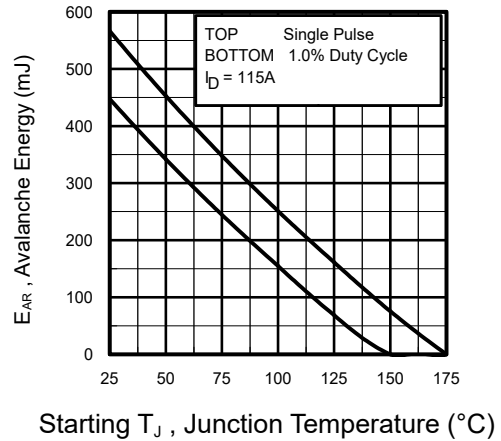


Figure 14: Maximum Avalanche Energy vs. Temperature

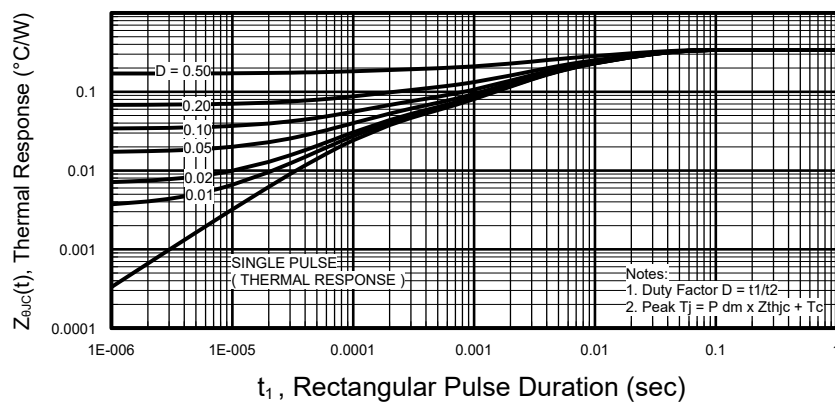


Figure 15: Maximum Effective Transient Thermal Impedance, Junction-to-Case

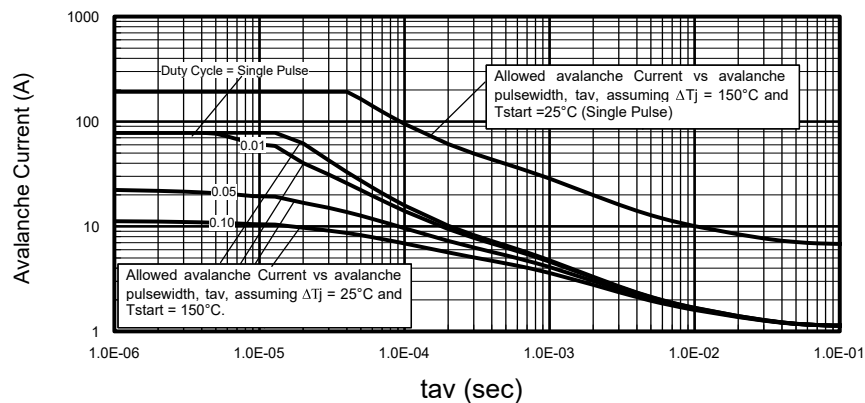


Figure 16: Typical Avalanche Current vs. Pulsewidth



Notes on Repetitive Avalanche Curves , Figures 14, 16:

1. Avalanche failures assumption: Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} .

This is validated for every part type.

2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.

3. Equation below based on circuit and waveforms shown in Figures 23a, 23b.

4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.

5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).

6. I_{av} = Allowable avalanche current.

7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax}

(assumed as 25°C in Figure 14, 15).

t_{av} = Average time in avalanche.

D = Duty cycle in avalanche = $t_{av} \cdot f$

$Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 14)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$



7.4 Typical Characteristics

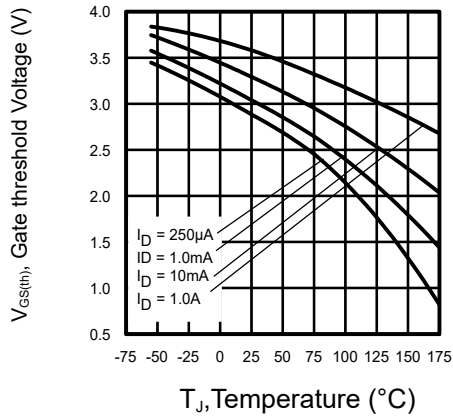


Figure 17: Threshold Voltage vs. Temperature

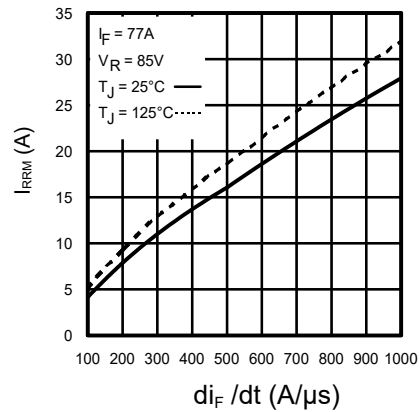


Figure 18: Typical Recovery Current vs. di/dt

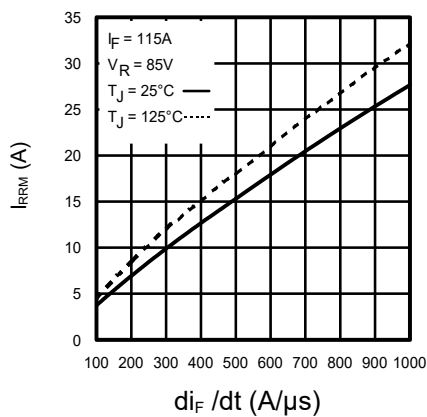


Figure 19: Typical Recovery Current vs. di/dt

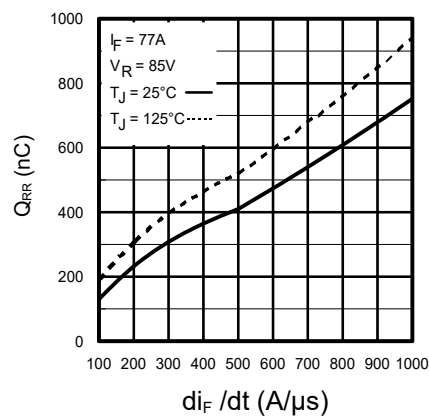


Figure 20: Typical Stored Charge vs. di/dt

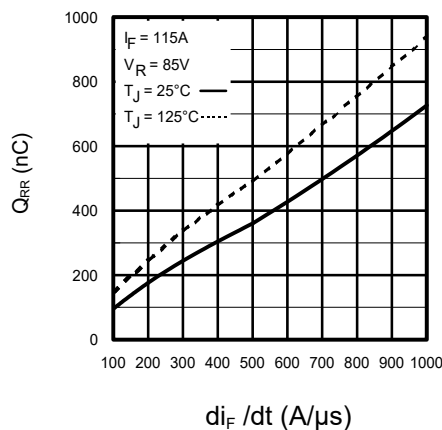
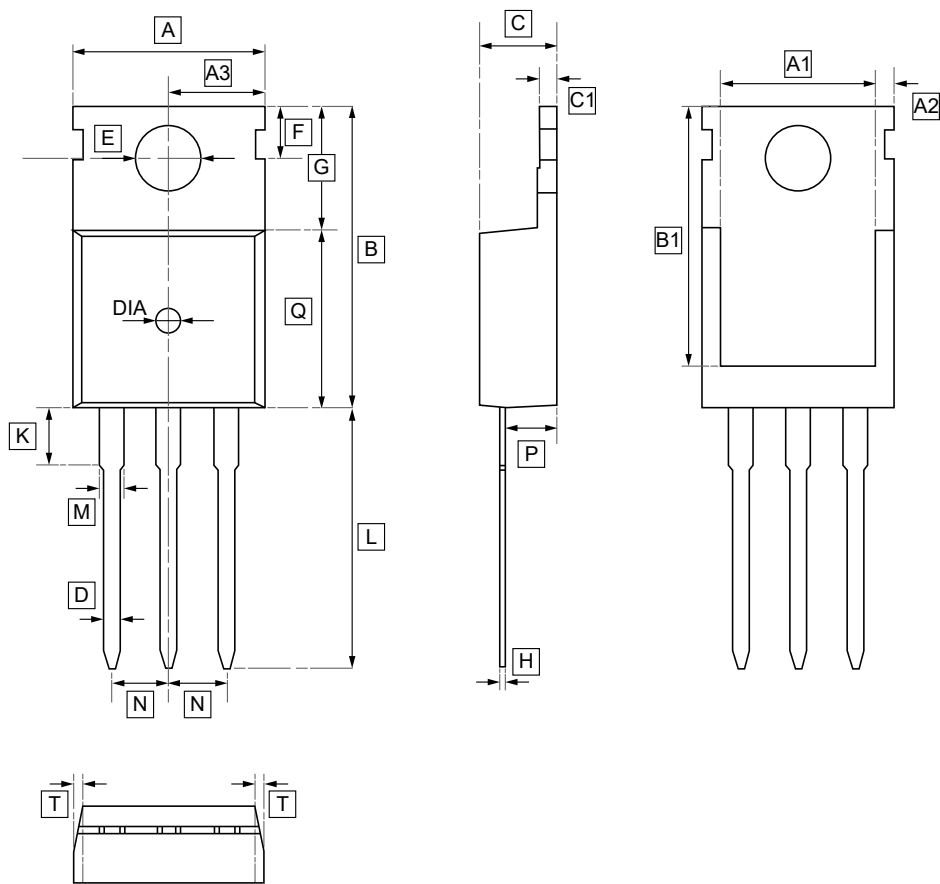


Figure 21: Typical Stored Charge vs. di/dt



8.1 TO-220 Package Outline Dimensions



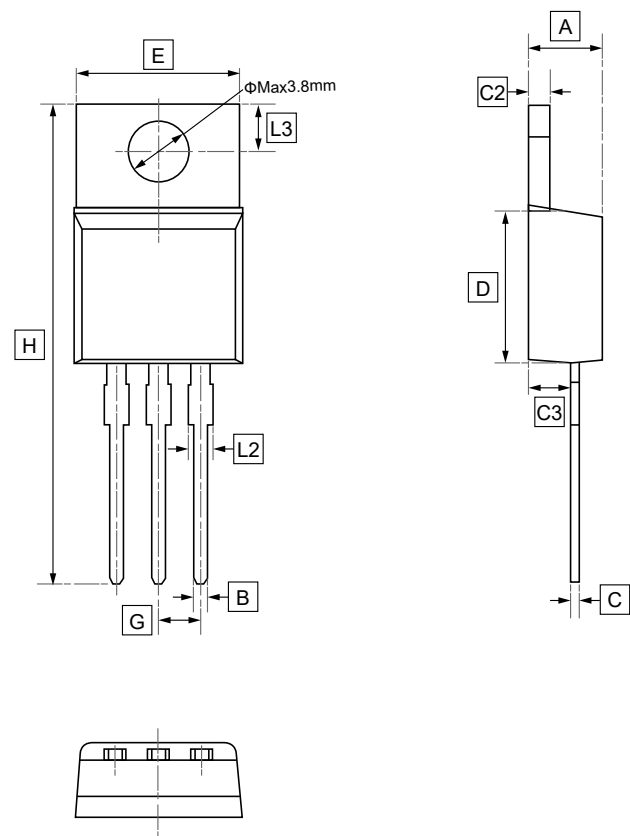
DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	A3	B	B1	C	C1	D	E	F	G
Min	9.7	8.44	1.05	4.8	15.4	12.9	4.28	1.1	0.6	3.4	2.65	5.2
Max	10.3	8.84	1.25	5.2	16.2	13.5	4.68	1.5	1.0	3.8	3.25	5.8

Symbol	H	K	L	L1	M	N	P	Q	T	DIA
Min	0.4	2.9	12.8	2.7	1.15	2.49	2.1	8.7	W:0.35	⌀1.5
Max	0.6	3.3	13.6	3.3	1.35	2.59	2.7	9.3		(deep 0.2)



8.2 TO-220 Package Outline Dimensions

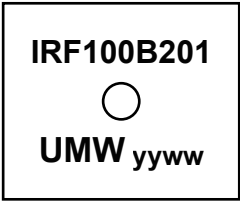


DIMENSIONS (mm are the original dimensions)

Symbol	A	B	C	C2	C3	D	E	G	H	L2	L3
Min	4.30	0.60	0.28	1.17	2.30	8.80	9.80	2.44	28.55	1.10	2.59
Max	4.70	1.00	0.48	1.37	2.70	9.20	10.20	2.64	29.15	1.50	2.89



9.Ordering Information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW IRF100B201	TO-220	1000	Tube and box



10.Disclaimer

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