1.Description

The UMW SN74LVC1G14 is a Schmitt trigger function of the NOT gate integrated circuit, can realize mathematical logic operation. The chip is designed on an advanced CMOS process, featuring low power consumption and high output drive capability. The chip works well with a V_{CC} supply voltage between 1.65 V and 5.5V. The UMW 74LVC1G14 is available in a variety of small package forms, which can be widely used in high-end precision instruments, miniaturized low-power handheld devices,andartificialintelligence.

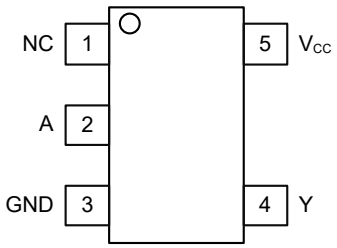
2.Features

- Low input current: 0.01μA typical
- Wide operating range: 1.65V to 5.5V
- Low quiescent power consumption: 0.1uA typical
- Package: SOT23-5/SC70-5/SOT-553, DFN/SON-6, DSBGA-5, X2SON-5
- High output drive V_{CC}=4.5V, greater than 32MA

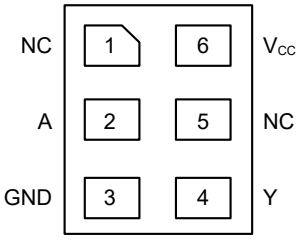
3.Product Usage

- Portable audio interface Blu-ray player and home theater
- Digital TV
- Solid state hard disk
- Intelligent wearable devices, such as wireless headphones, smart watches, etc

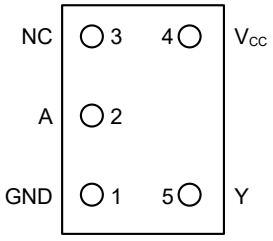
4.Pinning information



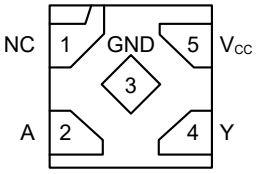
SOT23-5/SC70-5
SOT-553



DFN/SON-6



DSBGA-5



X2SON-5

5.Pin Function

Pin					Description
Name	SOT23-5/SC70-5/SOT-553	DFN/SON-6	DSBGA-5	X2SON-5	
NC	1	1,5	A1, B2	1	Empty foot
A	2	2	B1	2	Input
GND	3	3	C1	3	Power supply ground
Y	4	4	C2	4	Output
V_{CC}	5	6	A2	5	Power supply positive

Notes: NC null pin, no connecting wire inside.

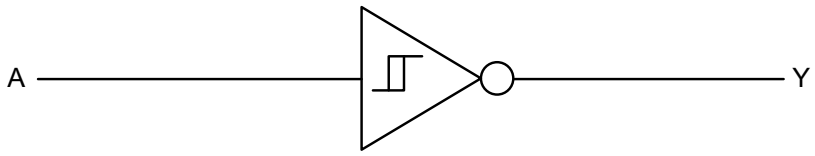
6.Limit parameter

Parameter	Symbol	Limit Value	Unit
operating voltage	V_{CC}	6.5	V
Input	V_{IN}	-0.5 ~ 6.5	V
Output voltage(1)	V_{OUT}	-0.5 ~ 6.5	V
Single pin output current	I_{OUT}	25	mA
V_{CC} or GND Current	I_{CC}	50	mA
Working Temperature	T_A	-40 to 125	°C
Storage temperature	T_S	-65 to 150	°C
Lead Soldering Temperature	T_W	260, 10s	°C

Note: 1. Under V_{CC}=0V power-off state, the output can withstand the limit voltage.

2. The limit parameter refers to the limit value which cannot be exceeded under any condition.If this limit value is exceeded, physical damage such as product degradation may be caused; at the same time, near the limit parameters, it is impossible to guarantee that the chip can work normally.

7.Principle Logic Diagram



Function Table

Input	Output
A	**Y**
L	H
H	L

8.Operating Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating Voltage	V_{CC}		1.65		5.5	V
Input High Level Voltage	V_{IH}	V_C=1.65V~1.95V	0.65*V_{CC}			V
		V_C=2.3V~2.7V	1.7			V
		V_C=3V~5.5V	0.7*V_{CC}			V
Low-level Input Voltage	V_{IL}	V_C=1.65V~1.95V			0.35*V_{CC}	V
		V_C=2.3V~2.7V			0.7	V
		V_C=3V~5.5V			0.3*V_{CC}	V
Input Voltage	V_I		0		5.5	V
Output Voltage	V_O		0		V_{CC}	V
High Level Output Current	I_{OH}	V_C=1.65V			-4	mA
		V_C=2.3V			-8	mA
		V_C=3V			-16	mA
		V_C=4.5V			-32	mA
Low Level Output Current	I_{OL}	V_C=1.65V			4	mA
		V_C=2.3V			8	mA
		V_C=3V			16	mA
		V_C=4.5V			32	mA

9.DC Electrical Characteristics (T_A=25°C)

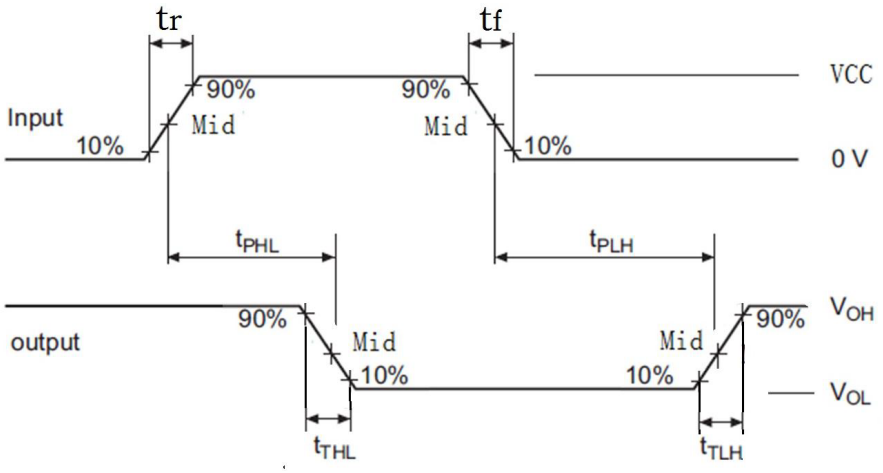
Parameter	Symbol	Conditions	V_{CC}	Min	Max	Unit
Upper critical voltage	VT+		1.65	0.79	1.16	V
			2.3	1.11	1.56	V
			3	1.5	1.87	V
			4.5	2.16	2.74	V
			5.5	2.61	3.33	V
lower critical voltage	VT-		1.65	0.39	0.62	V
			2.3	0.58	0.87	V
			3	0.84	1.14	V
			4.5	1.41	1.79	V
			5.5	1.87	2.29	V
Hysteresis Width Voltage	ΔV_T (VT+ - VT-)		1.65	0.37	0.62	V
			2.3	0.48	0.77	V
			3	0.56	0.87	V
			4.5	0.71	1.04	V
			5.5	0.71	1.11	V
High Level Load Voltage	V_{OH}	I_{OH}=-100μA	1.65~5.5	VCC-0.1		V
		I_{OH}=-4mA	1.65	1.2		V
		I_{OH}=-8mA	2.3	1.9		V
		I_{OH}=-16mA	3	2.4		V
		I_{OH}=-32mA	4.5	2.3		V
Low Level Load Voltage	V_{OL}	I_{OH}=100μA	1.65~5.5	3.8	0.1	V
		I_{OH}=4mA	1.65		0.45	V
		I_{OH}=8mA	2.3		0.3	V
		I_{OH}=16mA	3		0.4	V
		I_{OH}=32mA	4.5		0.55	V

Parameter	Symbol		Conditions	V_{cc}	Typ	Max	Unit
Input Current	I_I	A	V_I=5.5V or GND	0~5.5	0.01	±5	μA
Shutdown Current	I_{OFF}	V_I	V_I=5.5V	0	0.01	±10	μA
		V_O	V_O=5.5V	0	0.01	±10	μA
Operating current	I_{CC}		V_I=5.5V, I_O=0	1.65~5.5	0.01	10	μA
			V_I=GND, I_O=0	1.65~5.5	0.01	10	μA
Operating current variation value	ΔI_{CC}		A=V_{CC}-0.6V	3~5.5	25		μA

10.AC Electrical Characteristics

Ta=25°C, V_{CC}=5.0V, tr = tf ≤ 20ns, see test method.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Maximum transmission	t_{PHL}	C_L=15pF		20		ns
delay time A, B to Y	t_{PLH}			20		ns

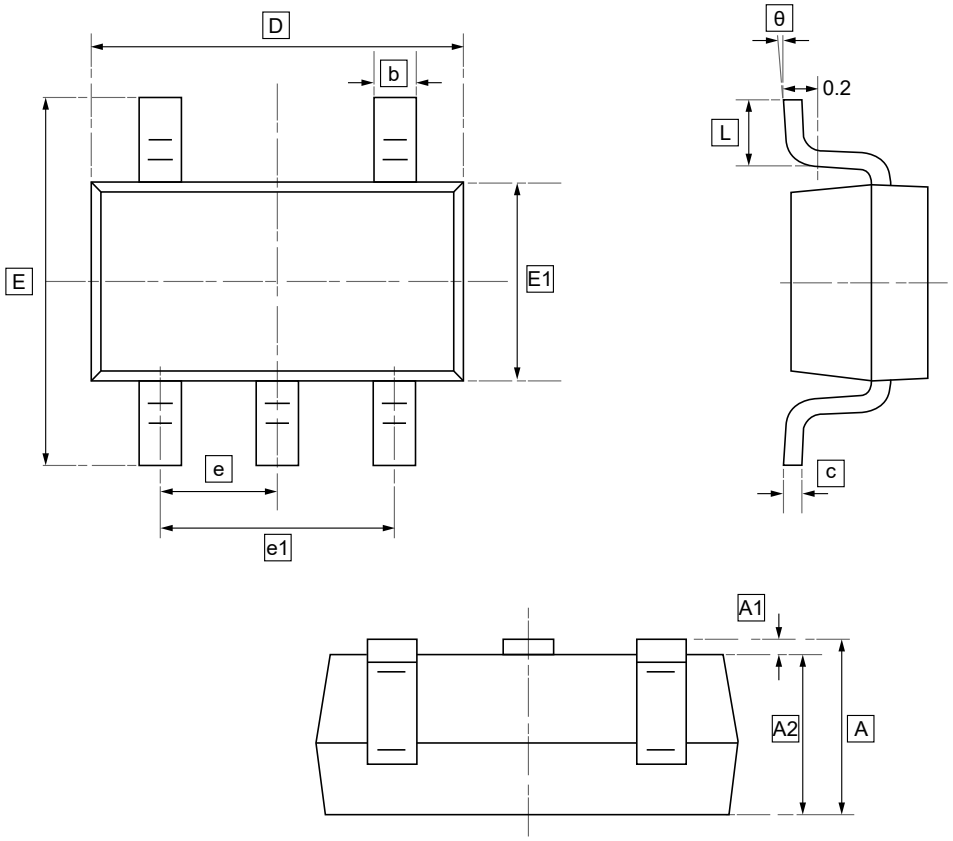


Note: 1. CL capacitor is external chip capacitor (0603), which is connected close to the output pin, and the capacitor ground is close to the chip GND;

2. Input: port input level, f=500kHz,D=50%; tr=tf≤20ns;

3. Output: Y-terminal output test.

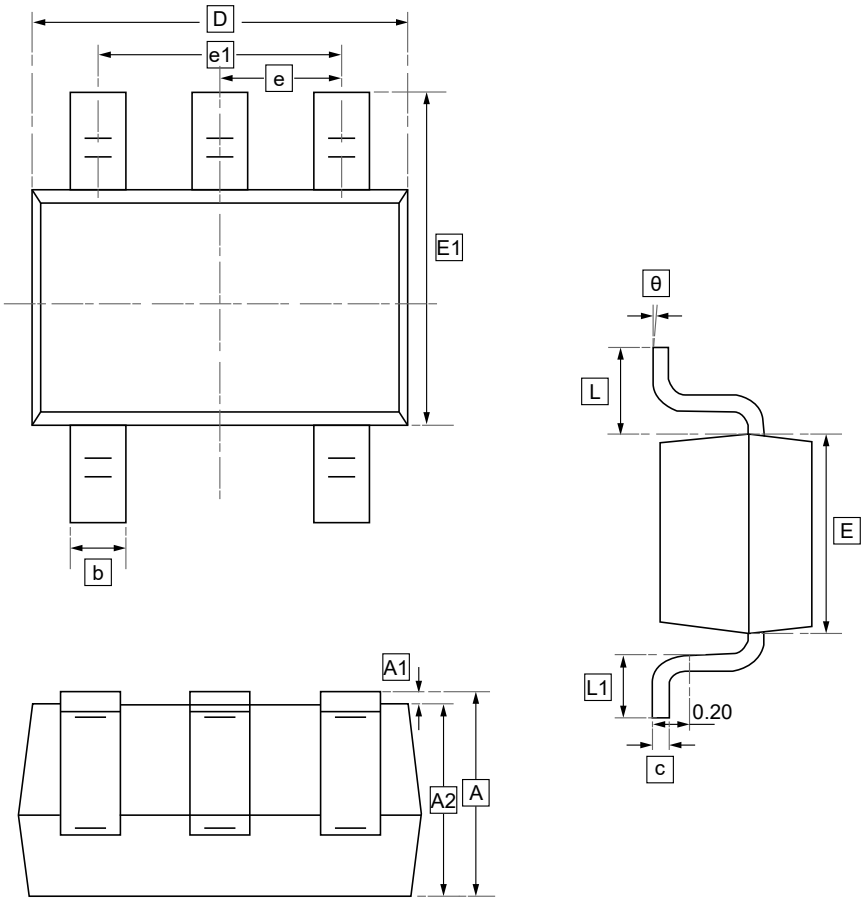
11.1 SOT23-5 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	c	D	E1	E	e	e1	L	θ
Min	1.050	0.000	1.050	0.300	0.100	2.820	1.500	2.650	0.950	1.800	0.300	0°
Max	1.250	0.100	1.150	0.500	0.200	3.020	1.700	2.950	BSC	2.000	0.600	8°

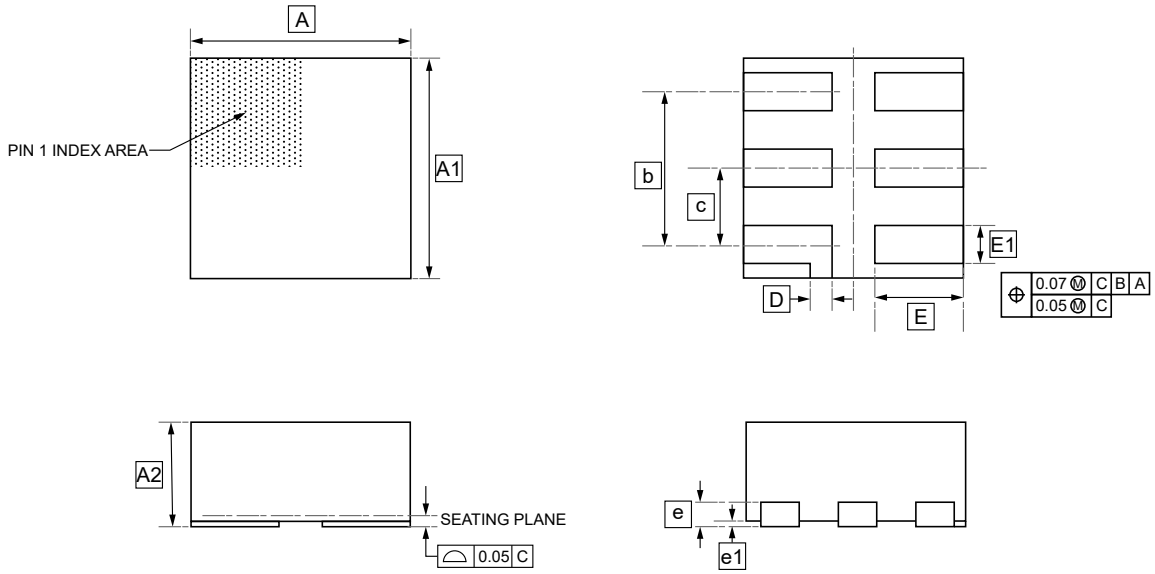
11.2 SC70-5 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	c	D	E	E1	e	e1	L	θ
Min	0.90	0.00	0.90	0.15	0.08	2.05	1.15	2.15	0.65	1.20	0.26	7°
Max	1.10	0.10	1.00	0.35	0.15	2.25	1.35	2.45	TYP	1.40	0.46	REF.

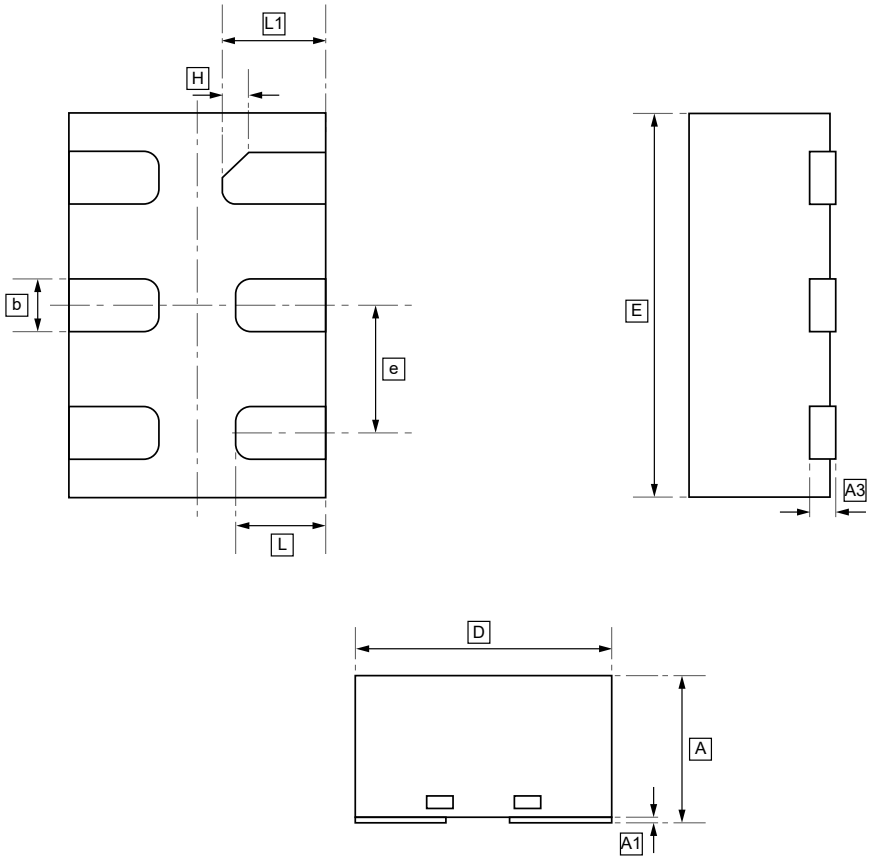
11.3 SON-6 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	c	D	E	E1	e	e1
Min	0.95	0.95	-	0.7	0.35	0.1	0.35	0.12	0.11	0.00
Max	1.05	1.05	0.4				0.45	0.22	TYP	0.05

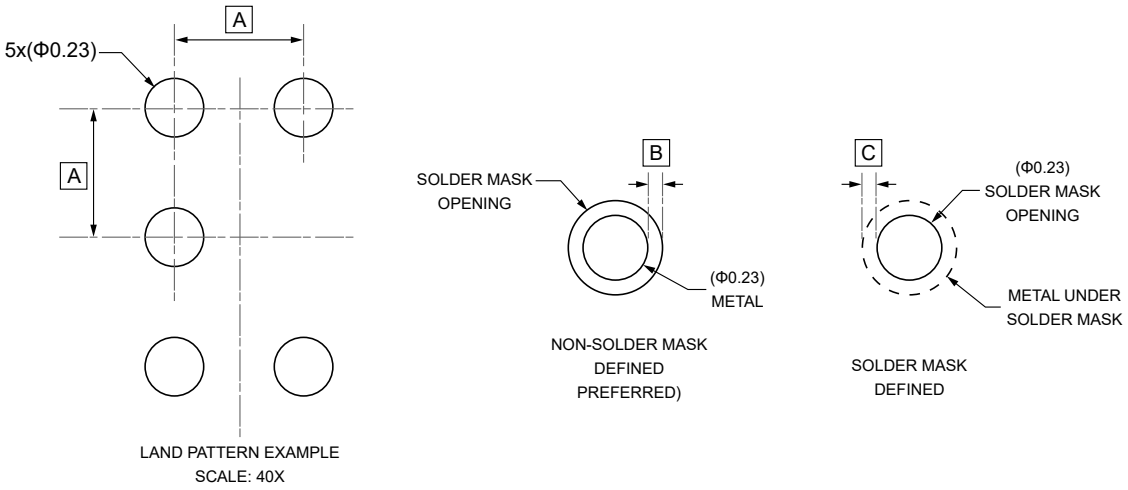
11.4 DFN6(1x1.5) Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A3	b	D	E	e	H	L	L1
Min	0.50	0	0.10	0.15	0.90	1.40	0.40	0.10	0.30	0.35
Max	0.60	0.05	REF	0.25	1.10	1.60	0.60	REF	0.40	0.45

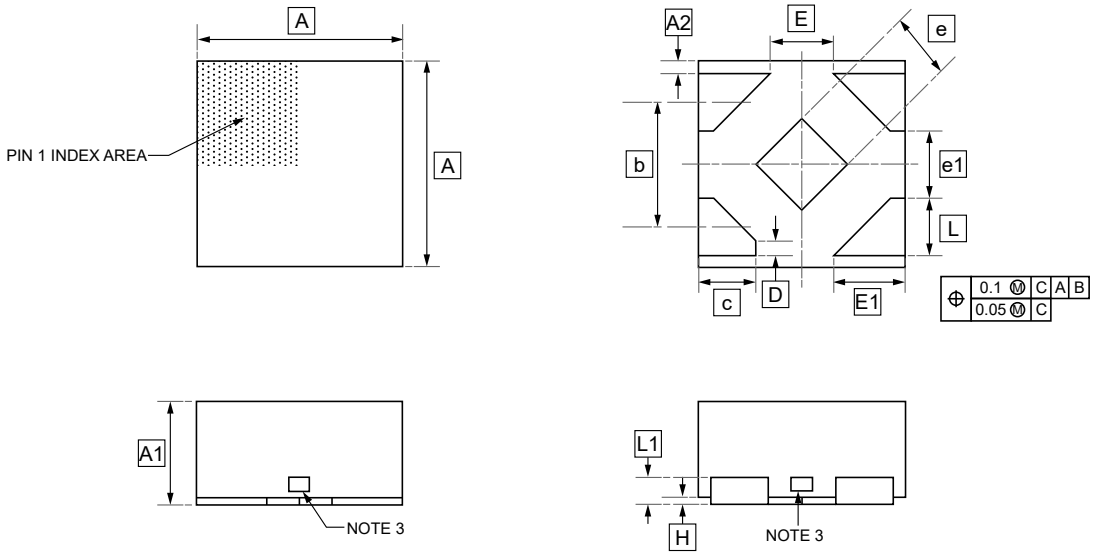
11.5 DSBGA-5 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	B	C
Min	0.5	-	0.05
Max	TYP	0.05	-

11.6 X2SON-5 Package Outline Dimensions

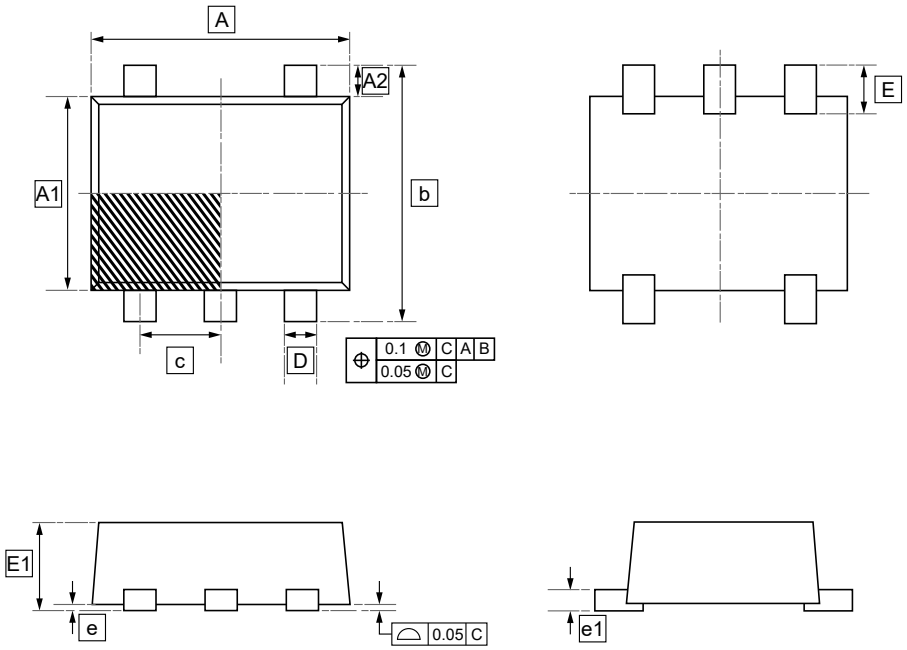


DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	c	D	E	E1	e	e1	L	L1
Min	0.75	-	0.05	0.48	0.17	0.06	0.25	0.23	0.15	0.26	0.17	0.1
Max	0.85	0.4			0.27			0.32	0.35		0.27	

Symbol	H
Min	0.00
Max	0.05

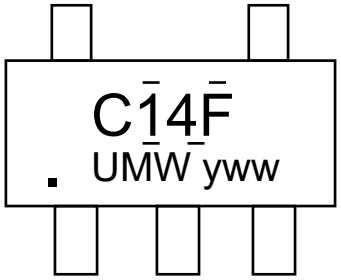
11.7 SOT-553 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	c	D	E	E1	e	e1
Min	1.50	1.10	0.13	1.50	0.50	0.15	0.20	0.50	0.00	0.08
Max	1.70	1.30	0.27	1.70		0.25	0.40	0.60	0.05	0.18

12.Ordering Information



yww: Batch Code

Order Code	Marking	Package	Base QTY	Delivery Mode
UMW SN74LVC1G14DBVR	C14F	SOT23-5	3000	Tape and reel
UMW SN74LVC1G14DCKR	CFR	SC70-5	3000	Tape and reel
UMW SN74LVC1G14YZPR	CF7	DSBGA-5	3000	Tape and reel
UMW SN74LVC1G14DPWR	9H	X2SON-5	3000	Tape and reel
UMW SN74LVC1G14DRLR	CFR	SOT-553	4000	Tape and reel
UMW SN74LVC1G14DSFR	CF	SON-6	5000	Tape and reel
UMW SN74LVC1G14DRYR	CF	DFN(1*1.5)	5000	Tape and reel

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