UMW FDP8D5N10C

100V N-Channel MOSFET

1.Description

This N-Channel MV MOSFET is produced using process that has been optimized to minimize on-state resistance and yet maintain superior switching performance with best in class soft body diode.

2.1Features

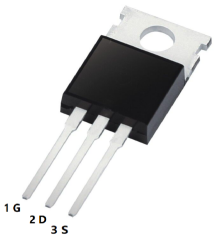
- $V_{DS\ (V)}$=100V
- I_D=76A
- $R_{DS(ON)}$<8.5mΩ(V_{GS}=10V)

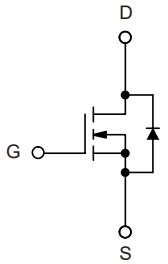
2.2Features

- Low Gate Charge
- Fast Switching
- Improved dv/dt Capability
- RoHS Compliant

3.Pinning information

Pin	Symbol	Description
1	G	GATE
2	D	SOURCE
3	S	DRAIN





4.Absolute Maximum Ratings T_C= 25°C

Parameter			Symbol	Rating	Units
Drain to Source Voltage			V_{DS}	100	V
Gate to Source Voltage			V_{GS}	±20	V
Drain Current - Continuous	T_C=25°C	(Note 3)	I_D	76	A
- Continuous	T_C=100°C	(Note 3)		54	A
- Pulsed		(Note 1)		304	A
Single Pulse Avalanche Energy		(Note 2)	E_{AS}	181	mJ
Power Dissipation	T_C=25°C		P_D	107	W
Power Dissipation	T_A=25°C			2.4	W
Storage Temperature Range			T_J, T_{STG}	-55 to 175	°C

* Drain current limited by maximum junction temperature.

5.Thermal Characteristics

Parameter	Symbol	Rating	Units
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.4	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

6.Electrical Characteristic (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain to Source Breakdown Voltage	BV_{DSS}	I_D=250μA, V_{GS}=0V	100			V
Breakdown Voltage Temperature Coefficient	$\frac{\Delta BV_{DSS}}{\Delta T_J}$	I_D=250μA Referenced to 25°C		57		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=80V, V_{GS}=0V			1	μA
		V_{DS}=80V, T_J=150°C			500	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V			±100	nA
Gate to Source Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=130μA	2	3	4	V
Static Drain to Source On Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=76A		7.4	8.5	mΩ
Forward Transconductance	g_{FS}	V_{DS}=5V, I_D=76A		68		S
Input Capacitance	C_{iss}	V_{DS}=50V, V_{GS}=0V, f=1MHz		1765	2475	pF
Output Capacitance	C_{oss}			1010	1415	pF
Reverse Transfer Capacitance	C_{rss}			16	25	pF
Gate Resistance	R_g		0.1	0.8	1.6	Ω
Turn-On Delay Time	$t_{D(on)}$	V_{DD}=50V, I_D=76A V_{GS}=10V,R_{GEN}=6Ω		12	22	ns
Rise Time	t_r			11	20	ns
Turn-Off Delay Time	$t_{D(off)}$			18	28	ns
Fall Time	t_f			4	10	ns
Total Gate Charge	Q_g	V_{GS}=0V to 10 V, V_{DD}=50V, I_D=76A		25	34	nC
Gate to Source Gate Charge	Q_{gs}			9		nC
Gate to Drain “Miller” Charge	Q_{gd}			5		nC
Output Charge	Q_{oss}	V_{DD}=50V, V_{GS}=0V		68		nC
Maximum Continuous Drain to Source Diode Forward Current	I_S				76	A
Maximum Pulsed Drain to Source Diode Forward Current	I_{SM}				304	A

Source to Drain Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_S=76 A		1	1.3	V
Reverse Recovery Time	t_{rr}	V_{GS}=0V, V_{DD}=50V, I_F=76A		58	92	ns
Reverse Recovery Charge	Q_{rr}	dI_F/dt=100A/μs		53	85	nC
Reverse Recovery Time	t_{rr}	V_{GS}=0V, V_{DD}=50V, I_F=76A		51	81	ns
Reverse Recovery Charge	Q_{rr}	dI_F/dt=300A/μs		141	226	nC

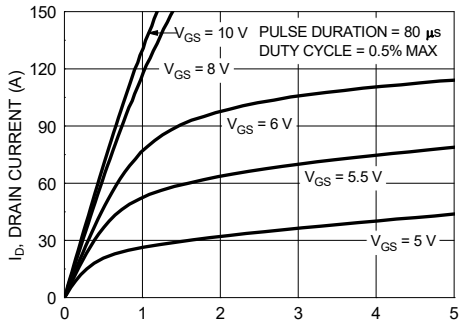
Notes:

1. Pulsed Id please refer to Figure 11 & Figure 12 “Forward Bias Safe Operating Area” for more details.

2. E_{AS} of 181 mJ is based on starting T_J= 25°C, L=3 mH, I_{AS}=11 A, V_{DD}=100 V, V_{GS}=10 V. 100% test at L = 0.3 mH, I_{AS}=25 A.

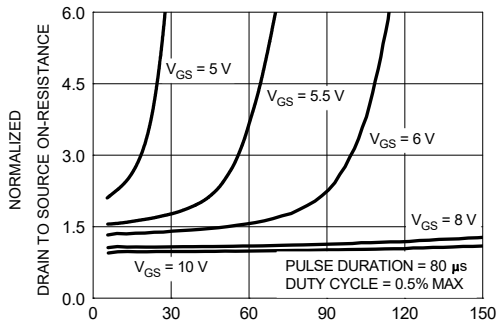
3. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

7.1Typical characteristic



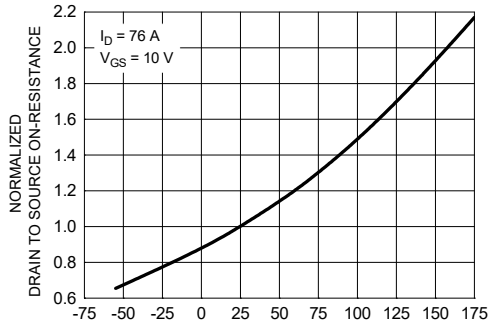
$V_{DS,}$, DRAIN TO SOURCE VOLTAGE (V)

Figure 1: On-Region Characteristics



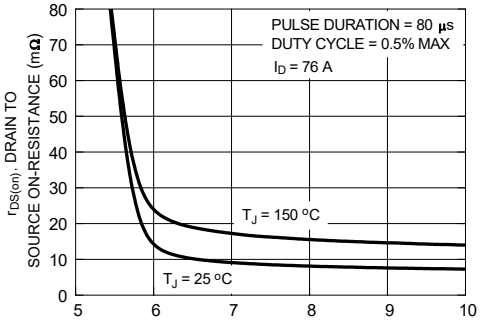
I_D, DRAIN CURRENT (A)

Figure 2: Normalized On-Resistance vs. Drain Current and Gate Voltage



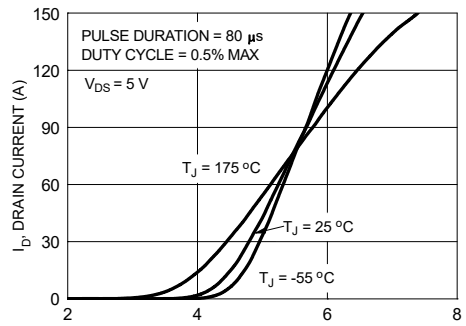
T_J, JUNCTION TEMPERATURE (°C)

Figure 3: Normalized On Resistance vs. Junction Temperature



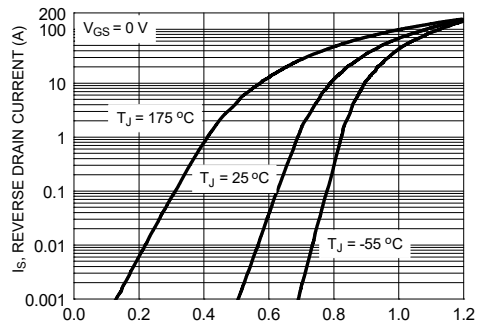
V_{GS}, GATE TO SOURCE VOLTAGE (V)

Figure 4: On-Resistance vs. Gate to Source Voltage



V_{GS}, GATE TO SOURCE VOLTAGE (V)

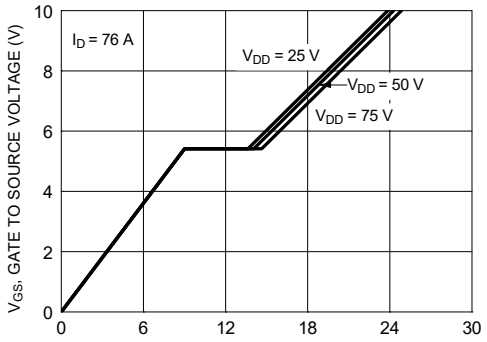
Figure 5: Transfer Characteristics



V_{SD}, BODY DIODE FORWARD VOLTAGE (V)

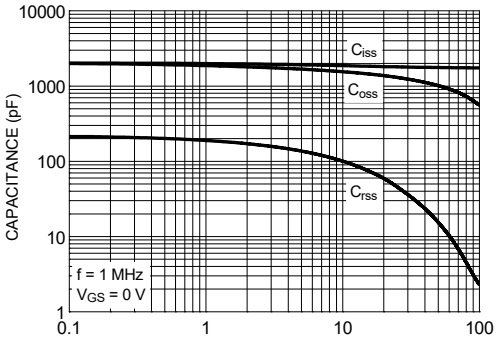
Figure 6: Source to Drain Diode Forward Voltage vs. Source Current

7.2Typical characteristic



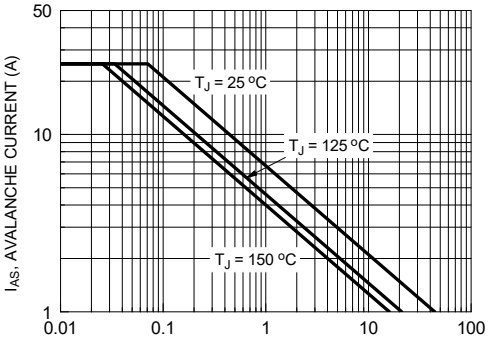
Q_g, GATE CHARGE (nC)

Figure 7: Gate Charge Characteristics



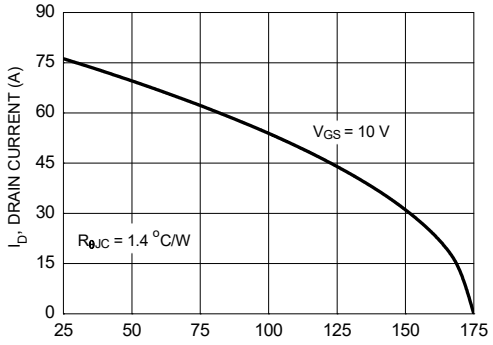
V_{DS}, DRAIN TO SOURCE VOLTAGE (V)

Figure 8: Capacitance vs. Drain to Source Voltage



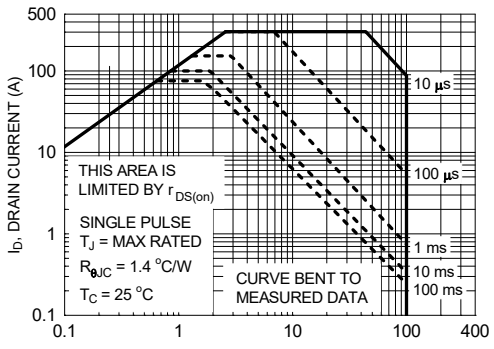
t_{AV}, TIME IN AVALANCHE (ms)

Figure 9: Unclamped Inductive Switching Capability



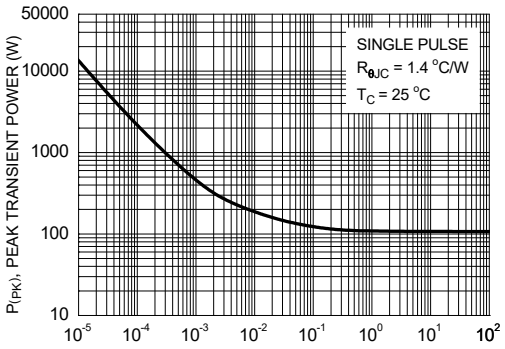
T_C, , CASE TEMPERATURE(°C)

Figure 10: Maximum Continuous Drain Current vs Case Temperature



V_{DS}, DRAIN to SOURCE VOLTAGE (V)

Figure 11: Forward Bias Safe Operating Area for FDP8D5N10C



t, PULSE WIDTH (sec)

Figure 12: Single Pulse Maximum Power Dissipation for FDP8D5N10C

7.3Typical characteristic

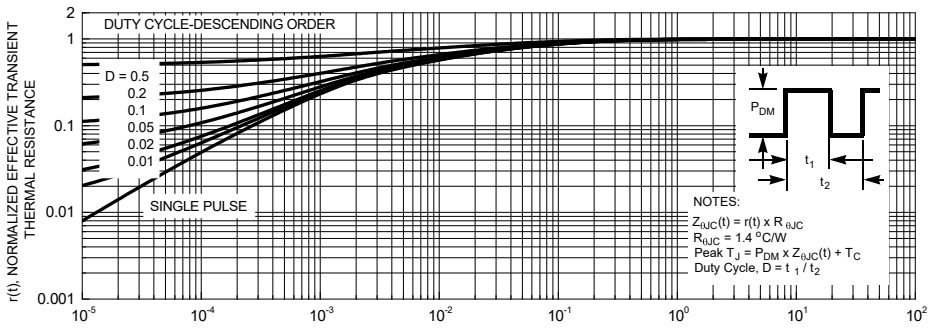


Figure 13: Junction-to-Case Transient Thermal Response Curve for FDP2D3N10C

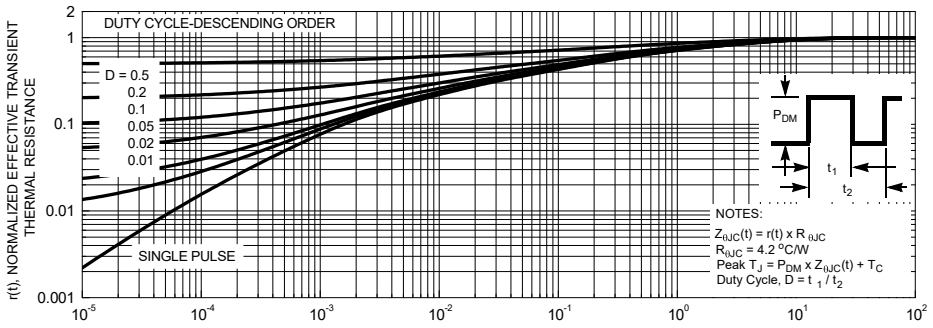
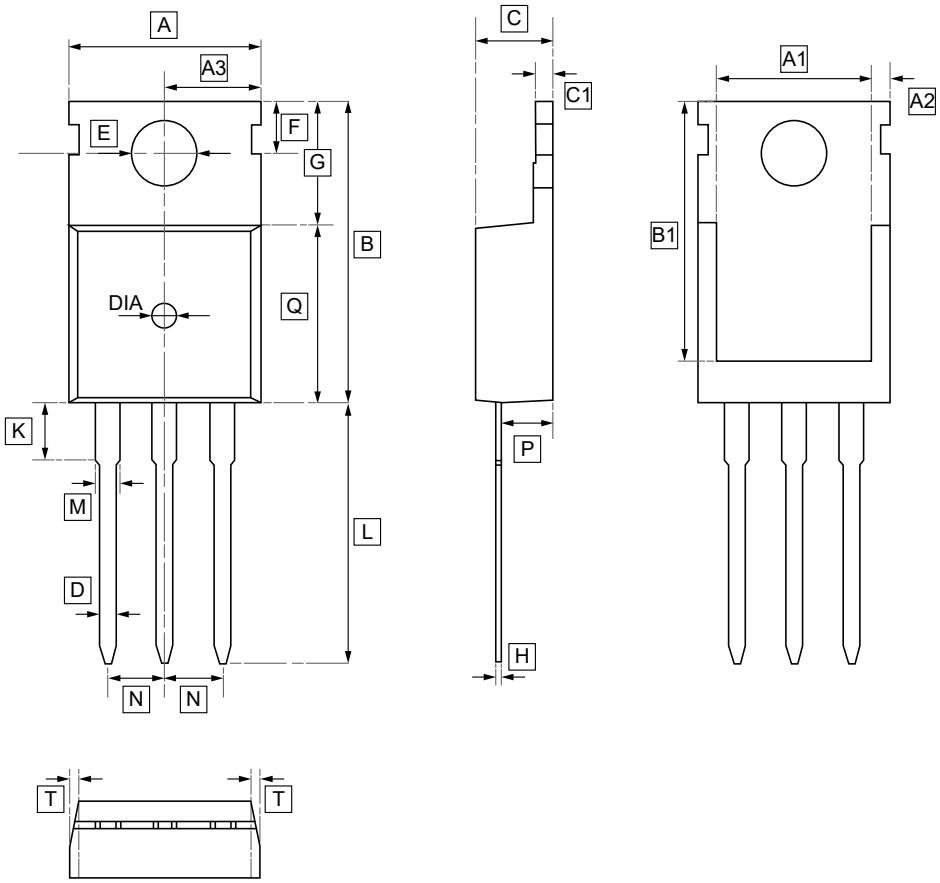


Figure 14: Junction-to-Case Transient Thermal Response Curve for FDPF2D3N10C

8.1 TO-220 Package Outline Dimensions

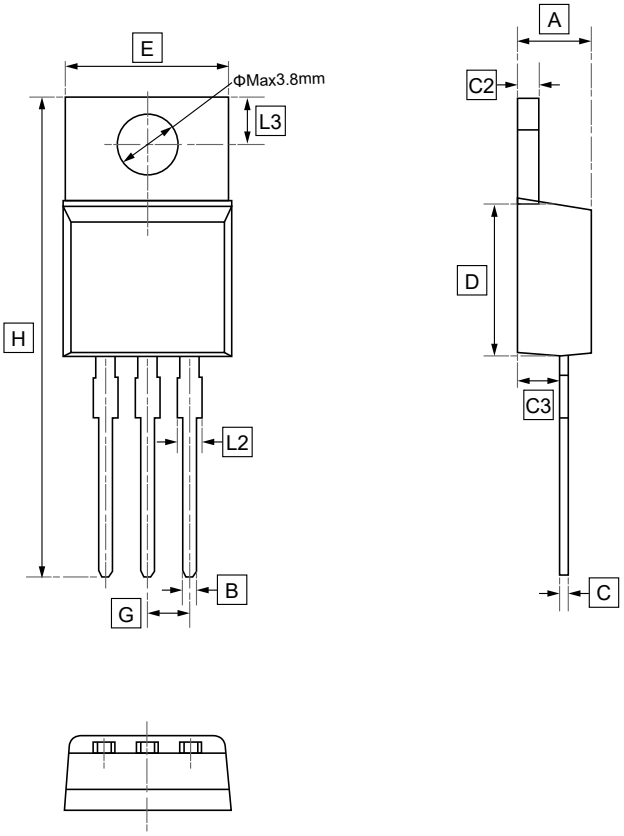


DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	A3	B	B1	C	C1	D	E	F	G
Min	9.7	8.44	1.05	4.8	15.4	12.9	4.28	1.1	0.6	3.4	2.65	5.2
Max	10.3	8.84	1.25	5.2	16.2	13.5	4.68	1.5	1.0	3.8	3.25	5.8

Symbol	H	K	L	L1	M	N	P	Q	T	DIA
Min	0.4	2.9	12.8	2.7	1.15	2.49	2.1	8.7	W:0.35	⊙1.5 (deep 0.2)
Max	0.6	3.3	13.6	3.3	1.35	2.59	2.7	9.3		

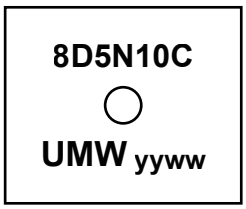
8.2 TO-220 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	B	C	C2	C3	D	E	G	H	L2	L3
Min	4.30	0.60	0.28	1.17	2.30	8.80	9.80	2.44	28.55	1.10	2.59
Max	4.70	1.00	0.48	1.37	2.70	9.20	10.20	2.64	29.15	1.50	2.89

9.Ordering Information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW FDP8D5N10C	TO-220	1000	Tube and box

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